Lattice Semiconductor Corporation - OR2T15A6BA256-DB Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1600
Total RAM Bits	25600
Number of I/O	223
Number of Gates	44200
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or2t15a6ba256-db

Table 3. ORCA Series 2TA System Performance

Function	# PFUs	Speed Grade				Unit
		-4	-5	-6	-7	
16-bit loadable up/down counter	4	87.0	104.2	129.9	144.9	MHz
16-bit accumulator	4	87.0	104.2	129.9	144.9	MHz
8 x 8 parallel multiplier:						
— Multiplier mode, unpipelined[1]	22	25.1	31.0	36.0	40.3	MHz
— ROM mode, unpipelined[2]	9	71.9	87.7	107.5	122.0	MHz
— Multiplier mode, pipelined[3]	44	82.0	103.1	125.0	142.9	MHz
32 x 16 RAM:						
— Single port (read and write/ cycle)[4]	9	36.2	53.8	53.8	62.5	MHz
— Single port[5]	9	69.0	92.6	92.6	96.2	MHz
— Dual port[6]	16	83.3	92.6	92.6	96.2	MHz
36-bit parity check (internal)	4	9.1	7.4	5.6	5.2	ns
32-bit address decode (internal)	3.25	7.5	6.1	4.6	4.3	ns

1. Implemented using 4 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 16 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 4 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (28 of 44 PFUs contain only pipelining registers).
4. Implemented using 16 x 4 synchronous single-port RAM mode allowing both read and write per clock cycle, including write/read address multiplexer.
5. Implemented using 16 x 4 synchronous single-port RAM mode allowing either read or write per clock cycle, including write/read address multiplexer.
6. Implemented using 16 x 2 synchronous dual-port RAM mode.

SELECT DEVICES DISCONTINUED

Programmable Logic Cells (continued)

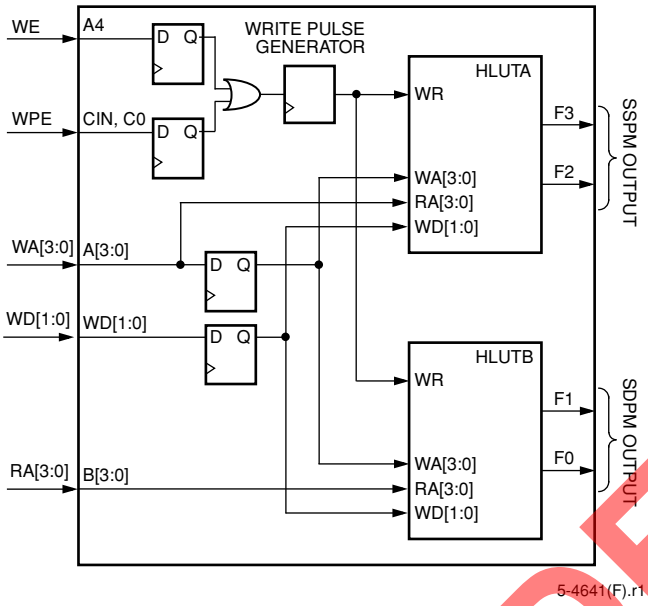

Figure 17. SDPM Mode—16 x 2 Synchronous Dual-Port Memory

The Series 2 devices have added a second synchronous memory mode known as the ***synchronous dual-port memory*** (SDPM) mode. This mode writes data into the memory synchronously in the same manner described previously for SSPM mode. The SDPM mode differs in that two separate 16 x 2 memories are created in each PFU that have the same WE, WPE, write data (WD[1:0]), and write address (WA[3:0]) inputs, as shown in Figure 17.

The outputs of HLUTA (F[3:2]) operate the same way they do in SSPM mode—the read address comes directly from the A[3:0] inputs used to create the latched write address. The outputs of HLUTB (F[1:0]) operate in a dual-port mode where the write address comes from the latched version of A[3:0], and the read address comes directly from RA[3:0], which is input on B[3:0].

Since external multiplexing of the write address and read address is not required, extremely fast RAMs can be created. New system applications that require an interface between two different asynchronous clocks can also be implemented using the SDPM mode. An example of this is accomplished by creating FIFOs where one clock controls the synchronous write of data into the FIFO, and the other clock controls the read address to allow reading of data at any time from the FIFO.

Latches/Flip-Flops

The four latches/FFs in the PFU can be used in a variety of configurations. In some cases, the configuration options apply to all four latches/FFs in the PFU. For other options, each latch/FF is independently programmable.

Table 6 summarizes these latch/FF options. The latches/FFs can be configured as either positive or negative level-sensitive latches, or positive or negative edge-triggered flip-flops. All latches/FFs in a given PFU share the same clock, and the clock to these latches/FFs can be inverted. The input into each latch/FF is from either the corresponding QLUT output (F[3:0]) or the direct data input (WD[3:0]). For latches/FFs located in the two outer rings of PLCs, additional inputs are possible. These additional inputs are fast paths from I/O pads located in PICs in the same row or column as the PLCs. If the latch/FF is not located in the two outer rings of the PLCs, the latch/FF input can also be tied to logic 0, which is the default. The four latch/FF outputs, Q[3:0], can be placed on the five PFU outputs, O[4:0].

Table 6. Configuration RAM Controlled Latch/Flip-Flop Operation

Function	Options
Functionality Common to All Latch/FFs in PFU	
LSR Operation	Asynchronous or synchronous
Clock Polarity	Noninverted or inverted
Front-End Select	Direct (WD[3:0]) or from LUT (F[3:0])
LSR Priority	Either LSR or CE has priority
Functionality Set Individually in Each Latch/FF in PFU	
Latch/FF Mode	Latch or flip-flop
Set/Reset Mode	Set or Reset

The four latches/FFs in a PFU share the clock (CK), clock enable (CE), and local set/reset (LSR) inputs. When CE is disabled, each latch/FF retains its previous value when clocked. Both the clock enable and LSR inputs can be inverted to be active-low.

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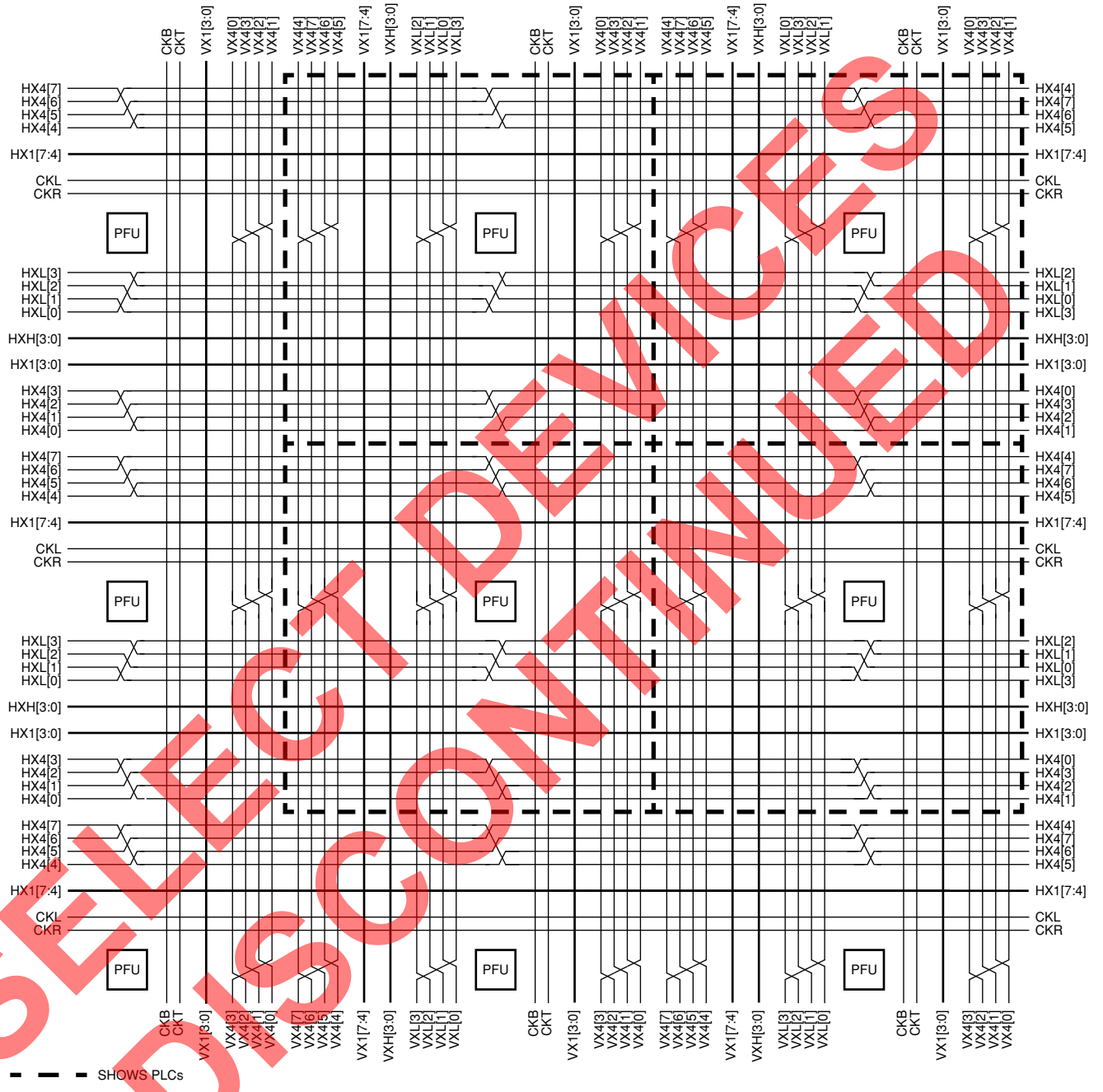
Programmable Logic Cells (continued)



SELECT DEVICES DISCONTINUED

Figure 22. Multiple PLC View of Inter-PLC Routing

Programmable Input/Output Cells

(continued)

PIC Architectural Description

The PIC architecture given in Figure 26 is described using the following letter references. The figure depicts a PIC at the top of the array, so inter-PIC routing is horizontal and the indirect PIC-PLC routing is horizontal to vertical. In some cases, letters are provided in more than one location to indicate the path of a line.

A. As in the PLCs, the PIC contains a set of lines which run the length (width) of the array. The PXL lines connect in the corners of the array to other PXL lines. The PXL lines also connect to the PIC BIDI, PIC BIDIH, and LLDRV lines. As in the PLC XL lines, the PXH lines twist as they propagate through the PICs.

B. As in the PLCs, the PIC contains a set of lines which run one-half the length (width) of the array. The PXH lines connect in the corners and in the middle of the array perimeter to other PXH lines. The PXH lines also connect to the PIC BIDI, PIC BIDIH, and LLDRV lines. As in the PLC XH lines, the PXH lines do not twist as they propagate through the PICs.

C. The PX2[3:0] lines span a length of two PICs before intersecting with a CIP. The CIP allows the length of a path using PX2 lines to be extended two PICs.

D. The PX1[3:0] lines span a single PIC before intersecting with a CIP. The CIP allows the length of a path using PX1 lines to be extended by one PIC.

E. These are four dedicated direct output lines connected to the output buffers. The DOUT[3:0] signals go directly from a PLC latch/FF to an output buffer, minimizing the latch/FF to pad propagation delay.

F. This is a direct path from the input pad to the PLC latch/flip-flops in the two rows (columns) adjacent to PICs. This input allows a reduced setup time. Direct inputs from the top and bottom PIC rows are PDINTB[3:0]. Direct inputs from the left and right PIC columns are PDINLR[3:0].

G. The OUT[3:0], TS[3:0], and IN[3:0] signals for each I/O pad can be routed directly to the adjacent PLC's switching lines.

H. The four TRIDI buffers allow connections from the pads to the PLC XL lines. The TRIDIs also allow connections between the PLC XL lines and the PBIDI lines, which are described in ***J*** below.

I. The four TRIDIH buffers allow connections from the pads to the PLC XH lines. The TRIDIHs also allow connections between the PLC XH lines and the pBIDIH lines, which are described in ***K*** below.

J. The PBIDI lines (bidi[3:0]) connect the PXL lines, PXH lines, and the PX1 lines. These are bidirectional in that the path can be from the PXL, PXH, or PX1 lines to the XL lines, or from the XL lines to the PXL, PXH, or PX1 lines.

K. The pBIDIH lines (BIDIH[3:0]) connect the PXL lines, PXH lines, and the PX1 lines. These are bidirectional in that the path can be from the PXL, PXH, or PX1 lines to the XH lines, or from the XH lines to the PXL, PXH, or PX1 lines.

L. The LLIN[3:0] lines provide a fast connection from the I/O pads to the XL and XH lines.

M. This set of CIPs allows the eight X1 lines (four on each side) of the PLC perpendicular to the PIC to be connected to either the PX1 or PX2 lines in the PIC.

N. This set of CIPs allows the eight X4 lines (four on each side) of the PLC perpendicular to the PIC to be connected to the PX1 lines. This allows fast access to/from the I/O pads from/to the PLCs.

O. All four of the PLC X4 lines in a group connect to all four of the PLC X4 lines in the adjacent PLC through a CIP. (This differs from the *ORCA* 1C Series in which two of the X4 lines in adjacent PLCs are directly connected without any CIPs.)

P. The long-line driver (LLDRV) line can be driven by the XSW4 switching line of the adjacent PLC. To provide connectivity to the pads, the LLDRV line can also connect to any of the four PXH or to one of the PXL lines. The 3-state enable (TS[i]) for all four I/O pads can be driven by XSW4, PXH, or PXL lines.

Q. For fast clock routing, one of the four I/O pads in each PIC can be selected to be driven onto a dedicated clock line. The clock line spans the length (width) of the PLC array. This dedicated clock line is typically used as a clock spine. In the PLCs, the spine is connected to an XL line to provide a clock branch in the perpendicular direction. Since there is another clock line in the PIC on the opposite side of the array, only one of the I/O pads in a given row (column) can be used to generate a global signal in this manner, if all PLCs are driven by the signal.

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FPGA States of Operation

Prior to becoming operational, the FPGA goes through a sequence of states, including initialization, configuration, and start-up. Figure 36 outlines these three FPGA states.

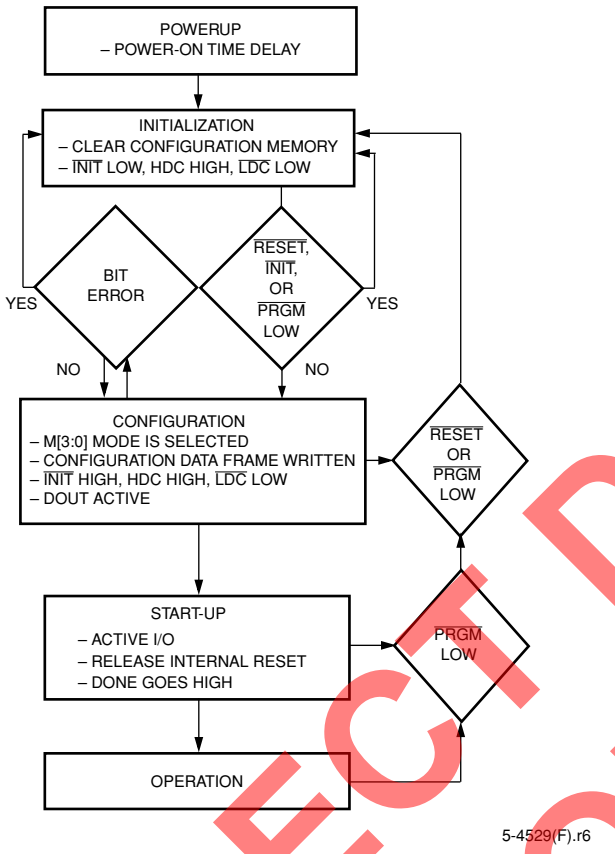

Figure 36. FPGA States of Operation

Initialization

Upon powerup, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When VDD reaches the voltage at which portions of the FPGA begin to operate (2.5 V to 3 V for the OR2CxxA, 2.2 V to 2.7 V for the OR2TxxA/OR2TxxB), the I/Os are configured based on the configuration mode, as determined by the mode select inputs M[2:0]. A time-out delay is initiated when VDD reaches between 3.0 V and 4.0 V (OR2CxxA) or 2.7 V to 3.0 V (OR2TxxA/2TxxB) to allow the power supply voltage to stabilize. The $\overline{\text{INIT}}$ and DONE outputs are low. At powerup, if VDD does not rise from 2.0 V to VDD in less than 25 ms, the user should delay configuration by inputting a low into $\overline{\text{INIT}}$, $\overline{\text{PRGM}}$, or $\overline{\text{RESET}}$ until VDD is greater than the recommended minimum operating voltage (4.75 V for OR2CxxA commercial devices and 3.0 V for OR2TxxA/B devices).

At the end of initialization, the default configuration option is that the configuration RAM is written to a low state. This prevents shorts prior to configuration. As a configuration option, after the first configuration (i.e., at reconfiguration), the user can reconfigure without clearing the internal configuration RAM first.

The active-low, open-drain initialization signal $\overline{\text{INIT}}$ is released and must be pulled high by an external resistor when initialization is complete. To synchronize the configuration of multiple FPGAs, one or more $\overline{\text{INIT}}$ pins should be wire-ANDed. If $\overline{\text{INIT}}$ is held low by one or more FPGAs or an external device, the FPGA remains in the initialization state. $\overline{\text{INIT}}$ can be used to signal that the FPGAs are not yet initialized. After $\overline{\text{INIT}}$ goes high for two internal clock cycles, the mode lines (M[3:0]) are sampled and the FPGA enters the configuration state.

The high during configuration (HDC), low during configuration ($\overline{\text{LDC}}$), and DONE signals are active outputs in the FPGA's initialization and configuration states. HDC, $\overline{\text{LDC}}$, and DONE can be used to provide control of external logic signals such as reset, bus enable, or PROM enable during configuration. For parallel master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

If configuration has begun, an assertion of $\overline{\text{RESET}}$ or $\overline{\text{PRGM}}$ initiates an abort, returning the FPGA to the initialization state. The $\overline{\text{PRGM}}$ and $\overline{\text{RESET}}$ pins must be pulled back high before the FPGA will enter the configuration state. During the start-up and operating states, only the assertion of $\overline{\text{PRGM}}$ causes a reconfiguration.

In the master configuration modes, the FPGA is the source of configuration clock (CCLK). In this mode, the initialization state is extended to ensure that, in daisy-chain operation, all daisy-chained slave devices are ready. Independent of differences in clock rates, master mode devices remain in the initialization state an additional six internal clock cycles after $\overline{\text{INIT}}$ goes high.

When configuration is initiated, a counter in the FPGA is set to 0 and begins to count configuration clock cycles applied to the FPGA. As each configuration data frame is supplied to the FPGA, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

SELECT DEVICES DISCONTINUED

FPGA Configuration Modes (continued)

Asynchronous Peripheral Mode

Figure 42 shows the connections needed for the asynchronous peripheral mode. In this mode, the FPGA system interface is similar to that of a microprocessor-peripheral interface. The microprocessor generates the control signals to write an 8-bit byte into the FPGA. The FPGA control inputs include active-low $\overline{CS0}$ and active-high CS1 chip selects, a write $\overline{WR}$ input, and a read $\overline{RD}$ input. The chip selects can be cycled or maintained at a static level during the configuration cycle. Each byte of data is written into the FPGA's D[7:0] input pins.

The FPGA provides a RDY status output to indicate that another byte can be loaded. A low on RDY indicates that the double-buffered hold/shift registers are not ready to receive data, and this pin must be monitored to go high before another byte of data can be written. The shortest time RDY is low occurs when a byte is loaded into the hold register and the shift register is empty, in which case the byte is immediately transferred to the shift register. The longest time for RDY to remain low occurs when a byte is loaded into the holding register and the shift register has just started shifting configuration data into configuration RAM.

The RDY status is also available on the D7 pin by enabling the chip selects, setting $\overline{WR}$ high, and applying $\overline{RD}$ low, where the $\overline{RD}$ input is an output enable for the D7 pin when $\overline{RD}$ is low. The D[6:0] pins are not enabled to drive when $\overline{RD}$ is low and, thus, only act as input pins in asynchronous peripheral mode.

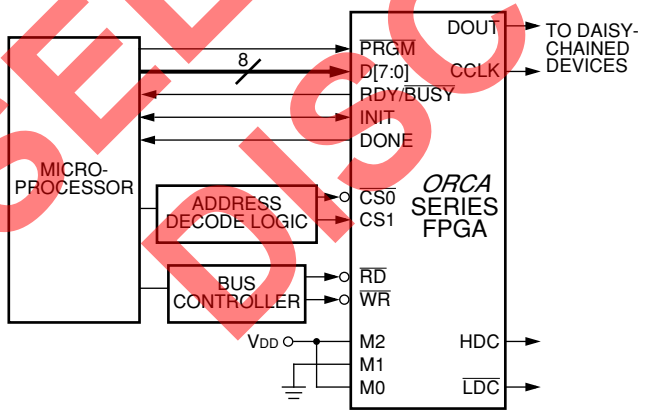

Figure 42. Asynchronous Peripheral Configuration Schematic

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after $\overline{INIT}$ goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The RDY signal is an output which acts as an acknowledge. RDY goes high one CCLK after data is clocked and, after one CCLK cycle, returns low. The process repeats until all of the data is loaded into the FPGA. The data begins shifting on DOUT 1.5 cycles after it is loaded in parallel. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 43 shows the connections for synchronous peripheral mode.

As with master modes, the peripheral modes can be used as the lead FPGA for a daisy chain of slave FPGAs.

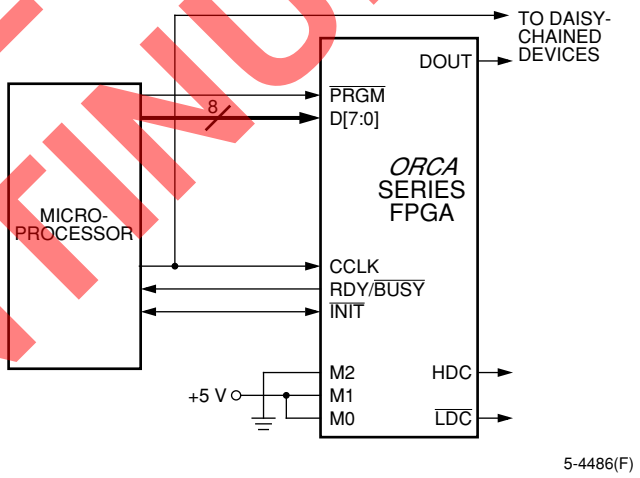

Figure 43. Synchronous Peripheral Configuration Schematic

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Special Function Blocks (continued)

ORCA Series TAP Controller (TAPC)

The *ORCA* Series TAP controller (TAPC) is a 1149.1 compatible test access port controller. The 16 JTAG state assignments from the *IEEE* 1149.1 specification are used. The TAPC is controlled by TCK and TMS. The TAPC states are used for loading the IR to allow three basic functions in testing: providing test stimuli (Update-DR), test execution (Run-Test/Idle), and obtaining test responses (Capture-DR). The TAPC allows the test host to shift in and out both instructions and test data/results. The inputs and outputs of the TAPC are provided in the table below. The outputs are primarily the control signals to the instruction register and the data register.

Table 13. TAP Controller Input/Outputs

Symbol	I/O	Function
TMS	I	Test Mode Select
TCK	I	Test Clock
PUR	I	Powerup Reset
$\overline{\text{PRGM}}$	I	BSCAN Reset
TRESET	O	Test Logic Reset
Select	O	Select IR (high); Select DR (low)
Enable	O	Test Data Out Enable
Capture-DR	O	Capture/Parallel Load DR
Capture-IR	O	Capture/Parallel Load IR
Shift-DR	O	Shift Data Register
Shift-DR	O	Shift Instruction Register
Update-DR	O	Update/Parallel Load DR
Update-IR	O	Update/Parallel Load IR

The TAPC generates control signals which allow capture, shift, and update operations on the instruction and data registers. In the capture operation, data is loaded into the register. In the shift operation, the captured data is shifted out while new data is shifted in. In the update operation, either the instruction register is loaded for instruction decode, or the boundary-scan register is updated for control of outputs.

The test host generates a test by providing input into the *ORCA* Series TMS input synchronous with TCK. This sequences the TAPC through states in order to perform the desired function on the instruction register or a data register. Figure 50 provides a diagram of the state transitions for the TAPC. The next state is determined by the TMS input value.

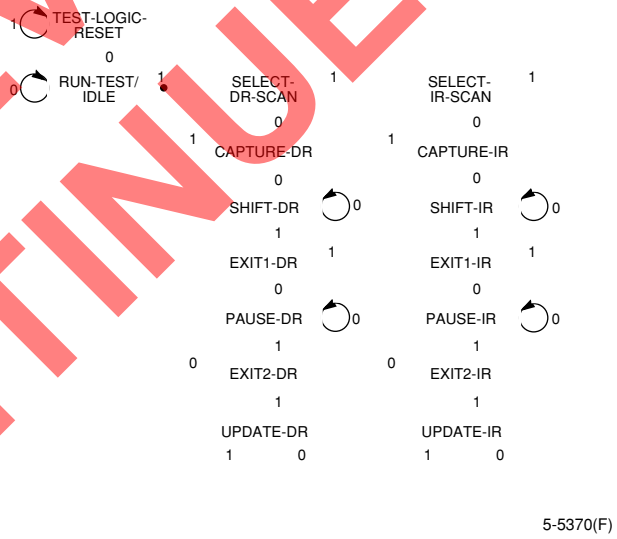

Figure 50. TAP Controller State Transition Diagram

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Special Function Blocks (continued)

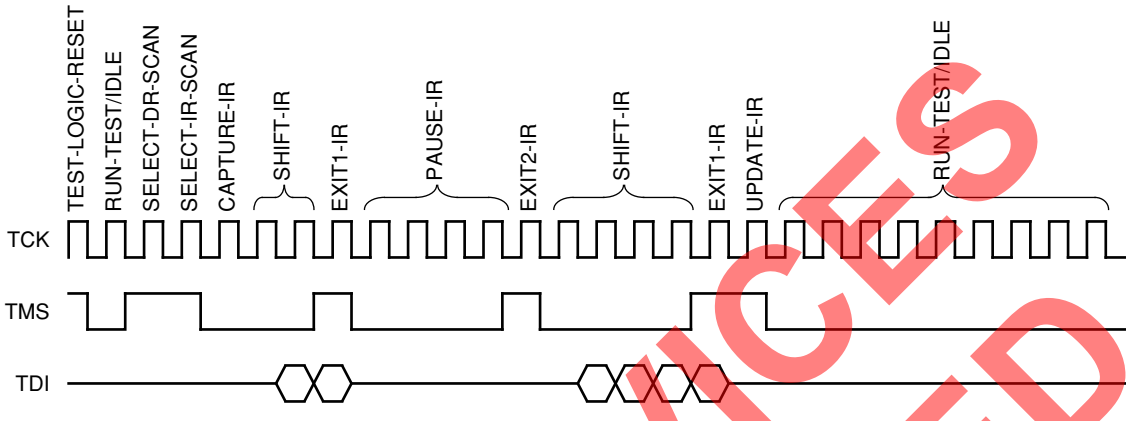

Fig.5.3(F)

Figure 52. Instruction Register Scan Timing Diagram

Boundary-Scan Timing

To ensure race-free operation, data changes on specific clock edges. The TMS and TDI inputs are clocked in on the rising edge of TCK, while changes on TDO occur on the falling edge of TCK. In the execution of an EXTEST instruction, parallel data is output from the BSR to the FPGA pads on the falling edge of TCK. The maximum frequency allowed for TCK is 10 MHz.

Figure 52 shows timing waveforms for an instruction scan operation. The diagram shows the use of TMS to sequence the TAPC through states. The test host (or BSM) changes data on the falling edge of TCK, and it is clocked into the DUT on the rising edge.

SELECT DEVICES DISCONTINUED

Estimating Power Dissipation (continued)

OR2C06A Clock Power

P = [0.63 mW/MHz
+ (0.25 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C06A clock power ≈ 5.3 mW/MHz.

OR2C08A Clock Power

P = [0.65 mW/MHz
+ (0.29 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C08A clock power ≈ 6.6 mW/MHz.

OR2C10A Clock Power

P = [0.66 mW/MHz
+ (0.32 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C10A clock power ≈ 8.6 mW/MHz.

OR2C12A Clock Power

P = [0.68 mW/MHz
+ (0.35 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C12A clock power ≈ 10.5 mW/MHz.

OR2C15A Clock Power

P = [0.69 mW/MHz
+ (0.38 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C15A clock power ≈ 12.7 mW/MHz.

OR2C26A Clock Power

P = [0.73 mW/MHz
+ (0.44 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C26A clock power ≈ 17.8 mW/MHz.

OR2C40A Clock Power

P = [0.77 mW/MHz
+ (0.53 mW/MHz – Branch) (# Branches)
+ (0.022 mW/MHz – PFU) (# PFUs)
+ (0.006 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2C40A clock power ≈ 26.6 mW/MHz.

The power dissipated in a PIC is the sum of the power dissipated in the four I/Os in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each I/O depends on whether it is configured as an input, output, or input/output. If an I/O is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

The power dissipated by a TTL input buffer is estimated as:

$$P_{TTL} = 2.2 \text{ mW} + 0.17 \text{ mW/MHz}$$

The power dissipated by an input buffer is estimated as:

$$P_{CMOS} = 0.17 \text{ mW/MHz}$$

The ac power dissipation from an output or bidirectional is estimated by the following:

$$P_{OUT} = (C_L + 8.8 \text{ pF}) \times V_{DD}^2 \times F \text{ Watts}$$

where the unit for C_L is farads, and the unit for F is Hz.

As an example of estimating power dissipation, suppose that a fully utilized OR2C15A has an average of three outputs for each of the 400 PFUs, that all 20 clock branches are used, that 150 of the 400 PFUs have FFs clocked at 40 MHz (16 of which are operating in a synchronous memory mode), and that the PFU outputs have an average activity factor of 20%.

Twenty TTL-configured inputs, 20 CMOS-configured inputs, 32 outputs driving 30 pF loads, and 16 bidirectional I/Os driving 50 pF loads are also generated from the 40 MHz clock with an average activity factor of 20%. The worst-case (V_{DD} = 5.25 V) power dissipation is estimated as follows:

P_{PFU} = 400 x 3 (0.16 mW/MHz x 20 MHz x 20%)
= 768 mW

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 21. OR2C/2T04A and OR2C06A 144-Pin TQFP Pinout (continued)

Pin	2C/2T04A Pad	2C06A Pad	Function	Pin	2C/2T04A Pad	2C06A Pad	Function
85	PR7A	PR8A	I/O-M3	115	PT9C	PT10D	I/O
86	PR7D	PR8D	I/O	116	PT9B	PT10C	I/O
87	VSS	VSS	VSS	117	PT9A	PT10A	I/O-D6
88	PR6A	PR7A	I/O	118	VDD	VDD	VDD
89	PR6C	PR7C	I/O	119	PT8D	PT9D	I/O
90	PR6D	PR7D	I/O	120	PT8A	PT9A	I/O-D5
91	VDD	VDD	VDD	121	PT7D	PT8D	I/O
92	PR5A	PR6A	I/O	122	PT7B	PT8B	I/O
93	PR5C	PR6C	I/O	123	PT7A	PT8A	I/O-D4
94	PR5D	PR6D	I/O	124	PT6D	PT7D	I/O
95	VSS	VSS	VSS	125	PT6C	PT7C	I/O
96	PR4A	PR5A	I/O-VDD5	126	PT6A	PT7A	I/O-D3
97	PR4C	PR5C	I/O	127	VSS	VSS	VSS
98	PR4D	PR5D	I/O	128	PT5D	PT6D	I/O
99	PR3A	PR4A	I/O-CS1	129	PT5C	PT6C	I/O
100	PR3D	PR4D	I/O	130	PT5A	PT6A	I/O-D2
101	PR2A	PR3A	I/O-$\overline{CS0}$	131	PT4D	PT5D	I/O-D1
102	PR2D	PR3D	I/O	132	PT4C	PT5C	I/O
103	PR1A	PR2A	I/O-$\overline{RD}$	133	PT4A	PT5A	I/O-D0/DIN
104	PR1B	PR2C	I/O	134	PT3D	PT4D	I/O
105	PR1C	PR2D	I/O	135	PT3A	PT4A	I/O-DOUT
106	PR1D	PR1A	I/O-$\overline{WR}$	136	VDD	VDD	VDD
107	VSS	VSS	VSS	137	PT2D	PT3D	I/O-VDD5
108	$\overline{RD\_CFG}$	$\overline{RD\_CFG}$	$\overline{RD\_CFG}$	138	PT2C	PT3C	I/O
109	VDD	VDD	VDD	139	PT2A	PT3A	I/O-TDI
110	VSS	VSS	VSS	140	PT1D	PT2A	I/O-TMS
111	PT10D	PT12D	I/O	141	PT1C	PT1D	I/O
112	PT10C	PT12A	I/O-RDY/RCLK	142	PT1A	PT1A	I/O-TCK
113	PT10B	PT11D	I/O	143	VSS	VSS	VSS
114	PT9D	PT11A	I/O-D7	144	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/TDO

Note: The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C/2T04A Pad	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
173	PT7D	PT8D	PT9D	PT10D	PT11D	PT12D	PT15D	PT18D	I/O
174	PT7C	PT8C	PT9C	PT10C	PT11C	PT12C	PT15A	PT18A	I/O
175	PT7B	PT8B	PT9B	PT10B	PT11B	PT12B	PT14D	PT17D	I/O
176	PT7A	PT8A	PT9A	PT10A	PT11A	PT12A	PT14A	PT17A	I/O-D4
177	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
178	PT6D	PT7D	PT8D	PT9D	PT10D	PT11D	PT13D	PT16D	I/O
179	PT6C	PT7C	PT8C	PT9C	PT10C	PT11C	PT13C	PT16C	I/O
180	PT6B	PT7B	PT8B	PT9B	PT10B	PT11B	PT13B	PT16B	I/O
181	PT6A	PT7A	PT8A	PT9A	PT10A	PT11A	PT13A	PT16A	I/O-D3
182	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
183	PT5D	PT6D	PT7D	PT8D	PT9D	PT10D	PT12D	PT15D	I/O
184	PT5C	PT6C	PT7C	PT8C	PT9C	PT10C	PT12C	PT15C	I/O
185	PT5B	PT6B	PT7B	PT8B	PT9B	PT10B	PT12B	PT15B	I/O-VDD5
186	PT5A	PT6A	PT7A	PT8A	PT9A	PT10A	PT12A	PT15A	I/O-D2
187	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
188	PT4D	PT5D	PT6D	PT7D	PT8D	PT9D	PT11D	PT14D	I/O-D1
189	PT4C	PT5C	PT6C	PT7C	PT8C	PT9C	PT11A	PT14A	I/O
190	PT4B	PT5B	PT6B	PT7B	PT8B	PT9B	PT10D	PT13D	I/O
191	PT4A	PT5A	PT6A	PT7A	PT8A	PT9A	PT10A	PT13A	I/O-D0/DIN
192	PT3D	PT4D	PT5D	PT6D	PT7D	PT8D	PT9D	PT12D	I/O
193	PT3C	PT4C	PT5C	PT6C	PT7C	PT8C	PT9A	PT12A	I/O
194	PT3B	PT4B	PT5B	PT6B	PT7B	PT8B	PT8D	PT11D	I/O
195	PT3A	PT4A	PT5A	PT6A	PT7A	PT8A	PT8A	PT11A	I/O-DOUT
196	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
197	PT2D	PT3D	PT4D	PT5D	PT6D	PT7D	PT7D	PT10D	I/O
198	PT2C	PT3C	PT4C	PT5A	PT6A	PT7A	PT7A	PT9A	I/O
199	PT2B	PT3B	PT4B	PT4D	PT5C	PT6C	PT6C	PT8A	I/O
200	PT2A	PT3A	PT4A	PT4A	PT5A	PT6A	PT6A	PT7A	I/O-TDI
201	See Note	PT2D	PT3D	PT3D	PT4A	PT5A	PT5A	PT6A	I/O
202	PT1D	PT2A	PT3A	PT3A	PT3A	PT4A	PT4A	PT5A	I/O-TMS
203	See Note	PT1D	PT2D	PT2D	PT2C	PT3A	PT3A	PT4A	I/O
204	PT1C	PT1C	PT2A	PT2A	PT2A	PT2A	PT2A	PT3A	I/O
205	PT1B	PT1B	PT1D	PT1D	PT1D	PT1D	PT1D	PT2D	I/O
206	PT1A	PT1A	PT1A	PT1A	PT1A	PT1A	PT1A	PT1A	I/O-TCK
207	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
208	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/ TDO	RD_DATA/TDO

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 24. OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 240-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
43	PL9A	PL10A	PL11A	PL12A	PL13A	PL17A	PL20A	I/O-A11
44	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
45	PL10D	PL11D	PL12D	PL13D	PL14D	PL18D	PL21D	I/O-A12
46	PL10C	PL11C	PL12C	PL13B	PL14B	PL18B	PL21B	I/O
47	PL10B	PL11B	PL12B	PL14D	PL15D	PL19D	PL22D	I/O
48	PL10A	PL11A	PL13D	PL14B	PL15B	PL19B	PL22B	I/O-A13
49	PL11D	PL12D	PL13B	PL14A	PL15A	PL19A	PL22A	I/O
50	PL11C	PL12C	PL13A	PL15D	PL16D	PL20D	PL23D	I/O
51	PL11B	PL12B	PL14D	PL15B	PL16B	PL20B	PL24D	I/O
52	PL11A	PL12A	PL14C	PL16D	PL17D	PL21D	PL25A	I/O-A14
53	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
54	PL12D	PL13D	PL15D	PL17D	PL18D	PL22D	PL27D	I/O
55	PL12C	PL13A	PL15A	PL17A	PL19D	PL23D	PL28D	I/O
56	PL12B	PL14D	PL16D	PL18C	PL19A	PL23A	PL28A	I/O
57	PL12A	PL14A	PL16A	PL18A	PL20A	PL24A	PL30A	I/O-A15
58	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
59	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
60	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
61	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
62	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
63	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	I/O-A16
64	PB1B	PB1D	PB1D	PB1D	PB2A	PB2A	PB3A	I/O
65	PB1C	PB2A	PB2A	PB2A	PB2D	PB2D	PB3D	I/O-VDD5
66	PB1D	PB2D	PB2D	PB2D	PB3D	PB3D	PB4D	I/O
67	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
68	PB2A	PB3A	PB3B	PB3D	PB4D	PB4D	PB5D	I/O-A17
69	PB2B	PB3B	PB4B	PB4D	PB5D	PB5D	PB6D	I/O
70	PB2C	PB3C	PB4C	PB5A	PB6A	PB6A	PB7A	I/O
71	PB2D	PB3D	PB4D	PB5B	PB6B	PB6B	PB7D	I/O
72	PB3A	PB4A	PB5A	PB5D	PB6D	PB6D	PB8D	I/O
73	PB3B	PB4B	PB5B	PB6A	PB7A	PB7A	PB9A	I/O
74	PB3C	PB4C	PB5C	PB6B	PB7B	PB7B	PB9D	I/O
75	PB3D	PB4D	PB5D	PB6D	PB7D	PB7D	PB10D	I/O
76	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
77	PB4A	PB5A	PB6A	PB7A	PB8A	PB8A	PB11A	I/O
78	PB4B	PB5B	PB6B	PB7B	PB8B	PB8D	PB11D	I/O
79	PB4C	PB5C	PB6C	PB7C	PB8C	PB9A	PB12A	I/O
80	PB4D	PB5D	PB6D	PB7D	PB8D	PB9D	PB12D	I/O
81	PB5A	PB6A	PB7A	PB8A	PB9A	PB10A	PB13A	I/O
82	PB5B	PB6B	PB7B	PB8B	PB9B	PB10D	PB13D	I/O
83	PB5C	PB6C	PB7C	PB8C	PB9C	PB11A	PB14A	I/O
84	PB5D	PB6D	PB7D	PB8D	PB9D	PB11D	PB14D	I/O

Notes:
The OR2C/2T08A and OR2C/2T10A do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 25. OR2C06A, OR2T08A, OR2C/2T10A, OR2C12A, and OR2C/2T15A/B 256-Pin PBGA Pinout (continued)

Pin	2C06A Pad	2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	Function
P3	PL10D	PL11D	PL12D	PL13D	PL14D	I/O-A12
R2	PL10C	PL11C	PL12C	PL13B	PL14B	I/O
T1	PL10B	PL11B	PL12B	PL14D	PL15D	I/O
P4	PL10A	PL11A	PL13D	PL14B	PL15B	I/O-A13
R3	PL11D	PL12D	PL13B	PL14A	PL15A	I/O
T2	PL11C	PL12C	PL13A	PL15D	PL16D	I/O
U1	PL11B	PL12B	PL14D	PL15B	PL16B	I/O
T3	PL11A	PL12A	PL14C	PL16D	PL17D	I/O-A14
U2	—	PL13D	PL15D	PL17D	PL18D	I/O-VDD5
V1	PL12D	PL13C	PL15C	PL17C	PL18C	I/O
T4	PL12C	PL13B	PL15B	PL17B	PL18A	I/O
U3	PL12B	PL13A	PL15A	PL17A	PL19D	I/O
V2	—	PL14D	PL16D	PL18D	PL19C	I/O
W1	—	PL14C	PL16C	PL18C	PL19A	I/O
V3	—	PL14B	PL16B	PL18B	PL20D	I/O
W2	PL12A	PL14A	PL16A	PL18A	PL20A	I/O-A15
Y1	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
Y2	PB1A	PB1A	PB1A	PB1A	PB1A	I/O-A16
W4	—	PB1C	PB1C	PB1C	PB1D	I/O
V4	PB1B	PB1D	PB1D	PB1D	PB2A	I/O
U5	PB1C	PB2A	PB2A	PB2A	PB2D	I/O-VDD5
Y3	PB1D	PB2B	PB2B	PB2B	PB3A	I/O
Y4	—	PB2C	PB2C	PB2C	PB3C	I/O
V5	—	PB2D	PB2D	PB2D	PB3D	I/O
W5	PB2A	PB3A	PB3B	PB3D	PB4D	I/O-A17
Y5	PB2B	PB3B	PB4B	PB4D	PB5D	I/O
V6	PB2C	PB3C	PB4C	PB5A	PB6A	I/O
U7	PB2D	PB3D	PB4D	PB5B	PB6B	I/O
W6	PB3A	PB4A	PB5A	PB5D	PB6D	I/O
Y6	PB3B	PB4B	PB5B	PB6A	PB7A	I/O
V7	PB3C	PB4C	PB5C	PB6B	PB7B	I/O
W7	PB3D	PB4D	PB5D	PB6D	PB7D	I/O
Y7	PB4A	PB5A	PB6A	PB7A	PB8A	I/O
V8	PB4B	PB5B	PB6B	PB7B	PB8B	I/O
W8	PB4C	PB5C	PB6C	PB7C	PB8C	I/O
Y8	PB4D	PB5D	PB6D	PB7D	PB8D	I/O
U9	PB5A	PB6A	PB7A	PB8A	PB9A	I/O
V9	PB5B	PB6B	PB7B	PB8B	PB9B	I/O
W9	PB5C	PB6C	PB7C	PB8C	PB9C	I/O
Y9	PB5D	PB6D	PB7D	PB8D	PB9D	I/O

Notes:
The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The OR2C/2T08A do not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 4 x 4 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
AC25	PR16B	PR18B	PR20C	PR24C	PR29A	I/O
AC24	PR16C	PR18C	PR20D	PR24D	PR29D	I/O
AC26	PR16D	PR18D	PR19A	PR23A	PR28A	I/O
AB25	PR15A	PR17A	PR19D	PR23D	PR28D	I/O
AB23	PR15B	PR17B	PR18A	PR22A	PR27A	I/O
AB24	PR15C	PR17C	PR18B	PR22B	PR27B	I/O
AB26	PR15D	PR17D	PR18D	PR22D	PR27D	I/O
AA25	PR14A	PR16A	PR17A	PR21A	PR26A	I/O
Y23	PR14B	PR16B	PR17B	PR21B	PR26B	I/O
AA24	PR14C	PR16C	PR17C	PR21C	PR26C	I/O
AA26	—	PR16D	PR17D	PR21D	PR25A	I/O
Y25	PR14D	PR15A	PR16A	PR20A	PR24A	I/O
Y26	—	PR15B	PR16B	PR20B	PR24B	I/O
Y24	PR13A	PR15C	PR16C	PR20C	PR24D	I/O
W25	PR13B	PR15D	PR16D	PR20D	PR23D	I/O-M1
V23	PR13C	PR14A	PR15A	PR19A	PR22A	I/O
W26	—	PR14B	PR15B	PR19B	PR22B	I/O
W24	PR13D	PR14C	PR15C	PR19C	PR22C	I/O
V25	PR12A	PR14D	PR15D	PR19D	VDD5	I/O-VDD5
V26	PR12B	PR13A	PR14A	PR18A	PR21A	I/O
U25	—	PR13B	PR14B	PR18B	PR21B	I/O
V24	PR12C	PR13C	PR14C	PR18C	PR21C	I/O
U26	PR12D	PR13D	PR14D	PR18D	PR21D	I/O
U23	PR11A	PR12A	PR13A	PR17A	PR20A	I/O-M2
T25	PR11B	PR12B	PR13B	PR17D	PR20D	I/O
U24	PR11C	PR12C	PR13C	PR16A	PR19A	I/O
T26	PR11D	PR12D	PR13D	PR16D	PR19D	I/O
R25	PR10A	PR11A	PR12A	PR15A	PR18A	I/O-M3
R26	PR10B	PR11B	PR12B	PR15D	PR18D	I/O
T24	PR10C	PR11C	PR12C	PR14A	PR17A	I/O
P25	PR10D	PR11D	PR12D	PR14D	PR17D	I/O
R23	PR9A	PR10A	PR11A	PR13A	PR16A	I/O
P26	PR9B	PR10B	PR11B	PR13B	PR16B	I/O
R24	PR9C	PR10C	PR11C	PR13C	PR16C	I/O
N25	PR9D	PR10D	PR11D	PR13D	PR16D	I/O
N23	PR8A	PR9A	PR10A	PR12A	PR15A	I/O
N26	PR8B	PR9B	PR10B	PR12B	PR15B	I/O
P24	PR8C	PR9C	PR10C	PR12C	PR15C	I/O
M25	PR8D	PR9D	PR10D	PR12D	PR15D	I/O

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

SELECT DEVICES DISCONTINUED

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
AC4	VSS	VSS	VSS	VSS	VSS	VSS
AC8	VSS	VSS	VSS	VSS	VSS	VSS
AD24	VSS	VSS	VSS	VSS	VSS	VSS
AD3	VSS	VSS	VSS	VSS	VSS	VSS
AE1	VSS	VSS	VSS	VSS	VSS	VSS
AE2	VSS	VSS	VSS	VSS	VSS	VSS
AE25	VSS	VSS	VSS	VSS	VSS	VSS
AF1	VSS	VSS	VSS	VSS	VSS	VSS
AF25	VSS	VSS	VSS	VSS	VSS	VSS
AF26	VSS	VSS	VSS	VSS	VSS	VSS
B2	VSS	VSS	VSS	VSS	VSS	VSS
B25	VSS	VSS	VSS	VSS	VSS	VSS
B26	VSS	VSS	VSS	VSS	VSS	VSS
C24	VSS	VSS	VSS	VSS	VSS	VSS
C3	VSS	VSS	VSS	VSS	VSS	VSS
D14	VSS	VSS	VSS	VSS	VSS	VSS
D19	VSS	VSS	VSS	VSS	VSS	VSS
D23	VSS	VSS	VSS	VSS	VSS	VSS
D4	VSS	VSS	VSS	VSS	VSS	VSS
D9	VSS	VSS	VSS	VSS	VSS	VSS
H4	VSS	VSS	VSS	VSS	VSS	VSS
J23	VSS	VSS	VSS	VSS	VSS	VSS
N4	VSS	VSS	VSS	VSS	VSS	VSS
P23	VSS	VSS	VSS	VSS	VSS	VSS
V4	VSS	VSS	VSS	VSS	VSS	VSS
W23	VSS	VSS	VSS	VSS	VSS	VSS
AA23	VDD	VDD	VDD	VDD	VDD	VDD
AA4	VDD	VDD	VDD	VDD	VDD	VDD
AC11	VDD	VDD	VDD	VDD	VDD	VDD
AC16	VDD	VDD	VDD	VDD	VDD	VDD
AC21	VDD	VDD	VDD	VDD	VDD	VDD
AC6	VDD	VDD	VDD	VDD	VDD	VDD
D11	VDD	VDD	VDD	VDD	VDD	VDD
D16	VDD	VDD	VDD	VDD	VDD	VDD
D21	VDD	VDD	VDD	VDD	VDD	VDD
D6	VDD	VDD	VDD	VDD	VDD	VDD
F23	VDD	VDD	VDD	VDD	VDD	VDD
F4	VDD	VDD	VDD	VDD	VDD	VDD
L23	VDD	VDD	VDD	VDD	VDD	VDD

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

SELECT DEVICES DISCONTINUED

Timing Characteristics (continued)

Table 36A. OR2CxxA and OR2TxxA Asynchronous Memory Write Characteristics (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C. OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation (TJ = 85 °C, VDD = min):												
Write Cycle Time	TWC	7.8	—	6.3	—	5.7	—	5.2	—	5.1	—	ns
Write Enable (WREN) Pulse Width (A4/B4)	TPW	2.5	—	2.0	—	1.8	—	1.7	—	1.6	—	ns
Setup Time (TJ = 85 °C, VDD = min):												
Address to WREN (A[3:0]/B[3:0] to A4/B4)	MEM*_AWRSET	0.1	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Data to WREN (WD[3:0] to A4/B4)	MEM*_DWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Address to WPE (A[3:0]/B[3:0] to C0)	MEM*_APWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Data to WPE (WD[3:0] to C0)	MEM*_DPWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
WPE to WREN (C0 to A4/B4)	MEM*_WPESET	2.0	—	1.5	—	1.4	—	1.1	—	1.1	—	ns
Hold Time (TJ = all, VDD = all):												
Address from WREN (A[3:0]/B[3:0] from A4/B4)	MEM*_WRAHLD	1.7	—	1.8	—	1.6	—	1.6	—	1.5	—	ns
Data from WREN (WD[3:0] from A4/B4)	MEM*_WRDHLD	2.0	—	1.9	—	1.5	—	1.6	—	1.6	—	ns
Address from WPE (A[3:0/B[3:0] to C0)	MEM*_PWRAHLD	3.3	—	2.8	—	2.5	—	2.4	—	2.3	—	ns
Data from WPE (WD[3:0] to C0)	MEM*_PWRDHLD	3.4	—	2.9	—	2.6	—	2.4	—	2.3	—	ns
WPE from WREN (C0 from A4/B4)	MEM*_WPEHLD	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns

Table 36B. OR2TxxB Asynchronous Memory Write Characteristics (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Write Operation (TJ = 85 °C, VDD = min):						
Write Cycle Time	TWC	5.1	—	4.2	—	ns
Write Enable (WREN) Pulse Width (A4/B4)	TPW	1.7	—	1.4	—	ns
Setup Time (TJ = 85 °C, VDD = min):						
Address to WREN (A[3:0]/B[3:0] to A4/B4)	MEM*_AWRSET	0.0	—	0.0	—	ns
Data to WREN (WD[3:0] to A4/B4)	MEM*_DWRSET	0.0	—	0.0	—	ns
Address to WPE (A[3:0]/B[3:0] to C0)	MEM*_APWRSET	0.0	—	0.0	—	ns
Data to WPE (WD[3:0] to C0)	MEM*_DPWRSET	0.0	—	0.0	—	ns
WPE to WREN (C0 to A4/B4)	MEM*_WPESET	1.0	—	0.8	—	ns
Hold Time (TJ = all, VDD = all):						
Address from WREN (A[3:0]/B[3:0] from A4/B4)	MEM*_WRAHLD	0.9	—	0.7	—	ns
Data from WREN (WD[3:0] from A4/B4)	MEM*_WRDHLD	1.6	—	1.3	—	ns
Address from WPE (A[3:0/B[3:0] to C0)	MEM*_PWRAHLD	2.3	—	1.9	—	ns
Data from WPE (WD[3:0] to C0)	MEM*_PWRDHLD	2.3	—	1.9	—	ns
WPE from WREN (C0 from A4/B4)	MEM*_WPEHLD	0.0	—	0.0	—	ns

SELECT DEVICES DISCONTINUED

Timing Characteristics (continued)

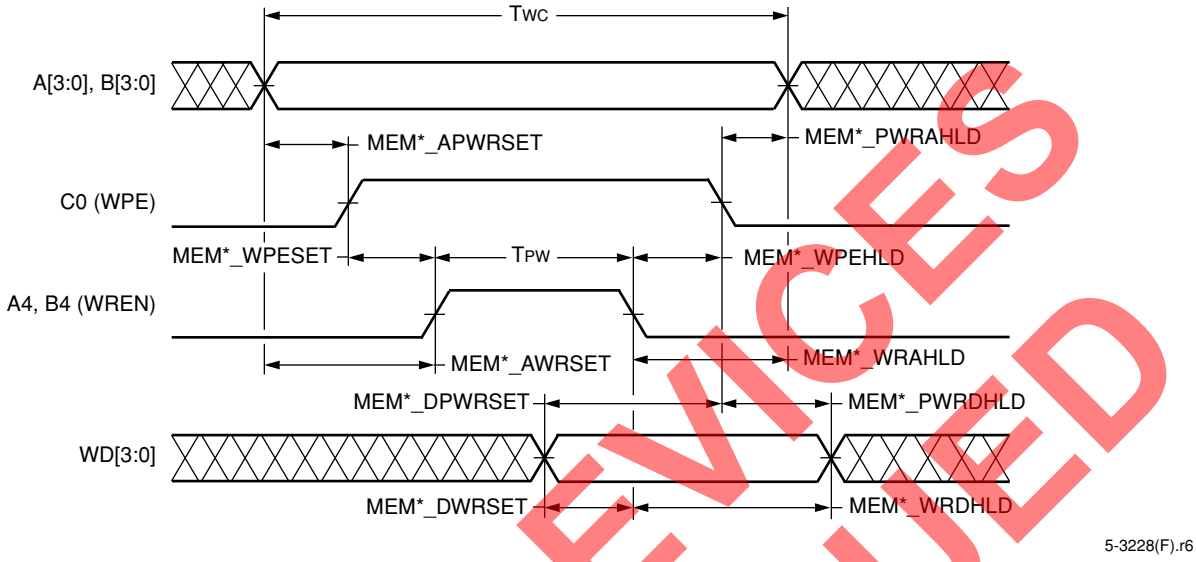

Figure 57. Write Operation

SELECT DEVICES DISCONTINUED

Timing Characteristics (continued)

Table 46B. OR2TxxB Programmable I/O Cell Timing Characteristics

OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Inputs (TJ = 85 °C, VDD = min)						
Input Rise Time	TR	—	500	—	500	ns
Input Fall Time	TF	—	500	—	500	ns
Pad to In Delay	PAD_IN_DEL	—	1.1	—	1.0	ns
Pad to Nearest PFU Latch Output	CHIP_LATCH	—	3.3	—	2.4	ns
Delay Added to General Routing (input buffer in delay mode for OR2T15B and smaller devices)	—	—	6.6	—	6.1	ns
Delay Added to General Routing (input buffer in delay mode for OR2T40B)	—	—	8.9	—	8.2	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2T15B and smaller devices)	—	—	6.4	—	6.0	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2T40B)	—	—	8.7	—	8.0	ns
Outputs (TJ = 85 °C, VDD = min, CL = 50 pF)						
PFU CK to Pad Delay (DOUT[3:0] to PAD):						
Fast	DOUT_DEL(F)	—	2.8	—	2.5	ns
Slewlim	DOUT_DEL(SL)	—	3.6	—	3.3	ns
Sinklim	DOUT_DEL(SI)	—	8.3	—	8.0	ns
Output to Pad Delay (OUT[3:0] to PAD):						
Fast	OUT_DEL(F)	—	2.8	—	2.5	ns
Slewlim	OUT_DEL(SL)	—	3.6	—	3.3	ns
Sinklim	OUT_DEL(SI)	—	8.3	—	8.0	ns
3-state Enable Delay (TS[3:0] to PAD):						
Fast	TS_DEL(F)	—	3.0	—	2.7	ns
Slewlim	TS_DEL(SL)	—	3.8	—	3.4	ns
Sinklim	TS_DEL(SI)	—	9.1	—	8.7	ns

Notes:
If the input buffer is placed in delay mode, the chip hold time to the nearest PFU latch is guaranteed to be 0 if the clock is routed using the primary clock network; (TJ = all, VDD = all). It should also be noted that any signals routed on the clock lines or using the TRIDI buffers directly from the input buffer do not get delayed at any time.

The delays for all input buffers assume an input rise/fall time of ≤1 V/ns.

SELECT DEVICES DISCONTINUED

Timing Characteristics (continued)

Table 55. Series 2 Boundary-Scan Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.
OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Min	Max	Unit
TDI/TMS to TCK Setup Time	TS	25	—	ns
TDI/TMS Hold Time from TCK	TH	0	—	ns
TCK Low Time	TCL	50	—	ns
TCK High Time	TCH	50	—	ns
TCK to TDO Delay	TD	—	20	ns
TCK Frequency	TTCK	—	10	MHz

BSTD(F).2c.r3

Figure 73. Boundary-Scan Timing Diagram

SELECT DEVICES DISCONTINUED

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2T40B	OR2T40B8PS208-DB[2]	8	SQFP2	208	C	DB
	OR2T40B8BA352-DB[2]	8	PBGA	352	C	DB
	OR2T40B8BC432-DB[2]	8	EBGA	432	C	DB
	OR2T40B7PS208-DB[2]	7	SQFP2	208	C	DB
	OR2T40B7BA352-DB[2]	7	PBGA	352	C	DB
	OR2T40B7BC432-DB[2]	7	EBGA	432	C	DB

Industrial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2C04A	OR2C04A3T100I-DB[2]	3	TQFP	100	I	DB
	OR2C04A3T144I-DB[2]	3	TQFP	144	I	DB
	OR2C04A3S208I-DB[2]	3	SQFP	208	I	DB
OR2C06A	OR2C06A3T100I-DB[2]	3	TQFP	100	I	DB
	OR2C06A3T144I-DB[2]	3	TQFP	144	I	DB
	OR2C06A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C06A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C06A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C06A3BA256I-DB[2]	3	PBGA	256	I	DB
OR2C08A	OR2C08A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C08A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C08A3S240I-DB[2]	3	SQFP	240	I	DB
OR2C10A	OR2C10A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C10A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C10A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C10A3BA352I-DB[2]	3	QFP	352	I	DB
OR2C12A	OR2C12A3M84I-D[2]	3	SQFP	84	I	D
	OR2C12A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C12A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C12A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C12A3S304I-DB[2]	3	SPBGA	304	I	DB
	OR2C12A3BA352I-DB[2]	3	PLCC	352	I	DB
OR2C15A	OR2C15A3M84I-D[2]	3	PLCC	84	I	D
	OR2C15A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C15A3PS208I-DB[2]	3	SQFP2	208	I	DB
	OR2C15A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C15A3PS240I-DB[2]	3	SQFP2	240	I	DB
	OR2C15A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C15A3BA352I-DB[2]	3	PBGA	352	I	DB

SELECT DEVICES DISCONTINUED