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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1600
Total RAM Bits	25600
Number of I/O	171
Number of Gates	44200
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or2t15a6s208-db

Description (continued)

The FPGA's functionality is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM, EPROM, or ROM on the circuit board, or any other storage media. Serial ROMs provide a simple, low pin count method for configuring FPGAs, while the peripheral and JTAG configuration modes allow for easy, in-system programming (ISP).

5-6779(F)

Figure 1. Series 2 Array

Programmable Logic Cells (continued)

PLC Routing Resources

Generally, the ispLEVER development system is used to automatically route interconnections. Interactive routing with the ispLEVER design editor (EPIC) is also available for design optimization. To use EPIC for interactive layout, an understanding of the routing resources is needed and is provided in this section.

The routing resources consist of switching circuitry and metal interconnect segments. Generally, the metal lines which carry the signals are designated as routing nodes (lines). The switching circuitry connects the routing nodes, providing one or more of three basic functions: signal switching, amplification, and isolation. A net running from a PFU or PIC output (source) to a PLC or PIC input (destination) consists of one or more lines, connected by switching circuitry designated as configurable interconnect points (CIPs).

The following sections discuss PLC, PIC, and interquad routing resources. This section discusses the PLC switching circuitry, intra-PLC routing, inter-PLC routing, and clock distribution.

Configurable Interconnect Points

The process of connecting lines uses three basic types of switching circuits: two types of configurable interconnect points (CIPs) and bidirectional buffers (BIDIs). The basic element in CIPs is one or more pass transistors, each controlled by a configuration RAM bit. The two types of CIPs are the mutually exclusive (or multiplexed) CIP and the independent CIP.

A mutually exclusive set of CIPs contains two or more CIPs, only one of which can be on at a time. An independent CIP has no such restrictions and can be on independent of the state of other CIPs. Figure 19 shows an example of both types of CIPs.

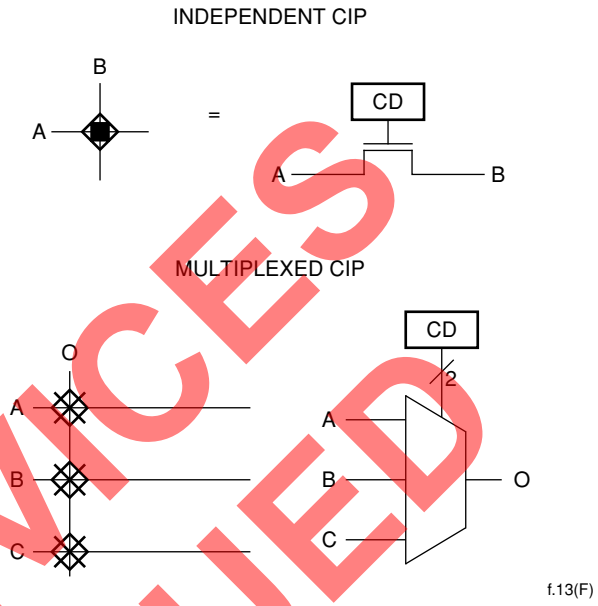


Figure 19. Configurable Interconnect Point

3-Statable Bidirectional Buffers

Bidirectional buffers provide isolation as well as amplification for signals routed a long distance. Bidirectional buffers are also used to drive signals directly onto either vertical or horizontal XL and XH lines (to be described later in the inter-PLC routing section). BIDIs are also used to indirectly route signals through the switching lines. Any number from zero to eight BIDIs can be used in a given PLC.

The BIDIs in a PLC are divided into two nibble-wide sets of four (BIDI and BIDIH). Each of these sets has a separate BIDI controller that can have an application net connected to its TRI input, which is used to 3-state enable the BIDIs. Although only one application net can be connected to both BIDI controllers, the sense of this signal (active-high, active-low, or ignored) can be configured independently. Therefore, one set can be used for driving signals, the other set can be used to create 3-state buses, both sets can be used for 3-state buses, and so forth.

Programmable Logic Cells (continued)

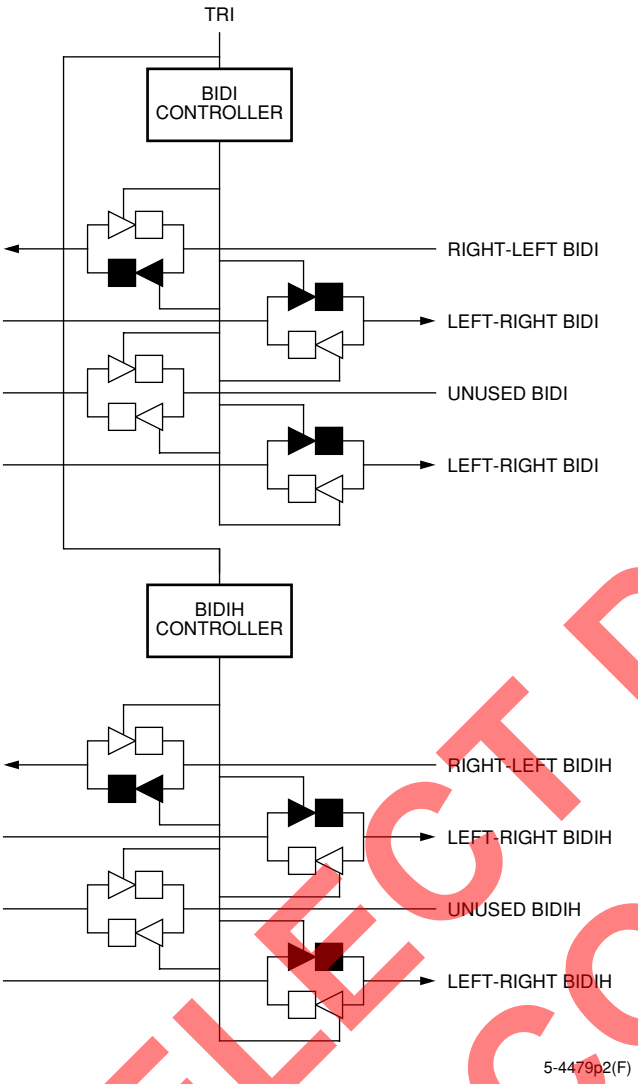


Figure 20. 3-Statable Bidirectional Buffers

Intra-PLC Routing

The function of the intra-PLC routing resources is to connect the PFU's input and output ports to the routing resources used for entry to and exit from the PLC. These are nets for providing PFU feedback, turning corners, or switching from one type of routing resource to another.

PFU Input and Output Ports. There are 19 input ports to each PFU. The PFU input ports are labeled A[4:0], B[4:0], WD[3:0], C0, CK, LSR, CIN, and CE. The six output ports are O[4:0] and COUT. These ports correspond to those described in the PFU section.

Switching Lines. There are four sets of switching lines in each PLC, one in each corner. Each set consists of five switching elements, labeled SUL[4:0], SUR[4:0], SLL[4:0], and SLR[4:0], for the upper-left, upper-right, lower-left, and lower-right sections of the PFUs, respectively. The switching lines connect to the PFU inputs and outputs as well as the BIDI and BIDIH lines, to be described later. They also connect to both the horizontal and vertical X1 and X4 lines (inter-PLC routing resources, described below) in their specific corner.

One of the four sets of switching lines can be connected to a set of switching lines in each of the four adjacent PLCs or PICs. This allows direct routing of up to five signals without using inter-PLC routing.

BIDI/BIDIH Lines. There are two sets of bidirectional lines in the PLC, each set consisting of four bidirectional buffers. They are designated BIDI and BIDIH and have similar functionality. The BIDI lines are used in conjunction with the XL lines, and the BIDIH lines are used in conjunction with the XH lines. Each side of the four BIDIs in the PLC is connected to a BIDI line on the left (BL[3:0]) and on the right (BR[3:0]). These lines can be connected to the XL lines through CIPs, with BL[3:0] connected to the vertical XL lines and BR[3:0] connected to the horizontal XL lines. Both BL[3:0] and BR[3:0] have CIPs which connect to the switching lines.

Similarly, each side of the four BIDIHs is connected to a BIDIH line: BLH[3:0] on the left and BRH[3:0] on the right. These lines can also be connected to the XH lines through CIPs, with BLH[3:0] connected to the vertical XH lines and BRH[3:0] connected to the horizontal XH lines. Both BLH[3:0] and BRH[3:0] have CIPs which connect to the switching lines.

CIPs are also provided to connect the BIDIH and BIDIL lines together on each side of the BIDIs. For example, BLH3 can connect to BL3, while BRH3 can connect to BR3.

Programmable Logic Cells (continued)

Inter-PLC Routing Resources

The inter-PLC routing is used to route signals between PLCs. The lines occur in groups of four, and differ in the numbers of PLCs spanned. The X1 lines span one PLC, the X4 lines span four PLCs, the XH lines span one-half the width (height) of the PLC array, and the XL lines span the width (height) of the PLC array. All types of lines run in both horizontal and vertical directions.

Table 5 shows the groups of inter-PLC lines in each PLC. In the table, there are two rows/columns each for X1 and X4 lines. In the design editor, the horizontal X1 and X4 lines are located above and below the PFU. Similarly, the vertical segments are located on each side. The XL and XH lines only run below and to the left of the PFU. The indexes specify individual lines within a group. For example, the VX4[2] line runs vertically to the left of the PFU, spans four PLCs, and is the third line in the 4-bit wide bus.

Table 5. Inter-PLC Routing Resources

Horizontal Lines	Vertical Lines	Distance Spanned
HX1[3:0]	VX1[3:0]	One PLC
HX1[7:4]	VX1[7:4]	One PLC
HX4[3:0]	VX4[3:0]	Four PLCs
HX4[7:4]	VX4[7:4]	Four PLCs
HXL[3:0]	VXL[3:0]	PLC Array
HXH[3:0]	VXH[3:0]	1/2 PLC Array
CKL, CKR	CKT, CKB	PLC Array

Figure 21 shows the inter-PLC routing within one PLC. Figure 22 provides a global view of inter-PLC routing resources across multiple PLCs.

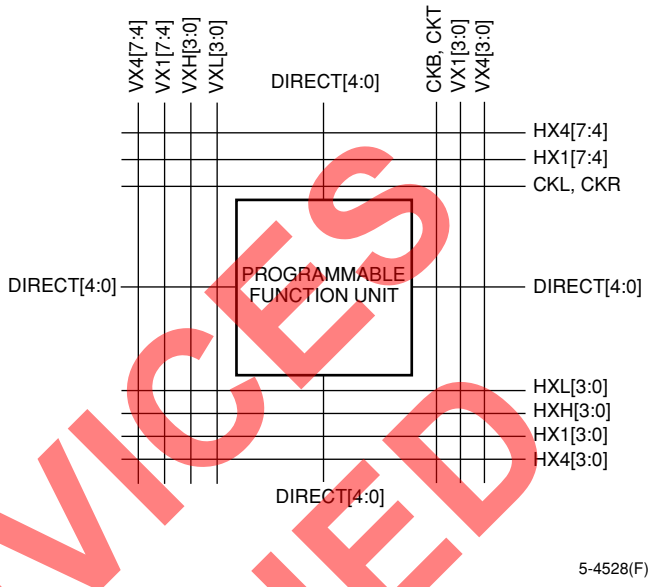


Figure 21. Single PLC View of Inter-PLC Lines

X1 Lines. There are a total of 16 X1 lines per PLC: eight vertical and eight horizontal. Each of these is subdivided into nibble-wide buses: HX1[3:0], HX1[7:4], VX1[3:0], and VX1[7:4]. An X1 line is one PLC long. If a net is longer than one PLC, an X1 line can be lengthened to n times its length by turning on n – 1 CIPs. A signal is routed onto an X1 line via the switching lines.

X4 Lines. There are four sets of four X4 lines, for a total of 16 X4 lines per PLC. They are HX4[3:0], HX4[7:4], VX4[3:0], and VX4[7:4]. Each set of X4 lines is twisted each time it passes through a PLC, and one of the four is broken with a CIP. This allows a signal to be routed for a length of four cells in any direction on a single line without additional CIPs. The X4 lines can be used to route any nets that require minimum delay. A longer net is routed by connecting two X4 lines together by a CIP. The X4 lines are accessed via the switching lines.

Programmable Logic Cells (continued)

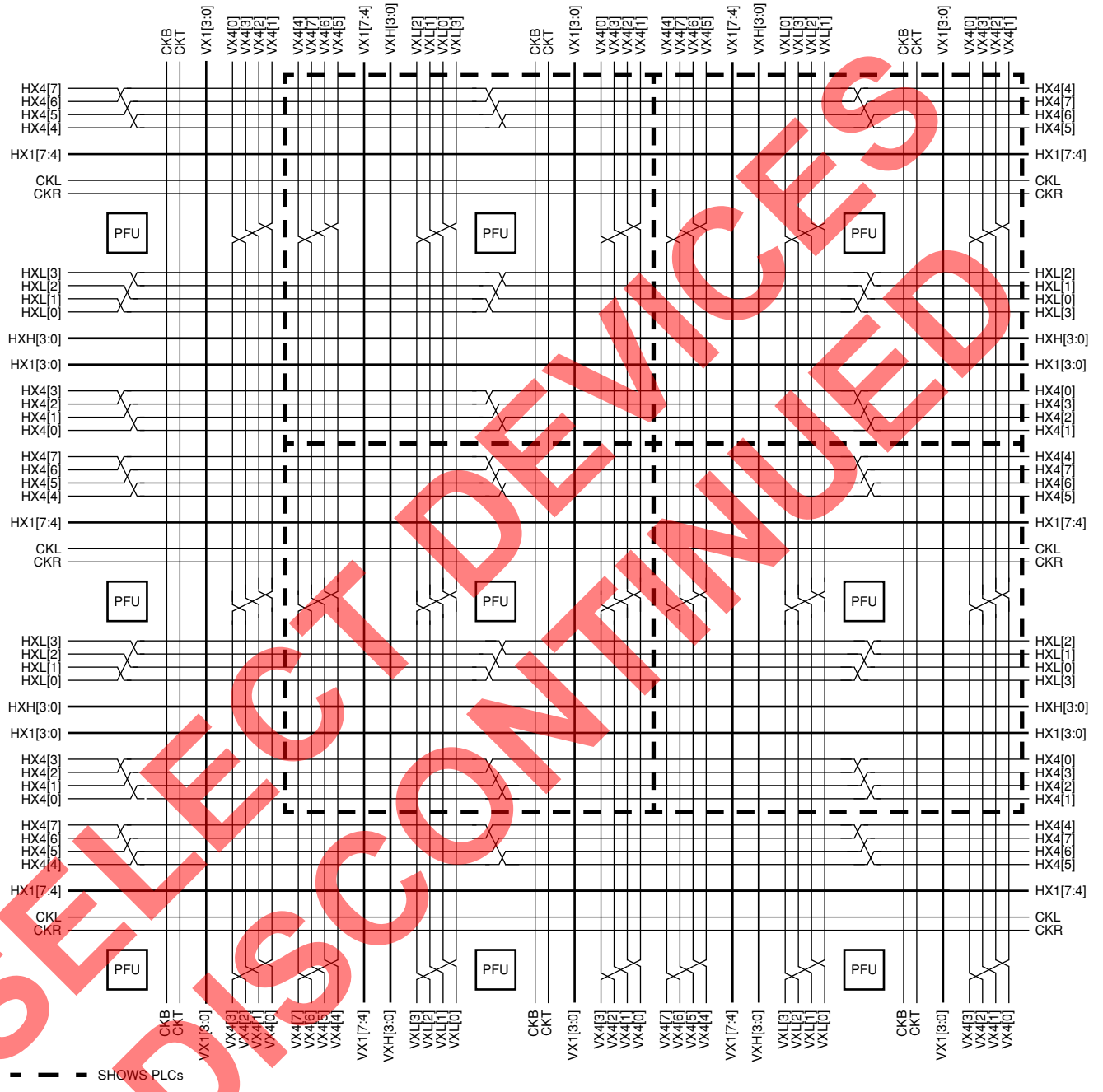


Figure 22. Multiple PLC View of Inter-PLC Routing

Programmable Input/Output Cells

(continued)

PIC Routing Resources

The PIC routing is designed to route 4-bit wide buses efficiently. For example, any four consecutive I/O pads can have both their input and output signals routed into one PLC. Using only PIC routing, either the input or output data can be routed to/from a single PLC from/to any eight pads in a row, as in Figure 25.

The connections between PLCs and the I/O pad are provided by two basic types of routing resources. These are routing resources internal to the PIC and routing resources used for PIC-PLC connection. Figure 26 and Figure 27 show a high-level and detailed view of these routing resources, respectively.

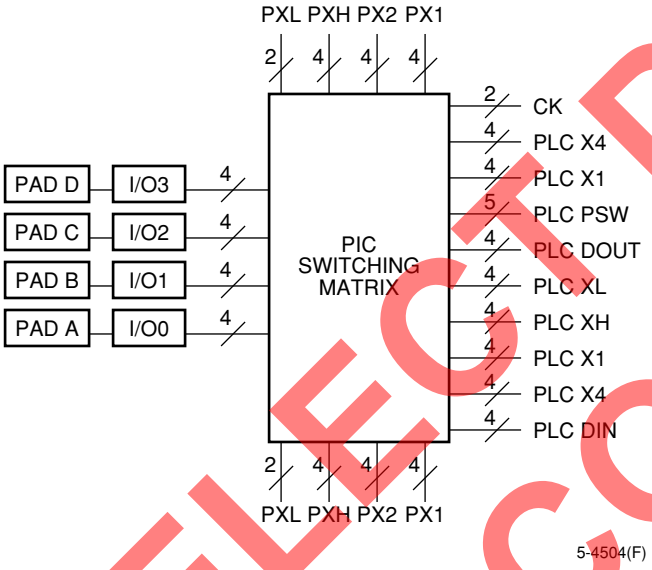


Figure 25. Simplified PIC Routing Diagram

The PIC's name is represented by a two-letter designation to indicate on which side of the device it is located followed by a number to indicate in which row or column it is located. The first letter, P, designates that the cell is a PIC and not a PLC. The second letter indicates the side of the array where the PIC is located. The four sides are left (L), right (R), top (T), and bottom (B). The individual I/O pad is indicated by a single letter (either A, B, C, or D) placed at the end of the PIC name. As an example, PL10A indicates a pad located on the left side of the array in the tenth row.

Each PIC has four pads and each pad can be configured as an input, an output (3-statable), a direct output, or a bidirectional I/O. When the pads are used as inputs, the external signals are provided to the internal circuitry at IN[3:0]. When the pads are used to provide direct inputs to the latches/FFs, they are connected through DIN[3:0]. When the pads are used as outputs, the internal signals connect to the pads through OUT[3:0]. When the pads are used as direct outputs, the output from the latches/flip-flops in the PLCs to the PIC is designated DOUT[3:0]. When the outputs are 3-statable, the 3-state enable signals are TS[3:0].

Routing Resources Internal to the PIC

For inter-PIC routing, the PIC contains 14 lines used to route signals around the perimeter of the FPGA. Figure 25 shows these lines running vertically for a PIC located on the left side. Figure 26 shows the lines running horizontally for a PIC located at the top of the FPGA.

PXL Lines. Each PIC has two PXL lines, labeled PXL[1:0]. Like the XL lines of the PLC, the PXL lines span the entire edge of the FPGA.

PXH Lines. Each PIC has four PXH lines, labeled PXH[3:0]. Like the XH lines of the PLC, the PXH lines span half the edge of the FPGA.

PX2 Lines. There are four PX2 lines in each PIC, labeled PX2[3:0]. The PX2 lines pass through two adjacent PICs before being broken. These are used to route nets around the perimeter equally a distance of two or more PICs.

PX1 Lines. Each PIC has four PX1 lines, labeled PX1[3:0]. The PX1 lines are one PIC long and are extended to adjacent PICs by enabling CIPs.

FPGA Configuration Modes (continued)

Asynchronous Peripheral Mode

Figure 42 shows the connections needed for the asynchronous peripheral mode. In this mode, the FPGA system interface is similar to that of a microprocessor-peripheral interface. The microprocessor generates the control signals to write an 8-bit byte into the FPGA. The FPGA control inputs include active-low $\overline{CS0}$ and active-high CS1 chip selects, a write $\overline{WR}$ input, and a read $\overline{RD}$ input. The chip selects can be cycled or maintained at a static level during the configuration cycle. Each byte of data is written into the FPGA's D[7:0] input pins.

The FPGA provides a RDY status output to indicate that another byte can be loaded. A low on RDY indicates that the double-buffered hold/shift registers are not ready to receive data, and this pin must be monitored to go high before another byte of data can be written. The shortest time RDY is low occurs when a byte is loaded into the hold register and the shift register is empty, in which case the byte is immediately transferred to the shift register. The longest time for RDY to remain low occurs when a byte is loaded into the holding register and the shift register has just started shifting configuration data into configuration RAM.

The RDY status is also available on the D7 pin by enabling the chip selects, setting $\overline{WR}$ high, and applying $\overline{RD}$ low, where the $\overline{RD}$ input is an output enable for the D7 pin when $\overline{RD}$ is low. The D[6:0] pins are not enabled to drive when $\overline{RD}$ is low and, thus, only act as input pins in asynchronous peripheral mode.

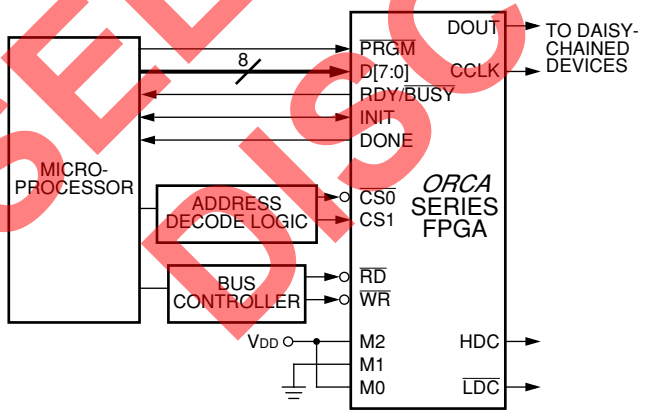


Figure 42. Asynchronous Peripheral Configuration Schematic

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after $\overline{INIT}$ goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The RDY signal is an output which acts as an acknowledge. RDY goes high one CCLK after data is clocked and, after one CCLK cycle, returns low. The process repeats until all of the data is loaded into the FPGA. The data begins shifting on DOUT 1.5 cycles after it is loaded in parallel. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 43 shows the connections for synchronous peripheral mode.

As with master modes, the peripheral modes can be used as the lead FPGA for a daisy chain of slave FPGAs.

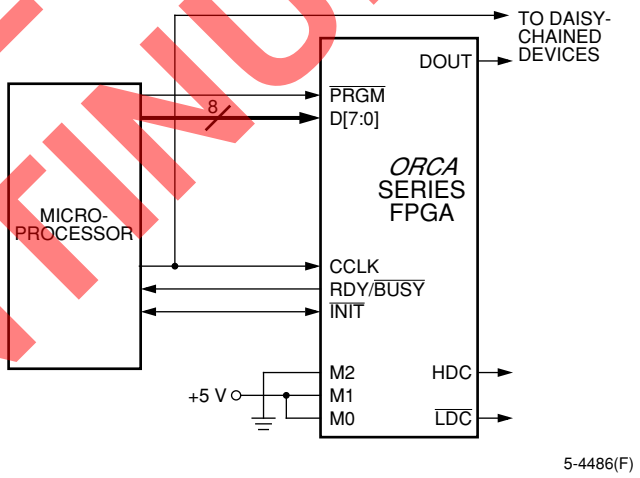


Figure 43. Synchronous Peripheral Configuration Schematic

Special Function Blocks (continued)

Global 3-State Control (TS_ALL)

The TS_ALL block resides in the upper-right corner of the FPGA array.

To increase the testability of the *ORCA* Series FPGAs, the global 3-state function (TS_ALL) disables the device. The TS_ALL signal is driven from either an external pin or an internal signal. Before and during configuration, the TS_ALL signal is driven by the input pad $\overline{\text{RD\_CFG}}$. After configuration, the TS_ALL signal can be disabled, driven from the $\overline{\text{RD\_CFG}}$ input pad, or driven by a general routing signal in the upper-right corner. Before configuration, TS_ALL is active-low; after configuration, the sense of TS_ALL can be inverted.

The following occur when TS_ALL is activated:

1. All of the user I/O output buffers are 3-stated, the user I/O input buffers are pulled up (with the pull-down disabled), and the input buffers are configured with TTL input thresholds (OR2CxxA only).
2. The TDO/RD_DATA output buffer is 3-stated.
3. The $\overline{\text{RD\_CFG}}$, $\overline{\text{RESET}}$, and $\overline{\text{PRGM}}$ input buffers remain active with a pull-up.
4. The DONE output buffer is 3-stated, and the input buffer is pulled-up.

Internal Oscillator

The internal oscillator resides in the lower-left corner of the FPGA array. It has output clock frequencies of 1.25 MHz and 10 MHz. The internal oscillator is the source of the internal CCLK used for configuration. It may also be used after configuration as a general-purpose clock signal.

Global Set/Reset (GSRN)

The GSRN logic resides in the lower-right corner of the FPGA. GSRN is an invertible, default, active-low signal that is used to reset all of the user-accessible latches/FFs on the device. GSRN is automatically asserted at powerup and during configuration of the device.

The timing of the release of GSRN at the end of configuration can be programmed in the start-up logic described below. Following configuration, GSRN may be connected to the $\overline{\text{RESET}}$ pin via dedicated routing, or it may be connected to any signal via normal routing. Within each PFU, individual FFs and latches can be programmed to either be set or reset when GSRN is asserted.

The $\overline{\text{RESET}}$ input pad has a special relationship to GSRN. During configuration, the $\overline{\text{RESET}}$ input pad always initiates a configuration abort, as described in the FPGA States of Operation section. After configuration, the global set/reset signal (GSRN) can either be disabled (the default), directly connected to the $\overline{\text{RESET}}$ input pad, or sourced by a lower-right corner signal. If the $\overline{\text{RESET}}$ input pad is not used as a global reset after configuration, this pad can be used as a normal input pad.

Start-Up Logic

The start-up logic block is located in the lower right corner of the FPGA. This block can be configured to coordinate the relative timing of the release of GSRN, the activation of all user I/Os, and the assertion of the DONE signal at the end of configuration. If a start-up clock is used to time these events, the start-up clock can come from CCLK, or it can be routed into the start-up block using lower-right corner routing resources. These signals are described in the Start-Up subsection of the FPGA States of Operation section.

Estimating Power Dissipation (continued)

OR2T15A Clock Power

P = [0.34 mW/MHz
+ (0.17 mW/MHz – Branch) (# Branches)
+ (0.01 mW/MHz – PFU) (# PFUs)
+ (0.003 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2T15A clock power ≈ 5.9 mW/MHz.

OR2T26A Clock Power

P = [0.35 mW/MHz
+ (0.19 mW/MHz – Branch) (# Branches)
+ (0.01 mW/MHz – PFU) (# PFUs)
+ (0.003 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2T26A clock power ≈ 8.3 mW/MHz.

OR2T40A Clock Power

P = [0.37 mW/MHz
+ (0.23 mW/MHz – Branch) (# Branches)
+ (0.01 mW/MHz – PFU) (# PFUs)
+ (0.003 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2T40A clock power ≈ 12.4 mW/MHz.

The power dissipated in a PIC is the sum of the power dissipated in the four I/Os in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each I/O depends on whether it is configured as an input, output, or input/output. If an I/O is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

The power dissipated by an input buffer ($V_{IH} = V_{DD} –$ 0.3 V or higher) is estimated as:

$$P_{IN} = 0.09 \text{ mW/MHz}$$

The 5 V tolerant input buffer feature dissipates additional dc power. The dc power, P_{TOL}, is always dissipated for the OR2TxxA, regardless of the number of 5 V tolerant input buffers used when the $V_{DD}5$ pins are connected to a 5 V supply as shown in Table 16. This power is not dissipated when the $V_{DD}5$ pins are connected to the 3.3 V supply.

Table 16. DC Power for 5 V Tolerant I/Os for OR2TxxA devices

Device	P_{TOL} ($V_{DD}5$ = 5.25 V)
2T04A	1.7 mW
2T08A	2.4 mW
2T10A	2.7 mW
2T15A	3.4 mW
2T26A	4.0 mW
2T40A	5.0 mW

The ac power dissipation from an output or bidirectional is estimated by the following:

$$P_{OUT} = (C_L + 8.8 \text{ pF}) \times V_{DD}^2 \times F \text{ Watts}$$

where the unit for C_L is farads, and the unit for F is Hz.

As an example of estimating power dissipation, suppose that a fully utilized OR2T15A has an average of three outputs for each of the 400 PFUs, that all 20 clock branches are used, that 150 of the 400 PFUs have FFs clocked at 40 MHz (16 of which are operating in a synchronous memory mode), and that the PFU outputs have an average activity factor of 20%.

Twenty inputs, 32 outputs driving 30 pF loads, and 16 bidirectional I/Os driving 50 pF loads are also generated from the 40 MHz clock with an average activity factor of 20%. The worst-case (V_{DD} = 3.6 V) power dissipation is estimated as follows:

P_{PFU} = 400 x 3 (0.08 mW/MHz x 20 MHz x 20%)
= 384 mW

P_{CLK} = [0.34 mW/MHz + (0.17 mW/MHz – Branch)
(20 Branches)
+ (0.01 mW/MHz – PFU) (150 PFUs)
+ (0.003 mW/MHz – SMEM_PFU)
(16 SMEM_PFUs)] [40 MHz]
= 212 mW

P_{IN} = 20 x [0.09 mW/MHz x 20 MHz x 20%]
= 7 mW

P_{TOL} = 3.4 mW

P_{OUT} = 30 x [(30 pF + 8.8 pF) x $(3.6)^2$ x 20 MHz
x 20%]
= 60 mW

P_{BID} = 16 x [(50 pF + 8.8 pF) x $(3.6)^2$ x 20 MHz
x 20%]
= 49 mW

TOTAL = 0.72 W

Estimating Power Dissipation (continued)

OR2T15B and OR2T40B

The total operating power dissipated is estimated by summing the standby (I_{DDSB}), internal, and external power dissipated. The internal and external power is the power consumed in the PLCs and PICs, respectively. In general, the standby power is small and may be neglected. The total operating power is as follows:

$$P_T = \Sigma P_{PLC} + \Sigma P_{PIC}$$

The internal operating power is made up of two parts: clock generation and PFU output power. The PFU output power can be estimated based upon the number of PFU outputs switching when driving an average fan-out of two:

$$P_{PFU} = 0.08 \text{ mW/MHz}$$

For each PFU output that switches, 0.08 mW/MHz needs to be multiplied times the frequency (in MHz) that the output switches. Generally, this can be estimated by using one-half the clock rate, multiplied by some activity factor; for example, 20%.

The power dissipated by the clock generation circuitry is based upon four parts: the fixed clock power, the power/clock branch row or column, the clock power dissipated in each PFU that uses this particular clock, and the power from the subset of those PFUs that is configured in either of the two synchronous modes (SSPM or SDPM). Therefore, the clock power can be calculated for the four parts using the following equations:

OR2T15B Clock Power

P = [0.30 mW/MHz
+ (0.85 mW/MHz – Branch) (# Branches)
+ (0.008 mW/MHz – PFU) (# PFUs)
+ (0.002 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2T15B clock power ≈ 3.9 mW/MHz.

OR2T40B Clock Power

P = [0.42 mW/MHz
+ (0.118 mW/MHz – Branch) (# Branches)
+ (0.008 mW/MHz – PFU) (# PFUs)
+ (0.002 mW/MHz – SMEM_PFU)
(# SMEM_PFUs)] fCLK

For a quick estimate, the worst-case (typical circuit) OR2T40B clock power ≈ 5.5 mW/MHz.

The power dissipated in a PIC is the sum of the power dissipated in the four I/Os in the PIC. This consists of power dissipated by inputs and ac power dissipated by outputs. The power dissipated in each I/O depends on whether it is configured as an input, output, or input/output. If an I/O is operating as an output, then there is a power dissipation component for P_{IN}, as well as P_{OUT}. This is because the output feeds back to the input.

The power dissipated by an input buffer ($V_{IH} = V_{DD} –$ 0.3 V or higher) is estimated as:

$$P_{IN} = 0.033 \text{ mW/MHz}$$

The OR2TxxB 5 V tolerant input buffer feature does not dissipate additional dc power.

The ac power dissipation from an output or bidirectional is estimated by the following:

$$P_{OUT} = (C_L + 8.8 \text{ pF}) \times V_{DD}^2 \times F \text{ Watts}$$

where the unit for C_L is farads, and the unit for F is Hz.

As an example of estimating power dissipation, suppose that a fully utilized OR2T15B has an average of three outputs for each of the 400 PFUs, that all 20 clock branches are used, that 150 of the 400 PFUs have FFs clocked at 40 MHz (16 of which are operating in a synchronous memory mode), and that the PFU outputs have an average activity factor of 20%.

Twenty inputs, 32 outputs driving 30 pF loads, and 16 bidirectional I/Os driving 50 pF loads are also generated from the 40 MHz clock with an average activity factor of 20%. The worst-case (V_{DD} = 3.6 V) power dissipation is estimated as follows:

P_{PFU} = 400 x 3 (0.08 mW/MHz x 20 MHz x 20%)
= 384 mW

P_{CLK} = [0.30 mW/MHz + (0.085 mW/MHz – Branch)
(20 Branches)
+ (0.008 mW/MHz – PFU) (150 PFUs)
+ (0.002 mW/MHz – SMEM_PFU)
(16 SMEM_PFUs)] [40 MHz]
= 129 mW

P_{IN} = 20 x [0.033 mW/MHz x 20 MHz x 20%]
= 3 mW

P_{TOL} = 3.4 mW

P_{OUT} = 30 x [(30 pF + 8.8 pF) x $(3.6)^2$ x 20 MHz
x 20%]
= 60 mW

P_{BID} = 16 x [(50 pF + 8.8 pF) x $(3.6)^2$ x 20 MHz
x 20%]
= 49 mW

TOTAL = 0.72 W

Pin Information (continued)

Table 19. OR2C04A, OR2C12A, and OR2C/2T15A 84-Pin PLCC Pinout (continued)

Pin	2C04A Pad	2C12A Pad	2C/2T15A Pad	Function
44	PB6A	PB10A	PB11A	I/O
45	VSS	VSS	VSS	VSS
46	PB7A	PB11A	PB12A	I/O-VDD5
47	PB7D	PB11D	PB12D	I/O
48	PB8A	PB12A	PB13A	I/O-HDC
49	PB9A	PB13A	PB14A	I/O-$\overline{LDC}$
50	PB9D	PB13D	PB14D	I/O
51	PB10A	PB15A	PB16A	I/O-$\overline{INIT}$
52	PB10D	PB18D	PB20D	I/O
53	DONE	DONE	DONE	DONE
54	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$
55	$\overline{PRGM}$	$\overline{PRGM}$	$\overline{PRGM}$	$\overline{PRGM}$
56	PR10A	PR18A	PR20A	I/O-M0
57	PR10D	PR16A	PR17A	I/O
58	PR9A	PR15D	PR16D	I/O-M1
59	PR9D	PR13A	PR14A	I/O
60	PR8A	PR12A	PR13A	I/O-M2
61	PR7A	PR11A	PR12A	I/O-M3
62	PR7D	PR11D	PR12D	I/O
63	PR6A	PR10A	PR11A	I/O
64	VDD	VDD	VDD	VDD
65	PR5A	PR9A	PR10A	I/O
66	VSS	VSS	VSS	VSS
67	PR4A	PR8A	PR9A	I/O
68	PR4D	PR8D	PR9D	I/O
69	PR3A	PR7A	PR8A	I/O-CS1
70	PR2A	PR6A	PR7A	I/O-$\overline{CS0}$
71	PR2D	PR5D	PR6D	I/O
72	PR1A	PR4A	PR5A	I/O-$\overline{RD}$
73	PR1D	PR2A	PR3A	I/O-$\overline{WR}$
74	$\overline{RD\_CFG}$	$\overline{RD\_CFG}$	$\overline{RD\_CFG}$	$\overline{RD\_CFG}$
75	VDD	VDD	VDD	VDD
76	VSS	VSS	VSS	VSS
77	PT10C	PT17D	PT19A	I/O-RDY/RCLK
78	PT9D	PT15D	PT16D	I/O-D7
79	PT9C	PT14D	PT15D	I/O
80	PT9A	PT13B	PT14B	I/O-D6
81	PT8A	PT12A	PT13A	I/O-D5
82	PT7D	PT11D	PT12D	I/O
83	PT7A	PT11A	PT12A	I/O-D4
84	PT6A	PT10A	PT11A	I/O-D3

Note: The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 24. OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 240-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
43	PL9A	PL10A	PL11A	PL12A	PL13A	PL17A	PL20A	I/O-A11
44	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
45	PL10D	PL11D	PL12D	PL13D	PL14D	PL18D	PL21D	I/O-A12
46	PL10C	PL11C	PL12C	PL13B	PL14B	PL18B	PL21B	I/O
47	PL10B	PL11B	PL12B	PL14D	PL15D	PL19D	PL22D	I/O
48	PL10A	PL11A	PL13D	PL14B	PL15B	PL19B	PL22B	I/O-A13
49	PL11D	PL12D	PL13B	PL14A	PL15A	PL19A	PL22A	I/O
50	PL11C	PL12C	PL13A	PL15D	PL16D	PL20D	PL23D	I/O
51	PL11B	PL12B	PL14D	PL15B	PL16B	PL20B	PL24D	I/O
52	PL11A	PL12A	PL14C	PL16D	PL17D	PL21D	PL25A	I/O-A14
53	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
54	PL12D	PL13D	PL15D	PL17D	PL18D	PL22D	PL27D	I/O
55	PL12C	PL13A	PL15A	PL17A	PL19D	PL23D	PL28D	I/O
56	PL12B	PL14D	PL16D	PL18C	PL19A	PL23A	PL28A	I/O
57	PL12A	PL14A	PL16A	PL18A	PL20A	PL24A	PL30A	I/O-A15
58	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
59	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
60	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
61	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
62	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
63	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	I/O-A16
64	PB1B	PB1D	PB1D	PB1D	PB2A	PB2A	PB3A	I/O
65	PB1C	PB2A	PB2A	PB2A	PB2D	PB2D	PB3D	I/O-VDD5
66	PB1D	PB2D	PB2D	PB2D	PB3D	PB3D	PB4D	I/O
67	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
68	PB2A	PB3A	PB3B	PB3D	PB4D	PB4D	PB5D	I/O-A17
69	PB2B	PB3B	PB4B	PB4D	PB5D	PB5D	PB6D	I/O
70	PB2C	PB3C	PB4C	PB5A	PB6A	PB6A	PB7A	I/O
71	PB2D	PB3D	PB4D	PB5B	PB6B	PB6B	PB7D	I/O
72	PB3A	PB4A	PB5A	PB5D	PB6D	PB6D	PB8D	I/O
73	PB3B	PB4B	PB5B	PB6A	PB7A	PB7A	PB9A	I/O
74	PB3C	PB4C	PB5C	PB6B	PB7B	PB7B	PB9D	I/O
75	PB3D	PB4D	PB5D	PB6D	PB7D	PB7D	PB10D	I/O
76	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
77	PB4A	PB5A	PB6A	PB7A	PB8A	PB8A	PB11A	I/O
78	PB4B	PB5B	PB6B	PB7B	PB8B	PB8D	PB11D	I/O
79	PB4C	PB5C	PB6C	PB7C	PB8C	PB9A	PB12A	I/O
80	PB4D	PB5D	PB6D	PB7D	PB8D	PB9D	PB12D	I/O
81	PB5A	PB6A	PB7A	PB8A	PB9A	PB10A	PB13A	I/O
82	PB5B	PB6B	PB7B	PB8B	PB9B	PB10D	PB13D	I/O
83	PB5C	PB6C	PB7C	PB8C	PB9C	PB11A	PB14A	I/O
84	PB5D	PB6D	PB7D	PB8D	PB9D	PB11D	PB14D	I/O

Notes:
The OR2C/2T08A and OR2C/2T10A do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 26. OR2C12A, OR2C15A, OR2C26A, and OR2C40A 304-Pin SQFP/SQFP2 Pinout

Pin	2C12A Pad	2C15A Pad	2C26A Pad	2C40A Pad	Function
1	VSS	VSS	VSS	VSS	VSS
2	VDD	VDD	VDD	VDD	VDD
3	VSS	VSS	VSS	VSS	VSS
4	PL1D	PL1D	PL1D	PL1D	I/O
5	PL1C	PL1C	PL1C	PL1A	I/O
6	PL1B	PL1B	PL1B	PL2D	I/O
7	PL1A	PL1A	PL1A	PL2A	I/O
8	PL2D	PL2D	PL2D	PL3D	I/O-A0
9	PL2C	PL2A	PL2A	PL3A	I/O
10	PL2B	PL3D	PL3D	PL4D	I/O
11	PL2A	PL3A	PL3A	PL4A	I/O
12	VSS	VSS	VSS	VSS	VSS
13	PL3D	PL4D	PL4D	PL5D	I/O
14	PL3A	PL4A	PL4A	PL6D	I/O
15	PL4D	PL5D	PL5D	PL7D	I/O
16	PL4A	PL5A	PL5A	PL8D	I/O-A1
17	PL5D	PL6D	PL6D	PL9D	I/O
18	PL5C	PL6C	PL6C	PL9C	I/O
19	PL5B	PL6B	PL6B	PL9B	I/O
20	PL5A	PL6A	PL6A	PL9A	I/O-A2
21	PL6D	PL7D	PL7D	PL10D	I/O
22	PL6C	PL7C	PL7C	PL10C	I/O
23	PL6B	PL7B	PL7B	PL10B	I/O
24	PL6A	PL7A	PL7A	PL10A	I/O-A3
25	VDD	VDD	VDD	VDD	VDD
26	PL7D	PL8D	PL8D	PL11D	I/O
27	PL7C	PL8C	PL8A	PL11A	I/O
28	PL7B	PL8B	PL9D	PL12D	I/O
29	PL7A	PL8A	PL9A	PL12A	I/O-A4
30	PL8D	PL9D	PL10D	PL13D	I/O-A5
31	PL8C	PL9C	PL10A	PL13A	I/O
32	PL8B	PL9B	PL11D	PL14D	I/O
33	PL8A	PL9A	PL11A	PL14A	I/O-A6
34	VSS	VSS	VSS	VSS	VSS
35	PL9D	PL10D	PL12D	PL15D	I/O
36	PL9C	PL10C	PL12C	PL15C	I/O
37	PL9B	PL10B	PL12B	PL15B	I/O
38	PL9A	PL10A	PL12A	PL15A	I/O-A7
39	VDD	VDD	VDD	VDD	VDD
40	PL10D	PL11D	PL13D	PL16D	I/O
41	PL10C	PL11C	PL13C	PL16C	I/O
42	PL10B	PL11B	PL13B	PL16B	I/O
43	PL10A	PL11A	PL13A	PL16A	I/O-A8
44	VSS	VSS	VSS	VSS	VSS

Note: The OR2TxxA and OR2TxxB series are not offered in the 304-pin SQFP/SQFP2 packages.

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
B1	PL1D	PL1D	PL1D	PL1D	PL1D	I/O
C2	PL1C	PL1C	PL1C	PL1C	PL1A	I/O
C1	PL1B	PL1B	PL1B	PL1B	PL2D	I/O
D2	PL1A	PL1A	PL1A	PL1A	PL2A	I/O
D3	PL2D	PL2D	PL2D	PL2D	PL3D	I/O-A0
D1	PL2C	PL2C	PL2A	PL2A	PL3A	I/O
E2	PL2B	PL2B	PL3D	PL3D	PL4D	I/O
E4	—	—	PL3B	PL3B	PL4B	I/O
E3	PL2A	PL2A	PL3A	PL3A	PL4A	I/O
E1	PL3D	PL3D	PL4D	PL4D	VDD5	I/O-VDD5
F2	—	PL3C	PL4C	PL4C	PL5C	I/O
G4	PL3C	PL3B	PL4B	PL4B	PL5B	I/O
F3	—	PL3A	PL4A	PL4A	PL6D	I/O
F1	PL3B	PL4D	PL5D	PL5D	PL7D	I/O
G2	—	PL4C	PL5C	PL5C	PL7C	I/O
G1	—	PL4B	PL5B	PL5B	PL7B	I/O
G3	PL3A	PL4A	PL5A	PL5A	PL8D	I/O-A1
H2	PL4D	PL5D	PL6D	PL6D	PL9D	I/O
J4	PL4C	PL5C	PL6C	PL6C	PL9C	I/O
H1	PL4B	PL5B	PL6B	PL6B	PL9B	I/O
H3	PL4A	PL5A	PL6A	PL6A	PL9A	I/O-A2
J2	PL5D	PL6D	PL7D	PL7D	PL10D	I/O
J1	PL5C	PL6C	PL7C	PL7C	PL10C	I/O
K2	PL5B	PL6B	PL7B	PL7B	PL10B	I/O
J3	PL5A	PL6A	PL7A	PL7A	PL10A	I/O-A3
K1	PL6D	PL7D	PL8D	PL8D	PL11D	I/O
K4	PL6C	PL7C	PL8C	PL8A	PL11A	I/O
L2	PL6B	PL7B	PL8B	PL9D	PL12D	I/O
K3	PL6A	PL7A	PL8A	PL9A	PL12A	I/O-A4
L1	PL7D	PL8D	PL9D	PL10D	PL13D	I/O-A5
M2	PL7C	PL8C	PL9C	PL10A	PL13A	I/O
M1	PL7B	PL8B	PL9B	PL11D	PL14D	I/O
L3	PL7A	PL8A	PL9A	PL11A	PL14A	I/O-A6
N2	PL8D	PL9D	PL10D	PL12D	PL15D	I/O
M4	PL8C	PL9C	PL10C	PL12C	PL15C	I/O
N1	PL8B	PL9B	PL10B	PL12B	PL15B	I/O
M3	PL8A	PL9A	PL10A	PL12A	PL15A	I/O-A7
P2	PL9D	PL10D	PL11D	PL13D	PL16D	I/O

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
AH3	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
AH2	PR20A	PR24A	PR30A	I/O-M0
AH1	PR20B	PR24B	PR30B	I/O
AF4	PR20C	PR24C	PR29A	I/O
AG3	PR20D	PR24D	PR29D	I/O
AG2	PR19A	PR23A	PR28A	I/O-VDD5
AG1	PR19B	PR23B	PR28B	I/O
AF3	PR19C	PR23C	PR28C	I/O
AF2	PR19D	PR23D	PR28D	I/O
AF1	PR18A	PR22A	PR27A	I/O
AD4	PR18B	PR22B	PR27B	I/O
AE3	PR18C	PR22C	PR27C	I/O
AE2	PR18D	PR22D	PR27D	I/O
AE1	PR17A	PR21A	PR26A	I/O
AC4	PR17B	PR21B	PR26B	I/O
AD3	PR17C	PR21C	PR26C	I/O
AD2	PR17D	PR21D	PR25A	I/O
AC3	PR16A	PR20A	PR24A	I/O
AB4	PR16B	PR20B	PR24B	I/O
AC2	PR16C	PR20C	PR24D	I/O
AC1	PR16D	PR20D	PR23D	I/O-M1
AB3	PR15A	PR19A	PR22A	I/O
AB2	PR15B	PR19B	PR22B	I/O
AB1	PR15C	PR19C	PR22C	I/O
AA3	PR15D	PR19D	PR22D	I/O-VDD5
Y4	PR14A	PR18A	PR21A	I/O
AA2	PR14B	PR18B	PR21B	I/O
AA1	PR14C	PR18C	PR21C	I/O
Y3	PR14D	PR18D	PR21D	I/O
W4	PR13A	PR17A	PR20A	I/O-M2
Y2	PR13B	PR17D	PR20D	I/O
W3	PR13C	PR16A	PR19A	I/O
W2	PR13D	PR16B	PR19B	I/O
V4	—	PR16D	PR19D	I/O
W1	PR12A	PR15A	PR18A	I/O-M3
V3	—	PR15D	PR18D	I/O
V2	PR12B	PR14A	PR17A	I/O
V1	PR12C	PR14B	PR17B	I/O
U3	PR12D	PR14D	PR17D	I/O
U2	PR11A	PR13A	PR16A	I/O
U1	PR11B	PR13B	PR16B	I/O
T3	PR11C	PR13C	PR16C	I/O
T4	PR11D	PR13D	PR16D	I/O
T2	PR10A	PR12A	PR15A	I/O

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
R1	PR10B	PR12B	PR15B	I/O
R2	PR10C	PR12C	PR15C	I/O
R3	PR10D	PR12D	PR15D	I/O
P1	PR9A	PR11A	PR14A	I/O-VDD5
P2	PR9B	PR11C	PR14C	I/O
P3	PR9C	PR11D	PR14D	I/O
N1	—	PR10A	PR13A	I/O
P4	PR9D	PR10C	PR13C	I/O
N2	—	PR10D	PR13D	I/O
N3	PR8A	PR9A	PR12A	I/O-CS1
M2	PR8B	PR9D	PR12D	I/O
N4	PR8C	PR8A	PR11A	I/O
M3	PR8D	PR8D	PR11D	I/O
L1	PR7A	PR7A	PR10A	I/O-$\overline{CS0}$
L2	PR7B	PR7B	PR10B	I/O
M4	PR7C	PR7C	PR10C	I/O
L3	PR7D	PR7D	PR10D	I/O
K1	PR6A	PR6A	PR9A	I/O
K2	PR6B	PR6B	PR9B	I/O
K3	PR6C	PR6C	PR9C	I/O
J1	PR6D	PR6D	PR9D	I/O
J2	PR5A	PR5A	PR8A	I/O-$\overline{RD}$
K4	PR5B	PR5B	PR7A	I/O
J3	PR5C	PR5C	PR7C	I/O
H2	PR5D	PR5D	PR6A	I/O
H3	PR4A	PR4A	PR5A	I/O-VDD5
J4	PR4B	PR4B	PR5B	I/O
G1	PR4C	PR4C	PR5C	I/O
G2	PR4D	PR4D	PR5D	I/O
G3	PR3A	PR3A	PR4A	I/O-$\overline{WR}$
H4	PR3B	PR3B	PR4B	I/O
F1	PR3C	PR3C	PR4C	I/O
F2	PR3D	PR3D	PR4D	I/O
F3	PR2A	PR2A	PR3A	I/O
E1	PR2B	PR2B	PR3B	I/O
E2	PR2C	PR2C	PR3C	I/O
E3	PR2D	PR2D	PR3D	I/O
F4	PR1A	PR1A	PR2A	I/O
D1	PR1B	PR1B	PR2D	I/O
D2	PR1C	PR1C	PR1A	I/O
D3	PR1D	PR1D	PR1D	I/O
E4	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
D5	PT20D	PT24D	PT30D	I/O
C4	PT20C	PT24C	PT30A	I/O

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Timing Characteristics (continued)

Table 37A. OR2CxxA and OR2TxxA Asynchronous Memory Read During Write Operation (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C. OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read During Write Operation (TJ = 85 °C, VDD = min):												
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.9	—	4.8	—	3.9	—	4.0	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	6.4	—	5.8	—	4.7	—	4.7	—	4.5	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	3.6	—	3.1	—	2.5	—	2.5	—	2.2	ns

Table 37B. OR2TxxB Asynchronous Memory Read During Write Operation (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Read During Write Operation (TJ = +85 °C, VDD = min):						
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.5	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	4.6	—	4.0	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	2.7	—	2.4	ns

Timing Characteristics (continued)

Table 46A. OR2CxxA/OR2TxxA Programmable I/O Cell Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Inputs (TJ = 85 °C, VDD = min)												
Input Rise Time	TR	—	500	—	500	—	500	—	500	—	500	ns
Input Fall Time	TF	—	500	—	500	—	500	—	500	—	500	ns
Pad to In Delay	PAD_IN_DEL	—	1.5	—	1.3	—	1.2	—	1.2	—	1.1	ns
Pad to Nearest PFU Latch Output	CHIP_LATCH	—	4.7	—	4.1	—	3.5	—	3.1	—	2.9	ns
Delay Added to General Routing (input buffer in delay mode for OR2C/2T15A and smaller devices)	—	—	7.0	—	6.0	—	5.9	—	6.2	—	5.8	ns
Delay Added to General Routing (input buffer in delay mode for OR2C/2T26A and OR2C/2T40A)	—	—	9.7	—	8.6	—	8.6	—	9.0	—	8.6	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2C/2T15A and smaller devices)	—	—	6.8	—	5.9	—	6.0	—	6.4	—	6.0	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2C/2T26A and OR2C/2T40A)	—	—	10.2	—	8.5	—	8.6	—	9.1	—	7.9	ns
Outputs (TJ = 85 °C, VDD = min, CL = 50 pF)												
PFU CK to Pad Delay (DOUT[3:0] to PAD):												
Fast	DOUT_DEL(F)	—	6.2	—	5.5	—	5.0	—	4.4	—	3.3	ns
Slewlim	DOUT_DEL(SL)	—	8.4	—	7.4	—	6.4	—	5.6	—	4.1	ns
Sinklim	DOUT_DEL(SI)	—	10.5	—	9.4	—	9.5	—	8.3	—	7.2	ns
Output to Pad Delay (OUT[3:0] to PAD):												
Fast	OUT_DEL(F)	—	4.0	—	3.6	—	3.1	—	2.7	—	2.3	ns
Slewlim	OUT_DEL(SL)	—	6.3	—	5.5	—	4.5	—	3.9	—	3.1	ns
Sinklim	OUT_DEL(SI)	—	7.2	—	7.5	—	7.6	—	6.5	—	6.2	ns
3-state Enable Delay (TS[3:0] to PAD):												
Fast	TS_DEL(F)	—	4.7	—	4.0	—	3.5	—	3.1	—	2.5	ns
Slewlim	TS_DEL(SL)	—	7.0	—	6.3	—	5.2	—	4.7	—	3.7	ns
Sinklim	TS_DEL(SI)	—	7.9	—	8.4	—	9.3	—	8.0	—	7.6	ns

Notes:
If the input buffer is placed in delay mode, the chip hold time to the nearest PFU latch is guaranteed to be 0 if the clock is routed using the primary clock network; (TJ = all, VDD = all). It should also be noted that any signals routed on the clock lines or using the TRIDI buffers directly from the input buffer do not get delayed at any time.

The delays for all input buffers assume an input rise/fall time of ≤1 V/ns.

Timing Characteristics (continued)

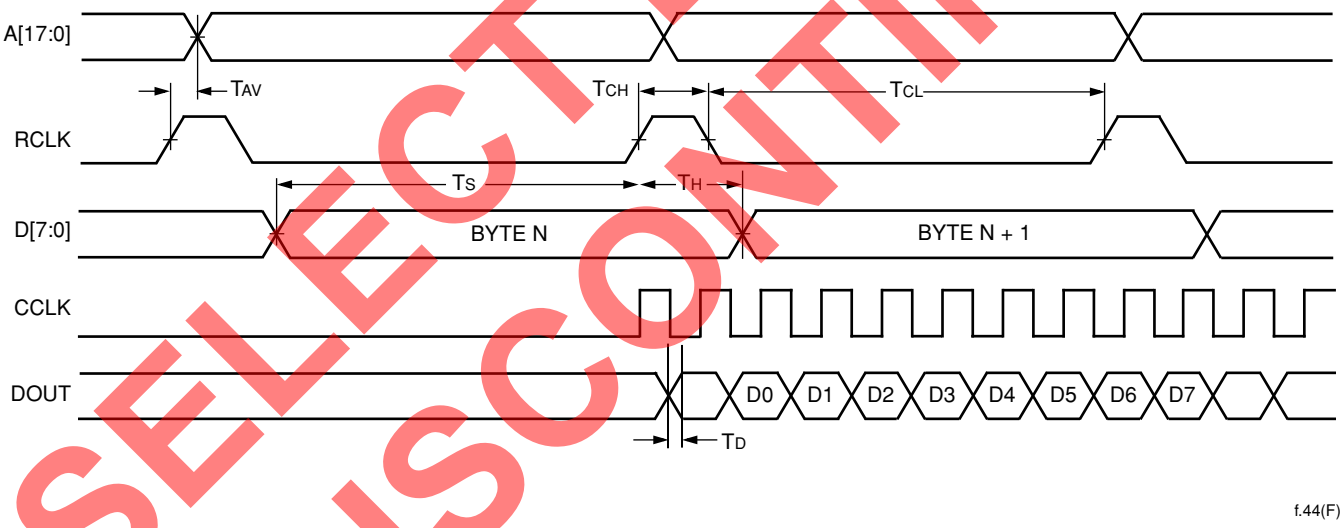
Table 49. Series 2 Master Parallel Configuration Mode Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA/B Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA/B Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Min	Max	Unit
RCLK to Address Valid	TAV	0	200	ns
D[7:0] Setup Time to RCLK High	TS	60	—	ns
D[7:0] Hold Time to RCLK High	TH	0	—	ns
RCLK Low Time (M3 = 0)	TCL	462	1855	ns
RCLK High Time (M3 = 0)	TCH	66	265	ns
RCLK Low Time (M3 = 1)	TCL	3696	14840	ns
RCLK High Time (M3 = 1)	TCH	528	2120	ns
CCLK to DOUT	TD	—	30	ns

Notes:
The RCLK period consists of seven CCLKs for RCLK low and one CCLK for RCLK high.

Serial data is transmitted out on DOUT 1.5 CCLK cycles after the byte is input D[7:0]



f.44(F)

Figure 67. Master Parallel Configuration Mode Timing Diagram

Package Outline Drawings (continued)

208-Pin SQFP2

Dimensions are in millimeters.

5-3828(F)