Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1600
Total RAM Bits	25600
Number of I/O	171
Number of Gates	44200
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or2t15a6s208i-db

Table 4. ORCA Series 2TB System Performance

Function	# PFUs	Speed Grade		Unit
		-7	-8	
16-bit loadable up/down counter	4	131.6	149.3	MHz
16-bit accumulator	4	131.6	149.3	MHz
8 x 8 parallel multiplier: — Multiplier mode, unpipelined[1] — ROM mode, unpipelined[2] — Multiplier mode, pipelined[3]	 22 9 44	 37.7 103.1 123.5	 44.8 120.5 142.9	 MHz MHz MHz
32 x 16 RAM: — Single port (read and write/cycle)[4] — Single port[5] — Dual port[6]	 9 9 16	 57.5 97.7 97.7	 69.4 112.4 112.4	 MHz MHz MHz
36-bit parity check (internal)	4	6.1	5.1	ns
32-bit address decode (internal)	3.25	4.8	4.0	ns

1. Implemented using 4 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 16 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 4 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (28 of 44 PFUs contain only pipelining registers).
4. Implemented using 16 x 4 synchronous single-port RAM mode allowing both read and write per clock cycle, including write/read address multiplexer.
5. Implemented using 16 x 4 synchronous single-port RAM mode allowing either read or write per clock cycle, including write/read address multiplexer.
6. Implemented using 16 x 2 synchronous dual-port RAM mode.

Interquad Routing (continued)

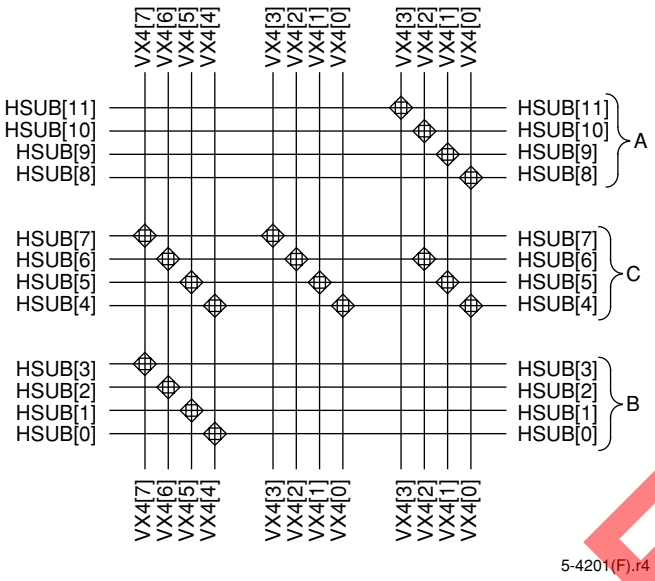


Figure 31. Horizontal Subquad Routing Connectivity

The X4 and XH lines make the only connections to the subquad lines; therefore, the array remains symmetrical and homogeneous. Since each subquad is made from a 4 x 4 array of PLCs, the distance between sets of subquad lines is four PLCs, which is also the distance between the breaks of the X4 lines. Therefore, each X4 line will cross exactly one set of subquad lines. Since all X4 lines make the same connections to the subquad lines that they cross, all X4 lines in the array have the same connectivity, and the symmetry of the routing is preserved. Since all XH lines cross the same number of subquad blocks, the symmetry is maintained for the XH lines as well.

The new subquad lines travel a length of eight PLCs (seven PLCs on the outside edge) before they are broken. Unlike other inter-PLC lines, they cannot be connected end-to-end. As shown in Figure 30, some of the horizontal (vertical) subquad lines have connectivity to the subquad to the left of (above) the current subquad, while others have connectivity to the subquad to the right (below). This allows connections to/from the current subquad from/to the PLCs in all subquads that surround it.

Between all subquads, including in the center of the array, there are three groups of subquad lines where each group contains four lines. Figure 31 shows the connectivity of these three groups of subquad lines (HSUB) to the VX4 and VXH lines running between a vertical pair of PLCs. Between each vertical pair of subquad blocks, four of the blocks shown in Figure 31 are used, one for each pair of vertical PLCs.

The first two groups, depicted as A and B, have connectivity to only one of the two sets of X4 lines between pairs of PLCs. Since they are very lightly loaded, they are very fast. The third group, C, connects to both groups of X4 lines between pairs of PLCs, as well as all of the XH lines between pairs of PLCs, providing high flexibility. The connectivity for the vertical subquad routing (Vsub) is the same as described above for the horizontal subquad routing, when rotated onto the other axis.

At the center row and column of each quadrant, a fourth group of subquad lines has been added. These subquad lines only have connectivity to the XH lines. The XH lines are also broken at this point, which means that each XH line travels one-half of the quadrant (i.e., one-quarter of the device) before it is broken by a CIP. Since the XH lines can be connected end-to-end, the resulting line can be either one-quarter, one-half, three-quarters, or the entire length of the array. The connectivity of the XH lines and this fourth group of subquad lines, indicated as D, are detailed in Figure 32. Again, the connectivity for the vertical subquad routing (VSUB) is the same as the horizontal subquad routing, when rotated onto the other axis.

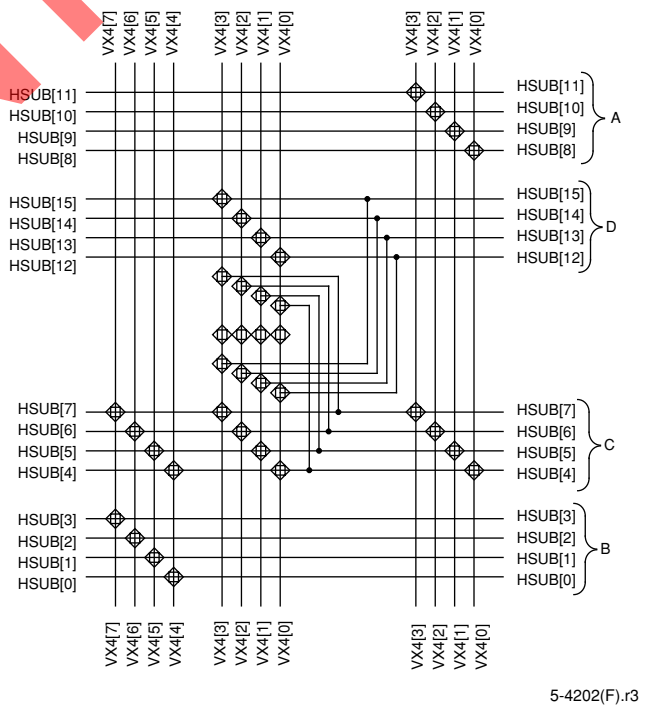
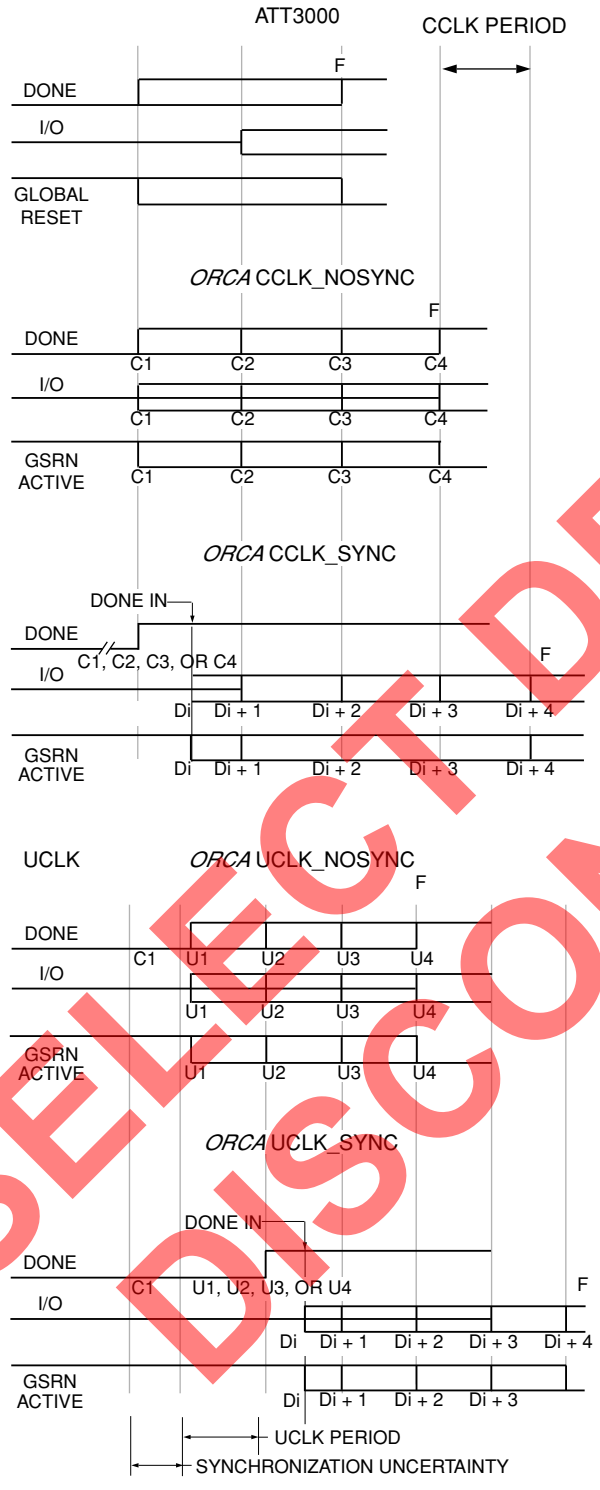


Figure 32. Horizontal Subquad Routing Connectivity (Half Quad)

FPGA States of Operation (continued)



F = finished, no more CLKs required.

5-2761(F).r4

Figure 38. Start-Up Waveforms

Partial Reconfiguration

All *ORCA* device families have been designed to allow a partial reconfiguration of the FPGA at any time. This is done by setting a bit stream option in the previous configuration sequence that tells the FPGA to not reset all of the configuration RAM during a reconfiguration. Then only the configuration frames that are to be modified need to be rewritten, thereby reducing the configuration time.

Other bit stream options are also available that allow one portion of the FPGA to remain in operation while a partial reconfiguration is being done. If this is done, the user must be careful to not cause contention between the two configurations (the bit stream resident in the FPGA and the partial reconfiguration bit stream) as the second reconfiguration bit stream is being loaded.

Other Configuration Options

Configuration options used during device start-up were previously discussed in the FPGA States of Operation section of this data sheet. There are many other configuration options available to the user that can be set during bit stream generation in ispLEVER. These include options to enable boundary scan, readback options, and options to control and use the internal oscillator after configuration.

Other useful options that affect the next configuration (not the current configuration process) include options to disable the global set/reset during configuration, disable the 3-state of I/Os during configuration, and disable the reset of internal RAMs during configuration to allow for partial configurations (see above). For more information on how to set these and other configuration options, please see the ispLEVER documentation.

Configuration Data Format

The ispLEVER development system interfaces with front-end design entry tools and provides the tools to produce a fully configured FPGA. This section discusses using the ispLEVER development system to generate configuration RAM data and then provides the details of the configuration frame format.

The *ORCA* Series 2 series of FPGAs are enhanced versions of the *ORCA* ATT2Cxx/ATT2Txx architectures that provide upward bit stream compatibility for both series of devices as well as with each other.

FPGA Configuration Modes (continued)

Asynchronous Peripheral Mode

Figure 42 shows the connections needed for the asynchronous peripheral mode. In this mode, the FPGA system interface is similar to that of a microprocessor-peripheral interface. The microprocessor generates the control signals to write an 8-bit byte into the FPGA. The FPGA control inputs include active-low $\overline{CS0}$ and active-high CS1 chip selects, a write $\overline{WR}$ input, and a read $\overline{RD}$ input. The chip selects can be cycled or maintained at a static level during the configuration cycle. Each byte of data is written into the FPGA's D[7:0] input pins.

The FPGA provides a RDY status output to indicate that another byte can be loaded. A low on RDY indicates that the double-buffered hold/shift registers are not ready to receive data, and this pin must be monitored to go high before another byte of data can be written. The shortest time RDY is low occurs when a byte is loaded into the hold register and the shift register is empty, in which case the byte is immediately transferred to the shift register. The longest time for RDY to remain low occurs when a byte is loaded into the holding register and the shift register has just started shifting configuration data into configuration RAM.

The RDY status is also available on the D7 pin by enabling the chip selects, setting $\overline{WR}$ high, and applying $\overline{RD}$ low, where the $\overline{RD}$ input is an output enable for the D7 pin when $\overline{RD}$ is low. The D[6:0] pins are not enabled to drive when $\overline{RD}$ is low and, thus, only act as input pins in asynchronous peripheral mode.

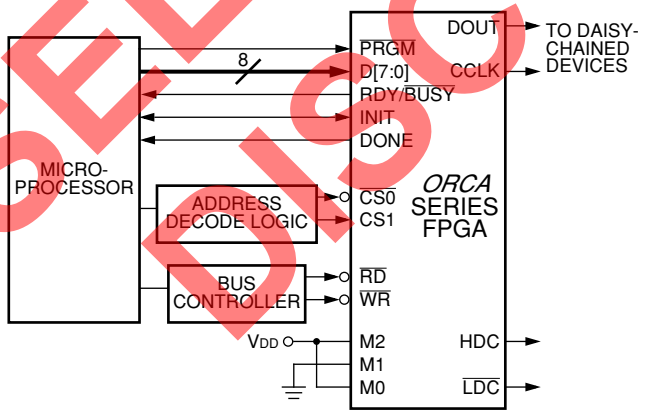


Figure 42. Asynchronous Peripheral Configuration Schematic

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the CCLK input. The first data byte is clocked in on the second CCLK after $\overline{INIT}$ goes high. Subsequent data bytes are clocked in on every eighth rising edge of CCLK. The RDY signal is an output which acts as an acknowledge. RDY goes high one CCLK after data is clocked and, after one CCLK cycle, returns low. The process repeats until all of the data is loaded into the FPGA. The data begins shifting on DOUT 1.5 cycles after it is loaded in parallel. It requires additional CCLKs after the last byte is loaded to complete the shifting. Figure 43 shows the connections for synchronous peripheral mode.

As with master modes, the peripheral modes can be used as the lead FPGA for a daisy chain of slave FPGAs.

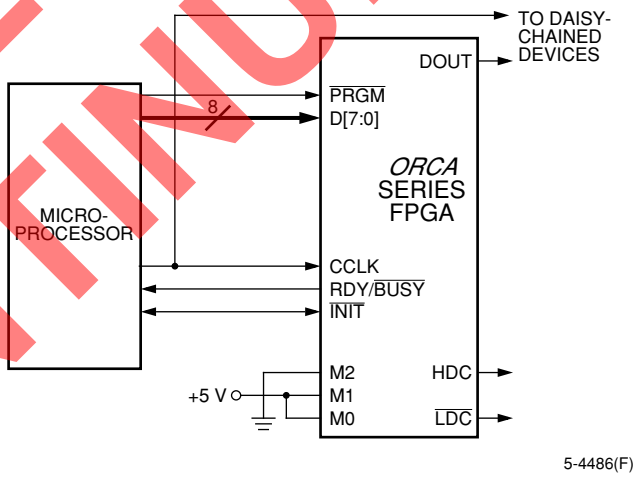


Figure 43. Synchronous Peripheral Configuration Schematic

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout

Pin	2C/2T04A Pad	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
3	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	I/O
4	PL1C	PL1A	PL2D	PL2D	PL2D	PL2D	PL2D	PL3D	I/O-A0
5	PL1B	PL2D	PL3D	PL3D	PL3D	PL4D	PL4D	PL5D	I/O-VDD5
6	See Note	PL2C	PL3C	PL3C	PL3A	PL4A	PL4A	PL6D	I/O
7	PL1A	PL2A	PL3A	PL3A	PL4A	PL5A	PL5A	PL8D	I/O-A1
8	PL2D	PL3D	PL4D	PL4A	PL5A	PL6A	PL6A	PL9A	I/O-A2
9	PL2C	PL3C	PL4C	PL5C	PL6D	PL7D	PL7D	PL10D	I/O
10	PL2B	PL3B	PL4B	PL5B	PL6B	PL7B	PL7B	PL10B	I/O
11	PL2A	PL3A	PL4A	PL5A	PL6A	PL7A	PL7A	PL10A	I/O-A3
12	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
13	PL3D	PL4D	PL5D	PL6D	PL7D	PL8D	PL8D	PL11D	I/O
14	PL3C	PL4C	PL5C	PL6C	PL7C	PL8C	PL8A	PL11A	I/O
15	PL3B	PL4B	PL5B	PL6B	PL7B	PL8B	PL9D	PL12D	I/O
16	PL3A	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL12A	I/O-A4
17	PL4D	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL13D	I/O-A5
18	PL4C	PL5C	PL6C	PL7C	PL8C	PL9C	PL10A	PL13A	I/O
19	PL4B	PL5B	PL6B	PL7B	PL8B	PL9B	PL11D	PL14D	I/O
20	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL11A	PL14A	I/O-A6
21	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
22	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL12D	PL15D	I/O
23	PL5C	PL6C	PL7C	PL8C	PL9C	PL10C	PL12C	PL15C	I/O
24	PL5B	PL6B	PL7B	PL8B	PL9B	PL10B	PL12B	PL15B	I/O
25	PL5A	PL6A	PL7A	PL8A	PL9A	PL10A	PL12A	PL15A	I/O-A7
26	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
27	PL6D	PL7D	PL8D	PL9D	PL10D	PL11D	PL13D	PL16D	I/O
28	PL6C	PL7C	PL8C	PL9C	PL10C	PL11C	PL13C	PL16C	I/O-VDD5
29	PL6B	PL7B	PL8B	PL9B	PL10B	PL11B	PL13B	PL16B	I/O
30	PL6A	PL7A	PL8A	PL9A	PL10A	PL11A	PL13A	PL16A	I/O-A8
31	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
32	PL7D	PL8D	PL9D	PL10D	PL11D	PL12D	PL14D	PL17D	I/O-A9
33	PL7C	PL8C	PL9C	PL10C	PL11C	PL12C	PL14A	PL17A	I/O
34	PL7B	PL8B	PL9B	PL10B	PL11B	PL12B	PL15D	PL18D	I/O
35	PL7A	PL8A	PL9A	PL10A	PL11A	PL12A	PL15A	PL18A	I/O-A10
36	PL8D	PL9D	PL10D	PL11D	PL12D	PL13D	PL16D	PL19D	I/O
37	PL8C	PL9C	PL10C	PL11C	PL12C	PL13C	PL16A	PL19A	I/O
38	PL8B	PL9B	PL10B	PL11B	PL12B	PL13B	PL17D	PL20D	I/O
39	PL8A	PL9A	PL10A	PL11A	PL12A	PL13A	PL17A	PL20A	I/O-A11
40	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
41	PL9D	PL10D	PL11D	PL12D	PL13D	PL14D	PL18D	PL21D	I/O-A12
42	PL9C	PL10C	PL11C	PL12C	PL13B	PL14B	PL18B	PL21B	I/O
43	PL9B	PL10B	PL11B	PL12B	PL14D	PL15D	PL19D	PL22D	I/O

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C/2T04A Pad	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
44	PL9A	PL10A	PL11A	PL13D	PL14B	PL15B	PL19B	PL22B	I/O-A13
45	See Note	PL11D	PL12D	PL13B	PL15D	PL16D	PL20D	PL23D	I/O
46	PL10D	PL11A	PL12A	PL14C	PL16D	PL17D	PL21D	PL25A	I/O-A14
47	See Note	PL12D	PL13D	PL15D	PL17D	PL18D	PL22D	PL27D	I/O
48	PL10C	PL12C	PL13A	PL15A	PL17A	PL19D	PL23D	PL28D	I/O
49	PL10B	PL12B	PL14D	PL16D	PL18C	PL19A	PL23A	PL28A	I/O
50	PL10A	PL12A	PL14A	PL16A	PL18A	PL20A	PL24A	PL30A	I/O-A15
51	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
52	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK	CCLK
53	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
54	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
55	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	PB1A	I/O-A16
56	See Note	PB1B	PB1D	PB1D	PB1D	PB2A	PB2A	PB3A	I/O
57	PB1B	PB1C	PB2A	PB2A	PB2A	PB2D	PB2D	PB3D	I/O-VDD5
58	PB1C	PB1D	PB2D	PB2D	PB2D	PB3D	PB3D	PB4D	I/O
59	PB1D	PB2A	PB3A	PB3B	PB3D	PB4D	PB4D	PB5D	I/O-A17
60	See Note	PB2D	PB3D	PB4D	PB4D	PB5D	PB5D	PB6D	I/O
61	PB2A	PB3A	PB4A	PB5A	PB5B	PB6B	PB6B	PB7D	I/O
62	PB2B	PB3B	PB4B	PB5B	PB5D	PB6D	PB6D	PB8D	I/O
63	PB2C	PB3C	PB4C	PB5C	PB6B	PB7B	PB7B	PB9D	I/O
64	PB2D	PB3D	PB4D	PB5D	PB6D	PB7D	PB7D	PB10D	I/O
65	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
66	PB3A	PB4A	PB5A	PB6A	PB7A	PB8A	PB8A	PB11A	I/O
67	PB3B	PB4B	PB5B	PB6B	PB7B	PB8B	PB8D	PB11D	I/O
68	PB3C	PB4C	PB5C	PB6C	PB7C	PB8C	PB9A	PB12A	I/O
69	PB3D	PB4D	PB5D	PB6D	PB7D	PB8D	PB9D	PB12D	I/O
70	PB4A	PB5A	PB6A	PB7A	PB8A	PB9A	PB10A	PB13A	I/O
71	PB4B	PB5B	PB6B	PB7B	PB8B	PB9B	PB10D	PB13D	I/O
72	PB4C	PB5C	PB6C	PB7C	PB8C	PB9C	PB11A	PB14A	I/O
73	PB4D	PB5D	PB6D	PB7D	PB8D	PB9D	PB11D	PB14D	I/O
74	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
75	PB5A	PB6A	PB7A	PB8A	PB9A	PB10A	PB12A	PB15A	I/O
76	PB5B	PB6B	PB7B	PB8B	PB9B	PB10B	PB12B	PB15B	I/O
77	PB5C	PB6C	PB7C	PB8C	PB9C	PB10C	PB12C	PB15C	I/O
78	PB5D	PB6D	PB7D	PB8D	PB9D	PB10D	PB12D	PB15D	I/O
79	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
80	PB6A	PB7A	PB8A	PB9A	PB10A	PB11A	PB13A	PB16A	I/O
81	PB6B	PB7B	PB8B	PB9B	PB10B	PB11B	PB13B	PB16B	I/O
82	PB6C	PB7C	PB8C	PB9C	PB10C	PB11C	PB13C	PB16C	I/O
83	PB6D	PB7D	PB8D	PB9D	PB10D	PB11D	PB13D	PB16D	I/O
84	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
85	PB7A	PB8A	PB9A	PB10A	PB11A	PB12A	PB14A	PB17A	I/O-VDD5
86	PB7B	PB8B	PB9B	PB10B	PB11B	PB12B	PB14D	PB17D	I/O

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 24. OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 240-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
169	PR3D	PR4D	PR4D	PR5D	PR6D	PR6D	PR9D	I/O
170	PR2A	PR3A	PR3A	PR4A	PR5A	PR5A	PR8A	I/O-$\overline{RD}$
171	PR2B	PR3B	PR3B	PR4B	PR5B	PR5B	PR7A	I/O
172	PR2C	PR3C	PR3C	PR4D	PR5D	PR5D	PR6A	I/O
173	PR2D	PR3D	PR3D	PR3A	PR4A	PR4A	PR5A	I/O
174	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
175	PR1A	PR2A	PR2A	PR2A	PR3A	PR3A	PR4A	I/O-$\overline{WR}$
176	PR1B	PR2D	PR2D	PR2C	PR2A	PR2A	PR3A	I/O
177	PR1C	PR1A	PR1A	PR1A	PR1A	PR1A	PR2A	I/O
178	PR1D	PR1D	PR1D	PR1D	PR1D	PR1D	PR1D	I/O
179	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
180	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
181	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
182	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
183	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
184	PT12D	PT14D	PT16D	PT18D	PT20D	PT24D	PT30D	I/O
185	PT12C	PT14C	PT16C	PT18B	PT20A	PT24A	PT29A	I/O
186	PT12B	PT14A	PT16A	PT18A	PT19D	PT23D	PT28D	I/O
187	PT12A	PT13D	PT15D	PT17D	PT19A	PT23A	PT28A	I/O-RDY/RCLK
188	VSS	See Note	See Note	VSS	VSS	VSS	VSS	VSS
189	PT11D	PT13B	PT15B	PT16D	PT17D	PT21D	PT26D	I/O
190	PT11C	PT13A	PT15A	PT16C	PT17C	PT21C	PT26C	I/O
191	PT11B	PT12D	PT14D	PT16A	PT17A	PT21A	PT26A	I/O
192	PT11A	PT12C	PT13D	PT15D	PT16D	PT20D	PT25D	I/O-D7
193	PT10D	PT12A	PT13B	PT14D	PT15D	PT19D	PT24D	I/O-VDD5
194	PT10C	PT11D	PT13A	PT14A	PT15A	PT19A	PT23D	I/O
195	PT10B	PT11C	PT12D	PT13D	PT14D	PT18D	PT22D	I/O
196	PT10A	PT11B	PT12B	PT13B	PT14B	PT18B	PT21D	I/O-D6
197	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
198	PT9D	PT10D	PT11D	PT12D	PT13D	PT17D	PT20D	I/O
199	PT9C	PT10C	PT11C	PT12C	PT13C	PT17A	PT20A	I/O
200	PT9B	PT10B	PT11B	PT12B	PT13B	PT16D	PT19D	I/O
201	PT9A	PT10A	PT11A	PT12A	PT13A	PT16A	PT19A	I/O-D5
202	PT8D	PT9D	PT10D	PT11D	PT12D	PT15D	PT18D	I/O
203	PT8C	PT9C	PT10C	PT11C	PT12C	PT15A	PT18A	I/O
204	PT8B	PT9B	PT10B	PT11B	PT12B	PT14D	PT17D	I/O
205	PT8A	PT9A	PT10A	PT11A	PT12A	PT14A	PT17A	I/O-D4
206	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
207	PT7D	PT8D	PT9D	PT10D	PT11D	PT13D	PT16D	I/O
208	PT7C	PT8C	PT9C	PT10C	PT11C	PT13C	PT16C	I/O
209	PT7B	PT8B	PT9B	PT10B	PT11B	PT13B	PT16B	I/O
210	PT7A	PT8A	PT9A	PT10A	PT11A	PT13A	PT16A	I/O-D3

Notes:
The OR2C/2T08A and OR2C/2T10A do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 26. OR2C12A, OR2C15A, OR2C26A, and OR2C40A 304-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C12A Pad	2C15A Pad	2C26A Pad	2C40A Pad	Function
135	PB14B	PB15B	PB19B	PB24A	I/O
136	PB14D	PB15D	PB19D	PB24D	I/O
137	PB15A	PB16A	PB20A	PB25A	I/O-$\overline{\text{INIT}}$
138	PB15D	PB16D	PB20D	PB25D	I/O
139	PB16A	PB17A	PB21A	PB26A	I/O
140	PB16D	PB17D	PB21D	PB26D	I/O
141	VSS	VSS	VSS	VSS	VSS
142	PB17A	PB18A	PB22A	PB27A	I/O
143	PB17B	PB18B	PB22B	PB27B	I/O
144	PB17C	PB18D	PB22D	PB27D	I/O
145	PB17D	PB19A	PB23A	PB28A	I/O
146	PB18A	PB19D	PB23D	PB28D	I/O
147	PB18B	PB20A	PB24A	PB29A	I/O
148	PB18C	PB20B	PB24B	PB29D	I/O
149	PB18D	PB20D	PB24D	PB30D	I/O
150	VSS	VSS	VSS	VSS	VSS
151	DONE	DONE	DONE	DONE	DONE
152	VDD	VDD	VDD	VDD	VDD
153	VSS	VSS	VSS	VSS	VSS
154	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
155	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
156	PR18A	PR20A	PR24A	PR30A	I/O-M0
157	PR18B	PR20C	PR24C	PR29A	I/O
158	PR18C	PR20D	PR24D	PR29D	I/O
159	PR18D	PR19A	PR23A	PR28A	I/O
160	PR17A	PR19D	PR23D	PR28D	I/O
161	PR17B	PR18A	PR22A	PR27A	I/O
162	PR17C	PR18B	PR22B	PR27B	I/O
163	PR17D	PR18D	PR22D	PR27D	I/O
164	VSS	VSS	VSS	VSS	VSS
165	PR16A	PR17A	PR21A	PR26A	I/O
166	PR16D	PR17D	PR21D	PR25A	I/O
167	PR15A	PR16A	PR20A	PR24A	I/O
168	PR15C	PR16C	PR20C	PR24D	I/O
169	PR15D	PR16D	PR20D	PR23D	I/O-M1
170	PR14A	PR15A	PR19A	PR22A	I/O
171	PR14C	PR15C	PR19C	PR22C	I/O
172	PR14D	PR15D	PR19D	PR22D	I/O
173	PR13A	PR14A	PR18A	PR21A	I/O
174	PR13C	PR14C	PR18C	PR21C	I/O
175	PR13D	PR14D	PR18D	PR21D	I/O
176	VDD	VDD	VDD	VDD	VDD
177	PR12A	PR13A	PR17A	PR20A	I/O-M2
178	PR12B	PR13B	PR17D	PR20D	I/O
179	PR12C	PR13C	PR16A	PR19A	I/O

Note: The OR2TxxA and OR2TxxB series are not offered in the 304-pin SQFP/SQFP2 packages.

Pin Information (continued)

Table 26. OR2C12A, OR2C15A, OR2C26A, and OR2C40A 304-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C12A Pad	2C15A Pad	2C26A Pad	2C40A Pad	Function
180	PR12D	PR13D	PR16D	PR19D	I/O
181	PR11A	PR12A	PR15A	PR18A	I/O-M3
182	PR11B	PR12B	PR15D	PR18D	I/O
183	PR11C	PR12C	PR14A	PR17A	I/O
184	PR11D	PR12D	PR14D	PR17D	I/O
185	VSS	VSS	VSS	VSS	VSS
186	PR10A	PR11A	PR13A	PR16A	I/O
187	PR10B	PR11B	PR13B	PR16B	I/O
188	PR10C	PR11C	PR13C	PR16C	I/O
189	PR10D	PR11D	PR13D	PR16D	I/O
190	VDD	VDD	VDD	VDD	VDD
191	PR9A	PR10A	PR12A	PR15A	I/O
192	PR9B	PR10B	PR12B	PR15B	I/O
193	PR9C	PR10C	PR12C	PR15C	I/O
194	PR9D	PR10D	PR12D	PR15D	I/O
195	VSS	VSS	VSS	VSS	VSS
196	PR8A	PR9A	PR11A	PR14A	I/O
197	PR8B	PR9B	PR11D	PR14D	I/O
198	PR8C	PR9C	PR10A	PR13A	I/O
199	PR8D	PR9D	PR10D	PR13D	I/O
200	PR7A	PR8A	PR9A	PR12A	I/O-CS1
201	PR7B	PR8B	PR9D	PR12D	I/O
202	PR7C	PR8C	PR8A	PR11A	I/O
203	PR7D	PR8D	PR8D	PR11D	I/O
204	VDD	VDD	VDD	VDD	VDD
205	PR6A	PR7A	PR7A	PR10A	I/O-$\overline{CS0}$
206	PR6B	PR7B	PR7B	PR10B	I/O
207	PR6C	PR7C	PR7C	PR10C	I/O
208	PR6D	PR7D	PR7D	PR10D	I/O
209	PR5A	PR6A	PR6A	PR9A	I/O
210	PR5B	PR6B	PR6B	PR9B	I/O
211	PR5C	PR6C	PR6C	PR9C	I/O
212	PR5D	PR6D	PR6D	PR9D	I/O
213	PR4A	PR5A	PR5A	PR8A	I/O-$\overline{RD}$
214	PR4B	PR5B	PR5B	PR7A	I/O
215	PR4D	PR5D	PR5D	PR6A	I/O
216	PR3A	PR4A	PR4A	PR5A	I/O
217	VSS	VSS	VSS	VSS	VSS
218	PR2A	PR3A	PR3A	PR4A	I/O-$\overline{WR}$
219	PR2B	PR3B	PR3B	PR4B	I/O
220	PR2C	PR2A	PR2A	PR3A	I/O
221	PR2D	PR2D	PR2D	PR3D	I/O
222	PR1A	PR1A	PR1A	PR2A	I/O
223	PR1B	PR1B	PR1B	PR2D	I/O
224	PR1C	PR1C	PR1C	PR1A	I/O

Note: The OR2TxxA and OR2TxxB series are not offered in the 304-pin SQFP/SQFP2 packages.

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
AD13	PB9D	PB10D	PB11D	PB13D	PB16D	I/O
AE15	PB10A	PB11A	PB12A	PB14A	VDD5	I/O-VDD5
AD14	PB10B	PB11B	PB12B	PB14D	PB17D	I/O
AF15	PB10C	PB11C	PB12C	PB15A	PB18A	I/O
AE16	PB10D	PB11D	PB12D	PB15D	PB18D	I/O
AD15	PB11A	PB12A	PB13A	PB16A	PB19A	I/O-HDC
AF16	PB11B	PB12B	PB13B	PB16D	PB19D	I/O
AC15	PB11C	PB12C	PB13C	PB17A	PB20A	I/O
AE17	PB11D	PB12D	PB13D	PB17D	PB20D	I/O
AD16	PB12A	PB13A	PB14A	PB18A	PB21A	I/O-$\overline{\text{LDC}}$
AF17	PB12B	PB13B	PB14B	PB18B	PB21D	I/O
AC17	PB12C	PB13C	PB14C	PB18C	PB22A	I/O
AE18	PB12D	PB13D	PB14D	PB18D	PB22D	I/O
AD17	PB13A	PB14A	PB15A	PB19A	PB23A	I/O
AF18	PB13B	PB14B	PB15B	PB19B	PB24A	I/O
AE19	—	PB14C	PB15C	PB19C	PB24C	I/O
AF19	PB13C	PB14D	PB15D	PB19D	PB24D	I/O
AD18	PB13D	PB15A	PB16A	PB20A	PB25A	I/O-$\overline{\text{INIT}}$
AE20	—	PB15B	PB16B	PB20B	PB25B	I/O
AC19	PB14A	PB15C	PB16C	PB20C	PB25C	I/O
AF20	—	PB15D	PB16D	PB20D	PB25D	I/O
AD19	PB14B	PB16A	PB17A	PB21A	VDD5	I/O-VDD5
AE21	PB14C	PB16B	PB17B	PB21B	PB26B	I/O
AC20	PB14D	PB16C	PB17C	PB21C	PB26C	I/O
AF21	PB15A	PB16D	PB17D	PB21D	PB26D	I/O
AD20	PB15B	PB17A	PB18A	PB22A	PB27A	I/O
AE22	PB15C	PB17B	PB18B	PB22B	PB27B	I/O
AF22	PB15D	PB17C	PB18D	PB22D	PB27D	I/O
AD21	PB16A	PB17D	PB19A	PB23A	PB28A	I/O
AE23	—	—	PB19C	PB23B	PB28B	I/O
AC22	PB16B	PB18A	PB19D	PB23D	PB28D	I/O
AF23	PB16C	PB18B	PB20A	PB24A	PB29A	I/O
AD22	PB16D	PB18C	PB20B	PB24B	PB29D	I/O
AE24	—	—	PB20C	PB24C	PB30C	I/O
AD23	—	PB18D	PB20D	PB24D	PB30D	I/O
AF24	DONE	DONE	DONE	DONE	PDONE	DONE
AE26	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	PRESETN	$\overline{\text{RESET}}$
AD25	$\overline{\text{PRGM}}$	PRGM	$\overline{\text{PRGM}}$	PRGM	PPRGMN	$\overline{\text{PRGM}}$
AD26	PR16A	PR18A	PR20A	PR24A	PR30A	I/O-M0

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	*2C10A Pad*	*2C12A Pad*	*2C/2T15A/B Pad*	*2T26A Pad*	*OR2T40A/B Pad*	*Function*
N24	PR7A	PR8A	PR9A	PR11A	$V_{DD}5$	I/O-$V_{DD}5$
M26	PR7B	PR8B	PR9B	PR11D	PR14D	I/O
L25	PR7C	PR8C	PR9C	PR10A	PR13A	I/O
M24	PR7D	PR8D	PR9D	PR10D	PR13D	I/O
L26	PR6A	PR7A	PR8A	PR9A	PR12A	I/O-CS1
M23	PR6B	PR7B	PR8B	PR9D	PR12D	I/O
K25	PR6C	PR7C	PR8C	PR8A	PR11A	I/O
L24	PR6D	PR7D	PR8D	PR8D	PR11D	I/O
K26	PR5A	PR6A	PR7A	PR7A	PR10A	I/O-$\overline{CS0}$
K23	PR5B	PR6B	PR7B	PR7B	PR10B	I/O
J25	PR5C	PR6C	PR7C	PR7C	PR10C	I/O
K24	PR5D	PR6D	PR7D	PR7D	PR10D	I/O
J26	PR4A	PR5A	PR6A	PR6A	PR9A	I/O
H25	PR4B	PR5B	PR6B	PR6B	PR9B	I/O
H26	PR4C	PR5C	PR6C	PR6C	PR9C	I/O
J24	PR4D	PR5D	PR6D	PR6D	PR9D	I/O
G25	PR3A	PR4A	PR5A	PR5A	PR8A	I/O-$\overline{RD}$
H23	PR3B	PR4B	PR5B	PR5B	PR7A	I/O
G26	—	PR4C	PR5C	PR5C	PR7C	I/O
H24	PR3C	PR4D	PR5D	PR5D	PR6A	I/O
F25	PR3D	PR3A	PR4A	PR4A	$V_{DD}5$	I/O-$V_{DD}5$
G23	—	PR3B	PR4B	PR4B	PR5B	I/O
F26	—	PR3C	PR4C	PR4C	PR5C	I/O
G24	—	PR3D	PR4D	PR4D	PR5D	I/O
E25	PR2A	PR2A	PR3A	PR3A	PR4A	I/O-$\overline{WR}$
E26	PR2B	PR2B	PR3B	PR3B	PR4B	I/O
F24	—	—	PR3D	PR3D	PR4D	I/O
D25	PR2C	PR2C	PR2A	PR2A	PR3A	I/O
E23	PR2D	PR2D	PR2D	PR2D	PR3D	I/O
D26	PR1A	PR1A	PR1A	PR1A	PR2A	I/O
E24	PR1B	PR1B	PR1B	PR1B	PR2D	I/O
C25	PR1C	PR1C	PR1C	PR1C	PR1A	I/O
D24	PR1D	PR1D	PR1D	PR1D	PR1D	I/O
C26	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
A25	PT16D	PT18D	PT20D	PT24D	PT30D	I/O
B24	PT16C	PT18C	PT20C	PT24C	PT30A	I/O
A24	—	—	PT20B	PT24B	PT29B	I/O
B23	PT16B	PT18B	PT20A	PT24A	PT29A	I/O
C23	PT16A	PT18A	PT19D	PT23D	PT28D	I/O

Notes:
The pins labeled I/O-$V_{DD}5$ are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to $V_{DD}5$ for the OR2TxxA series.

The pins labeled V_{SS}-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
L4	VDD	VDD	VDD	VDD	VDD	VDD
T23	VDD	VDD	VDD	VDD	VDD	VDD
T4	VDD	VDD	VDD	VDD	VDD	VDD
L11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
L12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
L13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
L14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
L15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
L16	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
M16	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
N16	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
P16	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
R16	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T11	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T12	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T13	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T14	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T15	VSS	VSS	VSS	VSS	VSS	VSS—ETC
T16	VSS	VSS	VSS	VSS	VSS	VSS—ETC

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
AH27	PB1A	PB1A	PB1A	I/O-A16
AJ28	PB1B	PB1B	PB1B	I/O
AK28	PB1C	PB1C	PB2A	I/O
AL28	PB1D	PB1D	PB2D	I/O
AH26	PB2A	PB2A	PB3A	I/O
AJ27	PB2B	PB2B	PB3B	I/O
AK27	PB2C	PB2C	PB3C	I/O
AL27	PB2D	PB2D	PB3D	I/O-VDD5
AJ26	PB3A	PB3A	PB4A	I/O
AK26	PB3B	PB3B	PB4B	I/O
AL26	PB3C	PB3C	PB4C	I/O
AH24	PB3D	PB3D	PB4D	I/O
AJ25	PB4A	PB4A	PB5A	I/O
AK25	PB4B	PB4B	PB5B	I/O
AL25	PB4C	PB4C	PB5C	I/O
AH23	PB4D	PB4D	PB5D	I/O-A17
AJ24	PB5A	PB5A	PB6A	I/O
AK24	PB5B	PB5B	PB6B	I/O
AJ23	PB5C	PB5C	PB6C	I/O
AH22	PB5D	PB5D	PB6D	I/O
AK23	PB6A	PB6A	PB7A	I/O
AL23	PB6B	PB6B	PB7D	I/O
AJ22	PB6C	PB6C	PB8A	I/O
AK22	PB6D	PB6D	PB8D	I/O
AL22	PB7A	PB7A	PB9A	I/O
AJ21	PB7B	PB7B	PB9D	I/O
AH20	PB7C	PB7C	PB10A	I/O
AK21	PB7D	PB7D	PB10D	I/O
AL21	—	PB8A	PB11A	I/O-VDD5
AJ20	PB8A	PB8B	PB11B	I/O
AH19	PB8B	PB8D	PB11D	I/O
AK20	PB8C	PB9A	PB12A	I/O
AJ19	—	PB9B	PB12B	I/O
AK19	PB8D	PB9D	PB12D	I/O
AH18	PB9A	PB10A	PB13A	I/O
AL19	PB9B	PB10D	PB13D	I/O
AJ18	PB9C	PB11A	PB14A	I/O
AK18	—	PB11B	PB14B	I/O
AL18	PB9D	PB11D	PB14D	I/O
AJ17	PB10A	PB12A	PB15A	I/O
AK17	PB10B	PB12B	PB15B	I/O
AL17	PB10C	PB12C	PB15C	I/O
AJ16	PB10D	PB12D	PB15D	I/O
AH16	PB11A	PB13A	PB16A	I/O

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
B4	PT20B	PT24B	PT29B	I/O
A4	PT20A	PT24A	PT29A	I/O
D6	PT19D	PT23D	PT28D	I/O
C5	PT19C	PT23C	PT28C	I/O
B5	PT19B	PT23B	PT28B	I/O
A5	PT19A	PT23A	PT28A	I/O-RDY/RCLK
C6	PT18D	PT22D	PT27D	I/O
B6	PT18C	PT22C	PT27C	I/O
A6	PT18B	PT22B	PT27B	I/O
D8	PT18A	PT22A	PT27A	I/O
C7	PT17D	PT21D	PT26D	I/O
B7	PT17C	PT21C	PT26C	I/O
A7	PT17B	PT21B	PT26B	I/O
D9	PT17A	PT21A	PT26A	I/O
C8	PT16D	PT20D	PT25D	I/O-D7
B8	PT16C	PT20C	PT25C	I/O
C9	PT16B	PT20B	PT25B	I/O
D10	PT16A	PT20A	PT25A	I/O
B9	PT15D	PT19D	PT24D	I/O-VDD5
A9	PT15C	PT19C	PT24C	I/O
C10	PT15B	PT19B	PT24B	I/O
B10	PT15A	PT19A	PT23D	I/O
A10	PT14D	PT18D	PT22D	I/O
C11	PT14C	PT18C	PT22A	I/O
D12	PT14B	PT18B	PT21D	I/O-D6
B11	PT14A	PT18A	PT21A	I/O
A11	PT13D	PT17D	PT20D	I/O
C12	PT13C	PT17A	PT20A	I/O
D13	—	PT16D	PT19D	I/O-VDD5
B12	PT13B	PT16B	PT19B	I/O
C13	PT13A	PT16A	PT19A	I/O-D5
B13	PT12D	PT15D	PT18D	I/O
D14	—	PT15B	PT18B	I/O
A13	PT12C	PT15A	PT18A	I/O
C14	PT12B	PT14D	PT17D	I/O
B14	—	PT14B	PT17B	I/O
A14	PT12A	PT14A	PT17A	I/O-D4
C15	PT11D	PT13D	PT16D	I/O
B15	PT11C	PT13C	PT16C	I/O
A15	PT11B	PT13B	PT16B	I/O
C16	PT11A	PT13A	PT16A	I/O-D3
D16	PT10D	PT12D	PT15D	I/O
B16	PT10C	PT12C	PT15C	I/O
A17	PT10B	PT12B	PT15B	I/O-VDD5

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Timing Characteristics (continued)

Table 35A. OR2CxxA and OR2TxxA Asynchronous Memory Read Characteristics (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Operation (TJ = 85 °C, VDD = min):												
Read Cycle Time	TRC	3.6	—	2.7	—	2.4	—	2.3	—	2.0	—	ns
Data Valid after Address (A[3:0], B[3:0] to F[3:0])	MEM*_ADEL	—	2.8	—	2.1	—	1.7	—	1.4	—	1.3	ns
Read Operation, Clocking Data into Latch/Flip-flop (TJ = 85 °C, VDD = min):												
Address to Clock Setup Time (A[3:0], B[3:0] to CK)	MEM*_ASET	1.8	—	1.2	—	1.1	—	1.0	—	1.0	—	ns
Clock to PFU Out (CK to Q[3:0])—Register	REG_DEL	—	2.0	—	1.9	—	1.5	—	1.3	—	1.0	ns

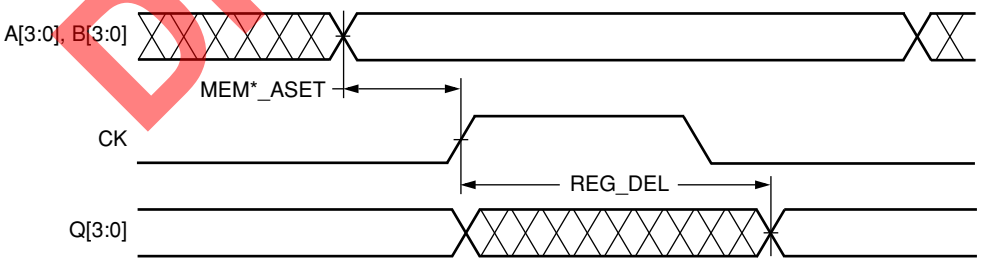
Table 35B. OR2TxxB Asynchronous Memory Read Characteristics (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Read Operation (TJ = 85 °C, VDD = min):						
Read Cycle Time	TRC	1.9	—	1.8	—	ns
Data Valid after Address (A[3:0], B[3:0] to F[3:0])	MEM*_ADEL	—	1.3	—	1.0	ns
Read Operation, Clocking Data into Latch/Flip-flop (TJ = 85 °C, VDD = min):						
Address to Clock Setup Time (A[3:0], B[3:0] to CK)	MEM*_ASET	0.9	—	0.8	—	ns
Clock to PFU Out (CK to Q[3:0])—Register	REG_DEL	—	1.0	—	1.0	ns

5-3226(F).r4

Figure 55. Read Operation—Flip-Flop Bypass



5-3227(F).r4

Figure 56. Read Operation—LUT Memory Loading Flip-Flops

Timing Characteristics (continued)

Table 37A. OR2CxxA and OR2TxxA Asynchronous Memory Read During Write Operation (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C. OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read During Write Operation (TJ = 85 °C, VDD = min):												
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.9	—	4.8	—	3.9	—	4.0	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	6.4	—	5.8	—	4.7	—	4.7	—	4.5	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	3.6	—	3.1	—	2.5	—	2.5	—	2.2	ns

Table 37B. OR2TxxB Asynchronous Memory Read During Write Operation (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Read During Write Operation (TJ = +85 °C, VDD = min):						
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.5	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	4.6	—	4.0	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	2.7	—	2.4	ns

Timing Characteristics (continued)

Table 41A. OR2CxxA and OR2TxxA PFU Output MUX, PLC BIDI, and Direct Routing Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
PFU Output MUX (TJ = 85 °C, VDD = min)												
Output MUX Delay (F[3:0]/Q[3:0] to O[4:0])	OMUX_DEL	—	0.8	—	0.6	—	0.5	—	0.4	—	0.4	ns
PLC 3-Statable BIDIs (TJ = 85 °C, VDD = min)												
BIDI Propagation Delay	TRI_DEL	—	1.0	—	0.8	—	0.7	—	0.6	—	0.5	ns
BIDI 3-state Enable/Disable Delay	TRIEN_DEL	—	1.3	—	1.0	—	0.8	—	0.8	—	0.7	ns
Direct Routing (TJ = 85 °C, VDD = min)												
PFU to PFU Delay (xSW)	DIR_DEL	—	1.1	—	0.9	—	0.7	—	0.6	—	0.6	ns
PFU Feedback (xSW)	FDBK_DEL	—	0.8	—	0.7	—	0.6	—	0.5	—	0.5	ns

Table 41B. OR2TxxB PFU Output MUX, PLC BIDI, and Direct Routing Timing Characteristics

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
PFU Output MUX (TJ = 85 °C, VDD = min)						
Output MUX Delay (F[3:0]/Q[3:0] to O[4:0])	OMUX_DEL	—	0.4	—	0.4	ns
PLC 3-Statable BIDIs (TJ = 85 °C, VDD = min)						
BIDI Propagation Delay	TRI_DEL	—	0.7	—	0.6	ns
BIDI 3-state Enable/Disable Delay	TRIEN_DEL	—	1.1	—	0.9	ns
Direct Routing (TJ = 85 °C, VDD = min)						
PFU to PFU Delay (xSW)	DIR_DEL	—	0.6	—	0.5	ns
PFU Feedback (xSW)	FDBK_DEL	—	0.4	—	0.4	ns

Timing Characteristics (continued)

Table 45A. OR2CxxA/OR2TxxA Global Input to Clock Setup/Hold Time (Pin-to-Pin)

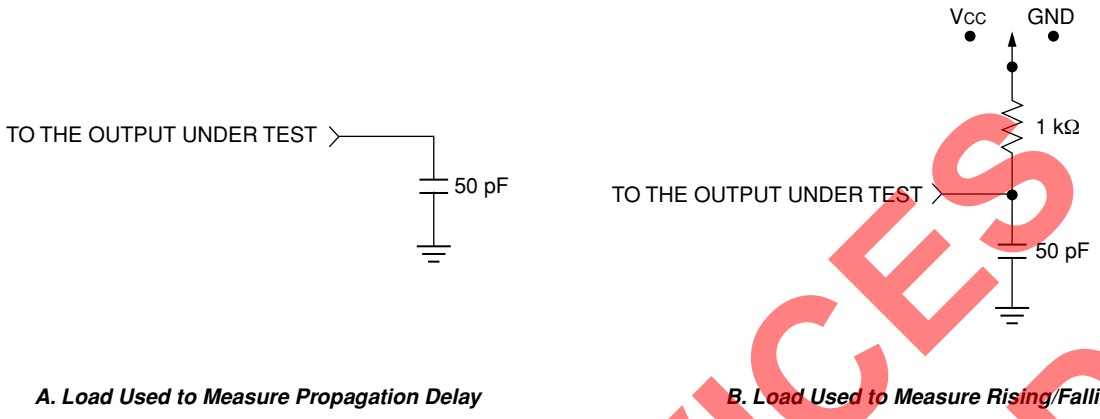
OR2CxxA Commercial: V_{DD} = 5.0 V ± 5%, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 5.0 V ± 10%, –40 °C ≤ T_A ≤ +85 °C.
OR2TxxA Commercial: V_{DD} = 3.0 V to 3.6 V, 0 °C ≤ T_A ≤ 70 °C; Industrial: V_{DD} = 3.0 V to 3.6 V, –40 °C ≤ T_A ≤ +85 °C.

Description (T_J = all, V_{DD} = all)	Device	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input to CLK (TTL/CMOS) Setup Time (no delay)	OR2C/2T04A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C06A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T08A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T10A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C12A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T15A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
	OR2C/2T26A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
	OR2C/2T40A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Input to CLK (TTL/CMOS) Setup Time (delayed)	OR2C/2T04A	5.5	—	4.2	—	4.0	—	—	—	—	—	ns
	OR2C06A	5.4	—	4.1	—	3.9	—	—	—	—	—	ns
	OR2C/2T08A	5.3	—	4.0	—	3.8	—	—	—	—	—	ns
	OR2C/2T10A	5.0	—	3.9	—	3.7	—	—	—	—	—	ns
	OR2C12A	4.9	—	3.8	—	3.6	—	—	—	—	—	ns
	OR2C/2T15A	4.7	—	3.6	—	3.4	—	4.1	—	4.1	—	ns
	OR2C/2T26A	6.9	—	6.0	—	5.7	—	6.7	—	6.0	—	ns
	OR2C/2T40A	6.4	—	5.5	—	5.2	—	6.5	—	5.8	—	ns
Input to CLK (TTL/CMOS) Hold Time (no delay)	OR2C/2T04A	4.0	—	3.8	—	3.6	—	—	—	—	—	ns
	OR2C06A	4.1	—	3.9	—	3.7	—	—	—	—	—	ns
	OR2C/2T08A	4.3	—	4.1	—	3.9	—	—	—	—	—	ns
	OR2C/2T10A	4.6	—	4.4	—	4.2	—	—	—	—	—	ns
	OR2C12A	4.8	—	4.6	—	4.4	—	—	—	—	—	ns
	OR2C/2T15A	5.1	—	4.9	—	4.7	—	4.2	—	3.7	—	ns
	OR2C/2T26A	5.8	—	5.6	—	5.3	—	4.6	—	4.1	—	ns
	OR2C/2T40A	6.8	—	6.6	—	6.3	—	5.8	—	4.9	—	ns
Input to CLK (TTL/CMOS) Hold Time (delayed)	OR2C/2T04A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C06A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T08A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T10A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C12A	0.0	—	0.0	—	0.0	—	—	—	—	—	ns
	OR2C/2T15A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
	OR2C/2T26A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
	OR2C/2T40A	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns

Notes:
The pin-to-pin timing parameters in this table should be used instead of results reported by ispLEVER.

This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay and the clock routing to the PFU CLK input. The delay will be reduced if any of the clock branches are not used. The given Setup (Delayed and No delay) and Hold (Delayed) timing allows the input clock pin to be located in any PIC on any side of the device, but direct I/O→FF routing must be used. The Hold (No delay) timing assumes the clock pin is located at one of the four center PICs and direct I/O→FF routing is used. If it is not located at one of the four center PICs, this delay must be increased by up to the following amounts: OR2C/2T04A = 5.3%, OR2C06A = 6.4%, OR2C/2T08A = 7.3%, OR2C/2T10A = 9.1%, OR2C12A = 10.8%, OR2C/2T15A = 12.2%, OR2C/2T26A = 16.1%, OR2C/2T40A = 21.2%.

Measurement Conditions

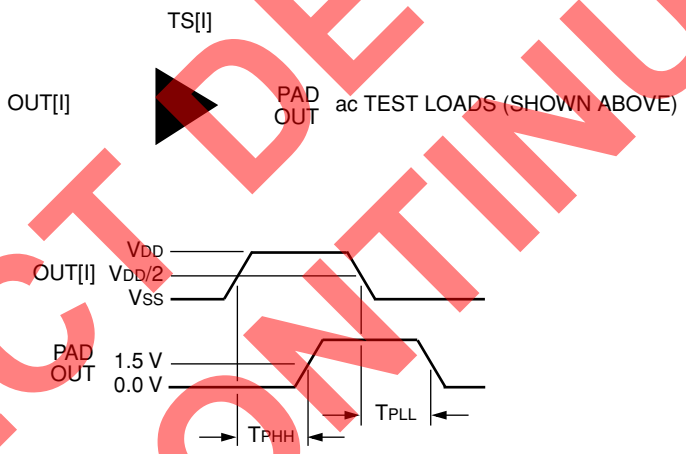


A. Load Used to Measure Propagation Delay

B. Load Used to Measure Rising/Falling Edges

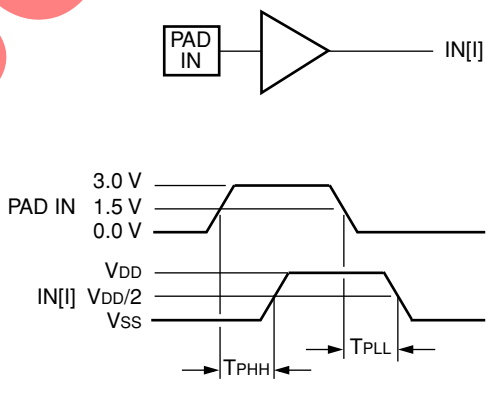
5-3234(F).r1

Figure 74. ac Test Loads



5-3233(F).ar4

Figure 75. Output Buffer Delays



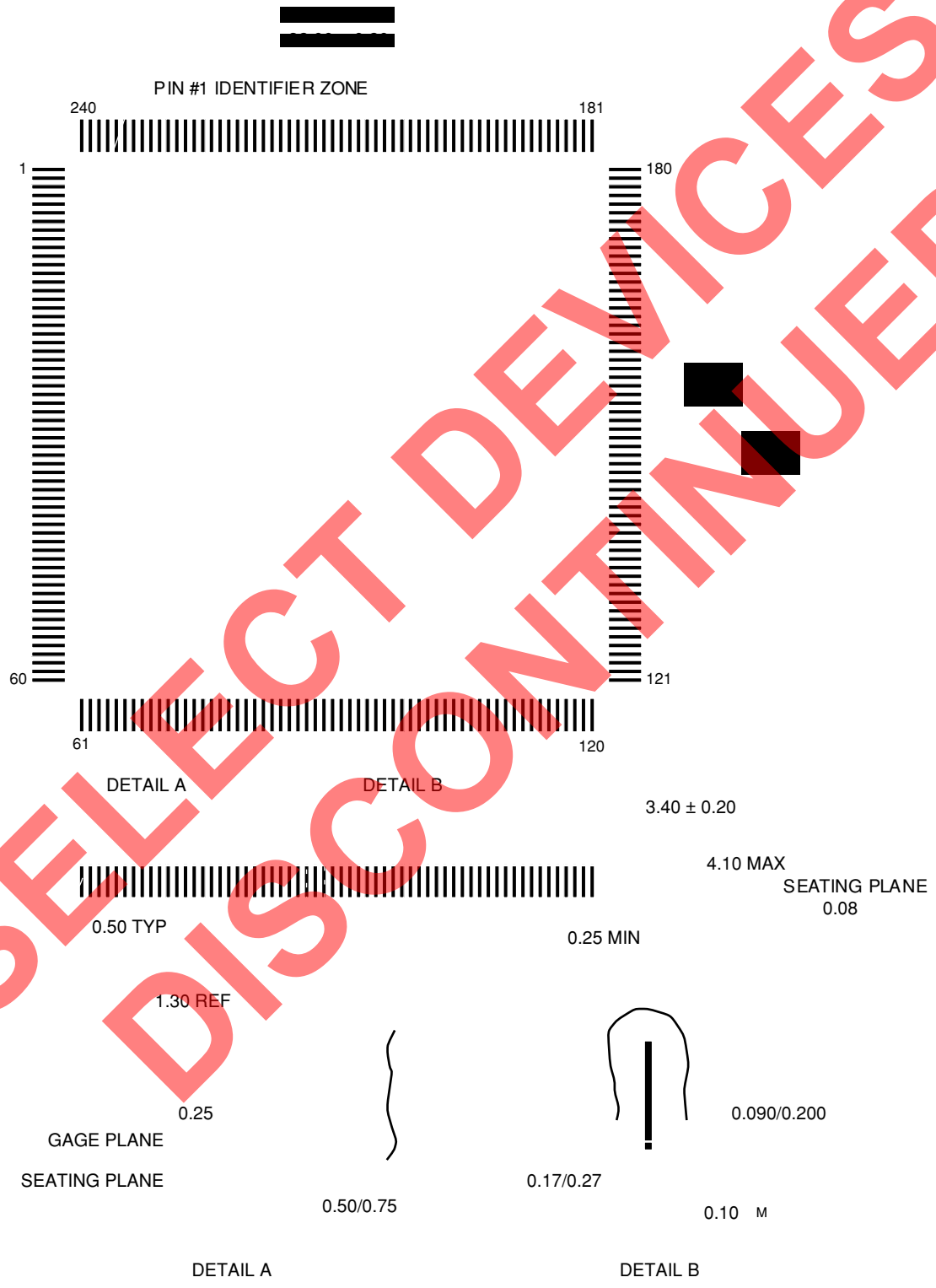
5-3235(F).a

Figure 76. Input Buffer Delays

Package Outline Drawings (continued)

240-Pin SQFP

Dimensions are in millimeters.



5-2718r.8