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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	36864
Number of I/O	171
Number of Gates	63600
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or2t26a6s208-db

ispLEVER Development System Overview

The ispLEVER development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points: at design entry and at the bit stream generation stage.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. Its bit stream generator is then used to generate the configuration data which is loaded into the FPGA's internal configuration RAM. When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, ispLEVER produces configuration data that implements the various logic and routing options discussed in this data sheet.

Architecture

The *ORCA* Series FPGA is comprised of two basic elements: PLCs and PICs. Figure 1 shows an array of programmable logic cells (PLCs) surrounded by programmable input/output cells (PICs). The Series 2 has PLCs arranged in an array of 20 rows and 20 columns. PICs are located on all four sides of the FPGA between the PLCs and the IC edge.

The location of a PLC is indicated by its row and column so that a PLC in the second row and third column is R2C3. PICs are indicated similarly, with PT (top) and PB (bottom) designating rows and PL (left) and PR (right) designating columns, followed by a number. The routing resources and configuration RAM are not shown, but the interquad routing blocks (hIQ, vIQ) present in the Series 2 series are shown.

Each PIC contains the necessary I/O buffers to interface to bond pads. The PICs also contain the routing resources needed to connect signals from the bond pads to/from PLCs. The PICs do not contain any user-accessible logic elements, such as flip-flops.

Combinatorial logic is done in look-up tables (LUTs) located in the PFU. The PFU can be used in different modes to meet different logic requirements. The LUT's configurable medium-/large-grain architecture can be used to implement from one to four combinatorial logic functions. The flexibility of the LUT to handle wide input functions, as well as multiple smaller input functions, maximizes the gate count/PFU.

The LUTs can be programmed to operate in one of three modes: combinatorial, ripple, or memory. In combinatorial mode, the LUTs can realize any four-, five-, or six-input logic functions. In ripple mode, the high-speed carry logic is used for arithmetic functions, the new multiplier function, or the enhanced data path functions. In memory mode, the LUTs can be used as a 16 x 4 read/write or read-only memory (asynchronous mode or the new synchronous mode) or a new 16 x 2 dual-port memory.

Programmable Logic Cells

The programmable logic cell (PLC) consists of a programmable function unit (PFU) and routing resources. All PLCs in the array are identical. The PFU, which contains four LUTs and four latches/FFs for logic implementation, is discussed in the next section.

Programmable Function Unit

The PFUs are used for logic. Each PFU has 19 external inputs and six outputs and can operate in several modes. The functionality of the inputs and outputs depends on the operating mode.

The PFU uses three input data buses (A[4:0], B[4:0], WD[3:0]), four control inputs (C0, CK, CE, LSR), and a carry input (CIN); the last is used for fast arithmetic functions. There is a 5-bit output bus (O[4:0]) and a carry-out (COUT).

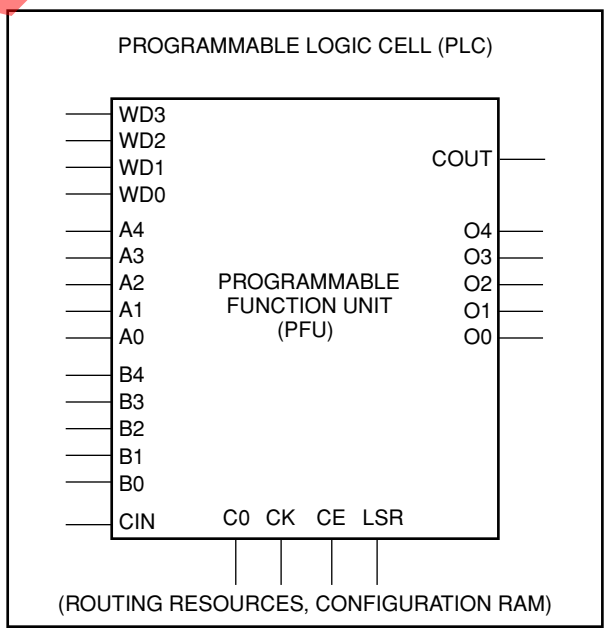

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Figure 2. PFU Ports

Programmable Logic Cells (continued)

The LUT ripple mode operation offers standard arithmetic functions, such as 4-bit adders, subtractors, adder/subtractors, and counters. In the *ORCA* Series 2, there are two new ripple modes available. The first new mode is a 4 x 1 multiplier, and the second is a 4-bit comparator. These new modes offer the advantages of faster speeds as well as denser logic capabilities.

When the LUT is configured to operate in the memory mode, a 16 x 2 asynchronous memory fits into an HLUT. Both the MA and MB modes were available in previous *ORCA* architectures, and each mode can be configured in an HLUT separately. In the Series 2, there are two new memory modes available. The first is a 16 x 4 synchronous single-port memory (SSPM), and the second is a 16 x 2 synchronous dual-port memory (SDPM). These new modes offer easier implementation, faster speeds, denser RAMs, and a dual-port capability that wasn't previously offered as an option in the ATT2Cxx/ATT2Txx families.

If the LUT is configured to operate in the ripple mode, it cannot be used for basic combinatorial logic or memory functions. In modes other than the ripple, SSPM, and SDPM modes, combinations of operating modes are possible. For example, the LUT can be configured as a 16 x 2 RAM in one HLUT and a five-input combinatorial logic function in the second HLUT. This can be done by configuring HLUTA in the MA mode and HLUTB in the F5B mode (or vice versa).

F4A/F4B Mode—Two Four-Input Functions

Each HLUT can be used to implement two four-input combinatorial functions, but the total number of inputs into each HLUT cannot exceed five. The two QLUTs within each HLUT share three inputs. In HLUTA, the A1, A2, and A3 inputs are shared by QLUT2 and QLUT3. Similarly, in HLUTB, the B1, B2, and B3 inputs are shared by QLUT0 and QLUT1. The four outputs are F0, F1, F2, and F3. The results can be routed to the D0, D1, D2, and D3 latch/FF inputs or as an output of the PFU. The use of the LUT for four functions of up to four inputs each is given in Figure 4.

F5A/F5B Mode—One Five-Input Variable Function

Each HLUT can be used to implement any five-input combinatorial function. The input ports are A[4:0] and B[4:0], and the output ports are F0 and F3. One five or less input function is input into A[4:0], and the second five or less input function is input into B[4:0]. The results are routed to the latch/FF D0 and latch/FF D3 inputs, or as a PFU output. The use of the LUT for two independent functions of up to five inputs is shown in Figure 5. In this case, the LUT is configured in the F5A and F5B modes. As a variation, the LUT can do one function of up to five input variables and two four-input functions using F5A and F4B modes or F4A and F5B modes.

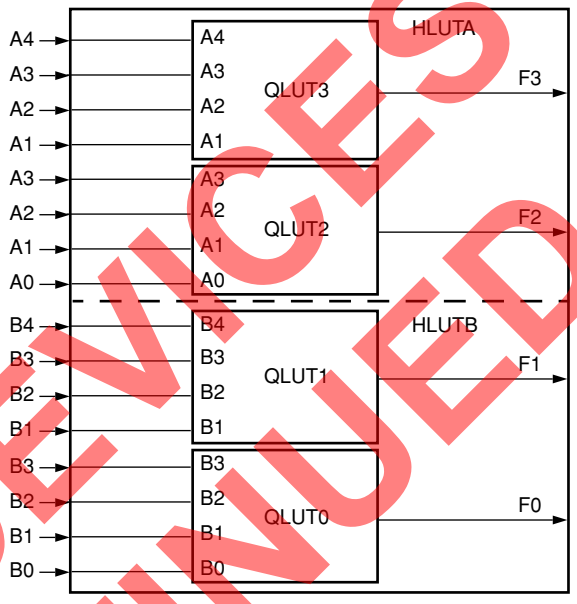


Figure 4. F4 Mode—Four Functions of Four-Input Variables

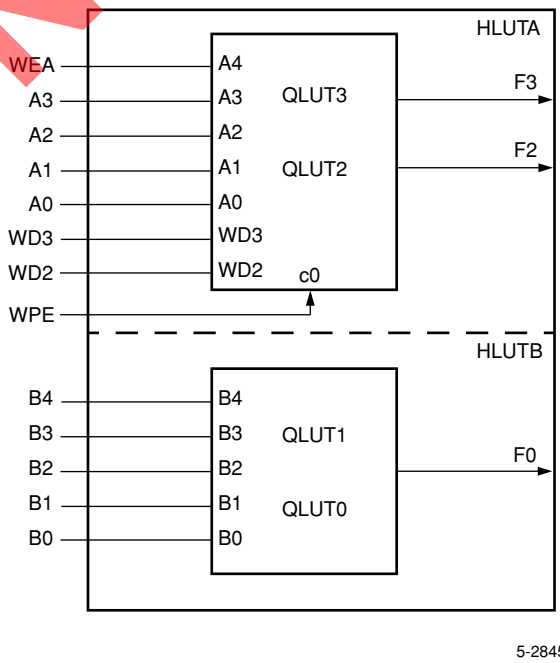


Figure 5. F5 Mode—Two Functions of Five-Input Variables

Programmable Logic Cells (continued)

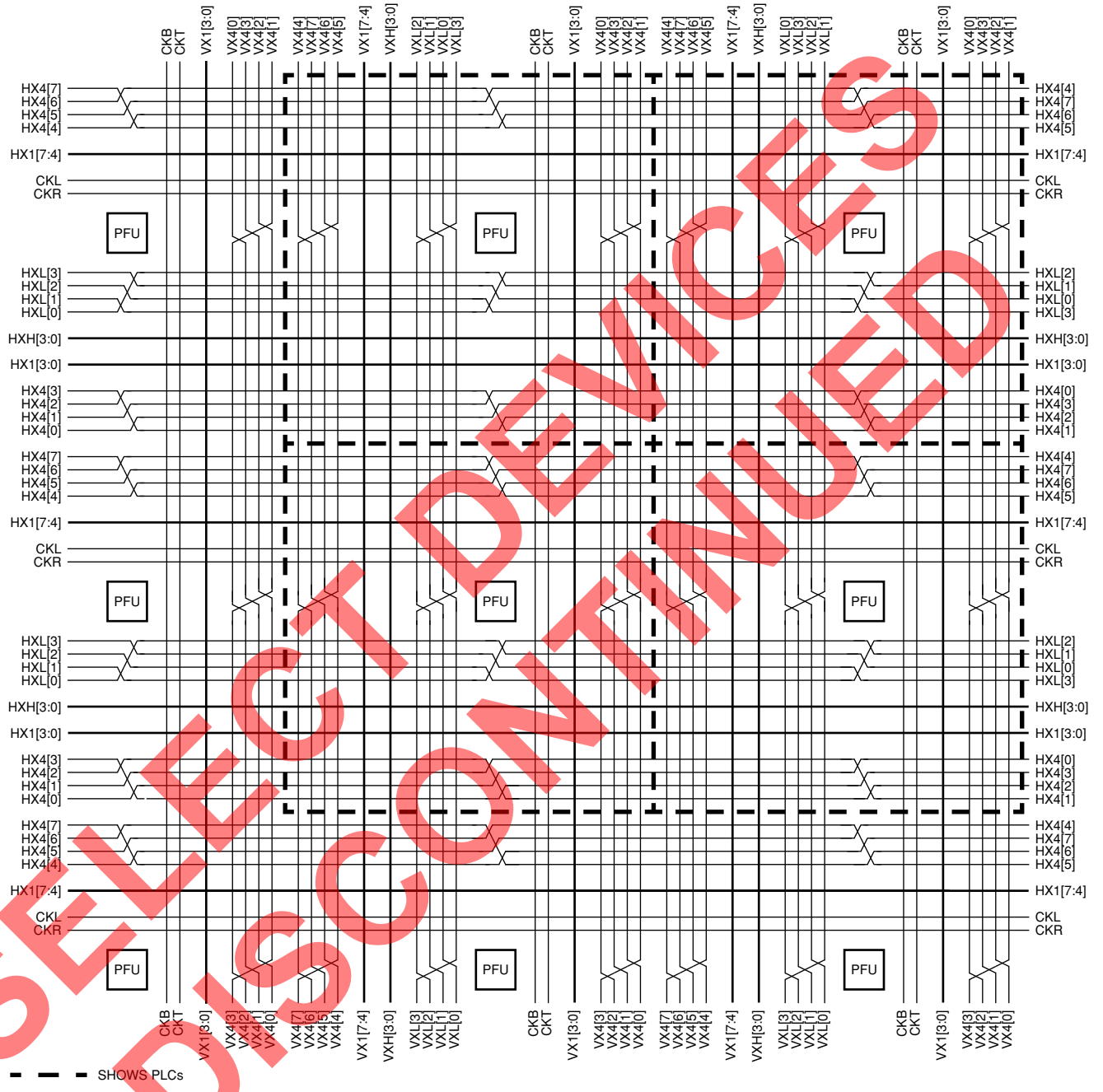


Figure 22. Multiple PLC View of Inter-PLC Routing

Programmable Logic Cells (continued)

PLC Architectural Description

Figure 23 is an architectural drawing of the PLC which reflects the PFU, the lines, and the CIPs. A discussion of each of the letters in the drawing follows.

A. These are switching lines which give the router flexibility. In general switching theory, the more levels of indirection there are in the routing, the more routable the network is. The switching lines can also connect to adjacent PLCs.

The switching lines provide direct connections to PLCs directly to the top, bottom, left, and right, without using other routing resources. The ability to disable this connection between PLCs is provided so that each side of these connections can be used exclusively as switching lines in their respective PLC.

B. These CIPs connect the X1 routing. These are located in the middle of the PLC to allow the block to connect to either the left end of the horizontal X1 line from the right or the right end of the horizontal X1 line from the left, or both. By symmetry, the same principle is used in the vertical direction. The X1 lines are not twisted, making them suitable for data paths.

C. This set of CIPs is used to connect the X1 and X4 nets to the switching lines or to other X1 and X4 nets. The CIPs on the major diagonal allow data to be transmitted from X1 nets to the switching lines without being scrambled. The CIPs on the major diagonal also allow unscrambled data to be passed between the X1 and X4 nets.

In addition to the major diagonal CIPs for the X1 lines, other CIPs provide an alternative entry path into the PLC in case the first one is already used. The other CIPs are arrayed in two patterns, as shown. Both of these patterns start with the main diagonal, but the extra CIPs are arrayed on either a parallel diagonal shifted by one or shifted by two (modulo the size of the vertical bus (5)). This allows any four application nets incident to the PLC corner to be transferred to the five switching lines in that corner. Many patterns of five nets can also be transferred.

D. The X4 lines are twisted at each PLC. One of the four X4 lines is broken with a CIP, which allows a signal to be routed a distance of four PLCs in any direction on a single line without an intermediate CIP. The X4 lines are less populated with CIPs than the X1 lines to increase their speed. A CIP can be enabled to extend an X4 line four more PLCs, and so on.

For example, if an application signal is routed onto HX4[4] in a PLC, it appears on HX4[5] in the PLC to the right. This signal step-up continues until it reaches HX4[7], two PLCs later. At this point, the user can break the connection or continue the signal for another four PLCs.

E. These symbols are bidirectional buffers (BIDIs). There are four BIDIs per PLC, and they provide signal amplification as needed to decrease signal delay. The BIDIs are also used to transmit signals on XL lines.

F. These are the BIDI and BIDIH controllers. The 3-state control signal can be disabled. They can be configured as active-high or active-low independently of each other.

G. This set of CIPs allows a BIDI to get or put a signal from one set of switching lines on each side. The BIDIs can be accessed by the switching lines. These CIPs allow a nibble of data to be routed though the BIDIs and continue to a subsequent block. They also provide an alternative routing resource to improve routability.

H. These CIPs are used to take data from/to the BIDIs to/from the XL lines. These CIPs have been optimized to allow the BIDI buffers to drive the large load usually seen when using XL lines.

I. Each latch/FF can accept data: from an LUT output; from a direct data input signal from general routing; or, as in the case of PLCs located in the two rows (columns) adjacent to PICs, directly from the pad. In addition, the LUT outputs can bypass the latches/FFs completely and output data on the general routing resources. The four inputs shown are used as the direct input to the latches/FFs from general routing resources. If the LUT is in memory mode, the four inputs WD[3:0] are the data input to the memory.

Programmable Input/Output Cells

The programmable input/output cells (PICs) are located along the perimeter of the device. Each PIC interfaces to four bond pads and contains the necessary routing resources to provide an interface between I/O pads and the PLCs. Each PIC is composed of input buffers, output buffers, and routing resources as described below. Table 6 provides an overview of the programmable functions in an I/O cell. A is a simplified diagram of the functionality of the OR2CxxA series I/O cells, while B is a simplified functional diagram of the OR2TxxA and OR2TxxB series I/O cells.

Table 6. Input/Output Cell Options

Input	***Option***
Input Levels	TTL/CMOS (OR2CxxA only) 5 V PCI compliant (OR2CxxA only) 3.3 V PCI compliant (OR2TxxA only) 3.3 V and 5 V PCI compliant (OR2TxxB only)
Input Speed	Fast/Delayed
Float Value	Pull-up/Pull-down/None
Direct-in to FF	Fast/Delayed
Output	***Option***
Output Drive	12 mA/6 mA or 6 mA/3 mA
Output Speed	Fast/Slewlim/Sinklim
Output Source	FF Direct-out/General Routing
Output Sense	Active-high/-low
3-State Sense	Active-high/-low (3-state)

Inputs

Each I/O can be configured to be either an input, an output, or bidirectional I/O. Inputs for the OR2CxxA can be configured as either TTL or CMOS compatible. The I/O for the OR2TxxA and OR2TxxB series devices are 5 V tolerant, and will be described in a later section of this data sheet. Pull-up or pull-down resistors are available on inputs to minimize power consumption.

To allow zero hold time to PLC latches/FFs, the input signal can be delayed. When enabled, this delay affects the input signal driven to general routing, but does not affect the clock input or the input lines that drive the TRIDI buffers (used to drive onto XL, XH, BIDI, and BIDIH lines).

A fast path from the input buffer to the clock lines is also provided. Any one of the four I/O pads on any PIC can be used to drive the clock line generated in that PIC. This path cannot be delayed.

To reduce the time required to input a signal into the FPGA, a dedicated path (PDIN) from the I/O pads to the PFU flip-flops is provided. Like general input signals, this signal can be configured as normal or delayed. The delayed direct input can be selected independently from the delayed general input.

Inputs should have transition times of less than 500 ns and should not be left floating. If an input can float, a pull-up or pull-down should be enabled. Floating inputs increase power consumption, produce oscillations, and increase system noise. The OR2CxxA inputs have a typical hysteresis of approximately 280 mV (200 mV for the OR2TxxA and OR2TxxB) to reduce sensitivity to input noise. The PIC contains input circuitry which provides protection against latch-up and electrostatic discharge.

Configuration Data Format (continued)

The data frames for all the Series 2 series devices are given in Table 8. An alignment field is required in the slave parallel mode for the uncompressed format. The alignment field (shown by [A]) is a series of 0s: five for the OR2C06A, OR2C10A/OR2T10A, OR2C15A/OR2T15A/OR2T15B, and OR2C26A/OR2T26A; three for the OR2C40A/OR2T40A/OR2T40B; and one for the OR2C04A/OR2T04A, OR2C08A/OR2T08A, and OR2C12A. The alignment field is not required in any other mode.

Table 8. Configuration Data Frames

OR2C04A/OR2T04A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data109:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C06A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data129:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C08A/OR2T08A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data149:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C10A/OR2T10A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data169:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C12A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data189:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C15A/OR2T15A/OR2T15B	
Uncompressed	010 opar epar [addr10:0] [A]1[Data209:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C26A/OR2T26A	
Uncompressed	010 opar epar [addr10:0] [A]1[Data249:0]111
Compressed	011 opar epar [addr10:0] 111
OR2C40A/OR2T40A/OR2T40B	
Uncompressed	010 opar epar [addr10:0] [A]1[Data315:0]111
Compressed	011 opar epar [addr10:0] 111

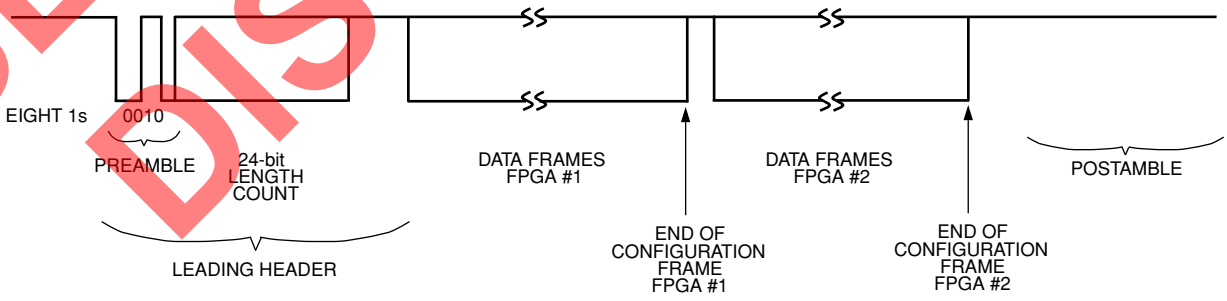


Figure 39. Serial Configuration Data Format

Special Function Blocks (continued)

ORCA Series TAP Controller (TAPC)

The *ORCA* Series TAP controller (TAPC) is a 1149.1 compatible test access port controller. The 16 JTAG state assignments from the *IEEE* 1149.1 specification are used. The TAPC is controlled by TCK and TMS. The TAPC states are used for loading the IR to allow three basic functions in testing: providing test stimuli (Update-DR), test execution (Run-Test/Idle), and obtaining test responses (Capture-DR). The TAPC allows the test host to shift in and out both instructions and test data/results. The inputs and outputs of the TAPC are provided in the table below. The outputs are primarily the control signals to the instruction register and the data register.

Table 13. TAP Controller Input/Outputs

Symbol	I/O	Function
TMS	I	Test Mode Select
TCK	I	Test Clock
PUR	I	Powerup Reset
$\overline{\text{PRGM}}$	I	BSCAN Reset
TRESET	O	Test Logic Reset
Select	O	Select IR (high); Select DR (low)
Enable	O	Test Data Out Enable
Capture-DR	O	Capture/Parallel Load DR
Capture-IR	O	Capture/Parallel Load IR
Shift-DR	O	Shift Data Register
Shift-DR	O	Shift Instruction Register
Update-DR	O	Update/Parallel Load DR
Update-IR	O	Update/Parallel Load IR

The TAPC generates control signals which allow capture, shift, and update operations on the instruction and data registers. In the capture operation, data is loaded into the register. In the shift operation, the captured data is shifted out while new data is shifted in. In the update operation, either the instruction register is loaded for instruction decode, or the boundary-scan register is updated for control of outputs.

The test host generates a test by providing input into the *ORCA* Series TMS input synchronous with TCK. This sequences the TAPC through states in order to perform the desired function on the instruction register or a data register. Figure 50 provides a diagram of the state transitions for the TAPC. The next state is determined by the TMS input value.

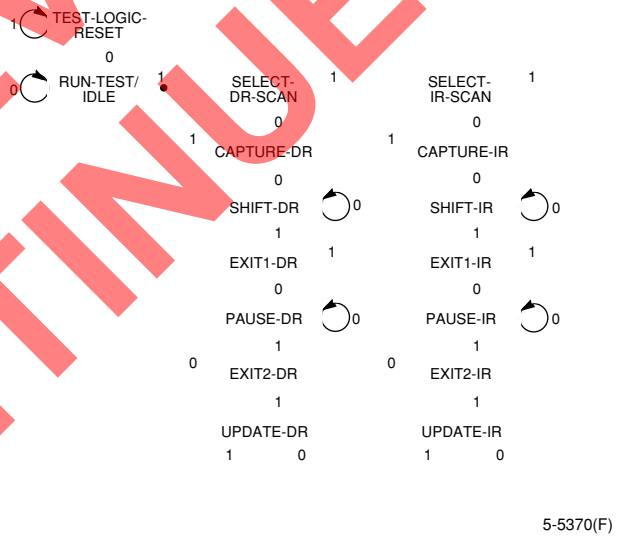


Figure 50. TAP Controller State Transition Diagram

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout

Pin	2C/2T04A Pad	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
3	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	I/O
4	PL1C	PL1A	PL2D	PL2D	PL2D	PL2D	PL2D	PL3D	I/O-A0
5	PL1B	PL2D	PL3D	PL3D	PL3D	PL4D	PL4D	PL5D	I/O-VDD5
6	See Note	PL2C	PL3C	PL3C	PL3A	PL4A	PL4A	PL6D	I/O
7	PL1A	PL2A	PL3A	PL3A	PL4A	PL5A	PL5A	PL8D	I/O-A1
8	PL2D	PL3D	PL4D	PL4A	PL5A	PL6A	PL6A	PL9A	I/O-A2
9	PL2C	PL3C	PL4C	PL5C	PL6D	PL7D	PL7D	PL10D	I/O
10	PL2B	PL3B	PL4B	PL5B	PL6B	PL7B	PL7B	PL10B	I/O
11	PL2A	PL3A	PL4A	PL5A	PL6A	PL7A	PL7A	PL10A	I/O-A3
12	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
13	PL3D	PL4D	PL5D	PL6D	PL7D	PL8D	PL8D	PL11D	I/O
14	PL3C	PL4C	PL5C	PL6C	PL7C	PL8C	PL8A	PL11A	I/O
15	PL3B	PL4B	PL5B	PL6B	PL7B	PL8B	PL9D	PL12D	I/O
16	PL3A	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL12A	I/O-A4
17	PL4D	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL13D	I/O-A5
18	PL4C	PL5C	PL6C	PL7C	PL8C	PL9C	PL10A	PL13A	I/O
19	PL4B	PL5B	PL6B	PL7B	PL8B	PL9B	PL11D	PL14D	I/O
20	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL11A	PL14A	I/O-A6
21	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
22	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL12D	PL15D	I/O
23	PL5C	PL6C	PL7C	PL8C	PL9C	PL10C	PL12C	PL15C	I/O
24	PL5B	PL6B	PL7B	PL8B	PL9B	PL10B	PL12B	PL15B	I/O
25	PL5A	PL6A	PL7A	PL8A	PL9A	PL10A	PL12A	PL15A	I/O-A7
26	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
27	PL6D	PL7D	PL8D	PL9D	PL10D	PL11D	PL13D	PL16D	I/O
28	PL6C	PL7C	PL8C	PL9C	PL10C	PL11C	PL13C	PL16C	I/O-VDD5
29	PL6B	PL7B	PL8B	PL9B	PL10B	PL11B	PL13B	PL16B	I/O
30	PL6A	PL7A	PL8A	PL9A	PL10A	PL11A	PL13A	PL16A	I/O-A8
31	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
32	PL7D	PL8D	PL9D	PL10D	PL11D	PL12D	PL14D	PL17D	I/O-A9
33	PL7C	PL8C	PL9C	PL10C	PL11C	PL12C	PL14A	PL17A	I/O
34	PL7B	PL8B	PL9B	PL10B	PL11B	PL12B	PL15D	PL18D	I/O
35	PL7A	PL8A	PL9A	PL10A	PL11A	PL12A	PL15A	PL18A	I/O-A10
36	PL8D	PL9D	PL10D	PL11D	PL12D	PL13D	PL16D	PL19D	I/O
37	PL8C	PL9C	PL10C	PL11C	PL12C	PL13C	PL16A	PL19A	I/O
38	PL8B	PL9B	PL10B	PL11B	PL12B	PL13B	PL17D	PL20D	I/O
39	PL8A	PL9A	PL10A	PL11A	PL12A	PL13A	PL17A	PL20A	I/O-A11
40	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
41	PL9D	PL10D	PL11D	PL12D	PL13D	PL14D	PL18D	PL21D	I/O-A12
42	PL9C	PL10C	PL11C	PL12C	PL13B	PL14B	PL18B	PL21B	I/O
43	PL9B	PL10B	PL11B	PL12B	PL14D	PL15D	PL19D	PL22D	I/O

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 24. OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 240-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
127	PR12D	PR13D	PR15D	PR17B	PR18A	PR22A	PR27A	I/O
128	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
129	PR11A	PR12A	PR14A	PR16A	PR17A	PR21A	PR26A	I/O
130	PR11B	PR12B	PR14C	PR16D	PR17D	PR21D	PR25A	I/O
131	PR11C	PR12C	PR14D	PR15A	PR16A	PR20A	PR24A	I/O
132	PR11D	PR12D	PR13A	PR15C	PR16C	PR20C	PR24D	I/O
133	PR10A	PR11A	PR13B	PR15D	PR16D	PR20D	PR23D	I/O-M1
134	PR10B	PR11B	PR13C	PR14A	PR15A	PR19A	PR22A	I/O
135	PR10C	PR11C	PR12A	PR14D	PR15D	PR19D	PR22D	I/O-VDD5
136	PR10D	PR11D	PR12B	PR13A	PR14A	PR18A	PR21A	I/O
137	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
138	PR9A	PR10A	PR11A	PR12A	PR13A	PR17A	PR20A	I/O-M2
139	PR9B	PR10B	PR11B	PR12B	PR13B	PR17D	PR20D	I/O
140	PR9C	PR10C	PR11C	PR12C	PR13C	PR16A	PR19A	I/O
141	PR9D	PR10D	PR11D	PR12D	PR13D	PR16D	PR19D	I/O
142	PR8A	PR9A	PR10A	PR11A	PR12A	PR15A	PR18A	I/O-M3
143	PR8B	PR9B	PR10B	PR11B	PR12B	PR15D	PR18D	I/O
144	PR8C	PR9C	PR10C	PR11C	PR12C	PR14A	PR17A	I/O
145	PR8D	PR9D	PR10D	PR11D	PR12D	PR14D	PR17D	I/O
146	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
147	PR7A	PR8A	PR9A	PR10A	PR11A	PR13A	PR16A	I/O
148	PR7B	PR8B	PR9B	PR10B	PR11B	PR13B	PR16B	I/O
149	PR7C	PR8C	PR9C	PR10C	PR11C	PR13C	PR16C	I/O
150	PR7D	PR8D	PR9D	PR10D	PR11D	PR13D	PR16D	I/O
151	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
152	PR6A	PR7A	PR8A	PR9A	PR10A	PR12A	PR15A	I/O
153	PR6B	PR7B	PR8B	PR9B	PR10B	PR12B	PR15B	I/O
154	PR6C	PR7C	PR8C	PR9C	PR10C	PR12C	PR15C	I/O
155	PR6D	PR7D	PR8D	PR9D	PR10D	PR12D	PR15D	I/O
156	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
157	PR5A	PR6A	PR7A	PR8A	PR9A	PR11A	PR14A	I/O-VDD5
158	PR5B	PR6B	PR7B	PR8B	PR9B	PR11D	PR14D	I/O
159	PR5C	PR6C	PR7C	PR8C	PR9C	PR10A	PR13A	I/O
160	PR5D	PR6D	PR7D	PR8D	PR9D	PR10D	PR13D	I/O
161	PR4A	PR5A	PR6A	PR7A	PR8A	PR9A	PR12A	I/O-CS1
162	PR4B	PR5B	PR6B	PR7B	PR8B	PR9D	PR12D	I/O
163	PR4C	PR5C	PR6C	PR7C	PR8C	PR8A	PR11A	I/O
164	PR4D	PR5D	PR6D	PR7D	PR8D	PR8D	PR11D	I/O
165	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
166	PR3A	PR4A	PR5A	PR6A	PR7A	PR7A	PR10A	I/O-$\overline{CS0}$
167	PR3B	PR4B	PR4B	PR6B	PR7B	PR7B	PR10B	I/O
168	PR3C	PR4C	PR4C	PR5B	PR6B	PR6B	PR9B	I/O

Notes:
The OR2C/2T08A and OR2C/2T10A do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 27. OR2C10A, OR2C12A, OR2C/2T15A/B, OR2T26A, and OR2T40A/B 352-Pin PBGA Pinout (continued)

Pin	2C10A Pad	2C12A Pad	2C/2T15A/B Pad	2T26A Pad	OR2T40A/B Pad	Function
A23	PT15D	PT17D	PT19A	PT23A	PT28A	I/O-RDY/ RCLK
B22	PT15C	PT17C	PT18D	PT22D	PT27D	I/O
D22	PT15B	PT17B	PT18C	PT22C	PT27C	I/O
C22	PT15A	PT17A	PT18A	PT22A	PT27A	I/O
A22	PT14D	PT16D	PT17D	PT21D	PT26D	I/O
B21	PT14C	PT16C	PT17C	PT21C	PT26C	I/O
D20	PT14B	PT16B	PT17B	PT21B	PT26B	I/O
C21	PT14A	PT16A	PT17A	PT21A	PT26A	I/O
A21	PT13D	PT15D	PT16D	PT20D	PT25D	I/O-D7
B20	—	PT15C	PT16C	PT20C	PT25C	I/O
A20	PT13C	PT15B	PT16B	PT20B	PT25B	I/O
C20	—	PT15A	PT16A	PT20A	PT25A	I/O
B19	PT13B	PT14D	PT15D	PT19D	VDD5	I/O-VDD5
D18	—	PT14C	PT15C	PT19C	PT24C	I/O
A19	PT13A	PT14B	PT15B	PT19B	PT24B	I/O
C19	—	PT14A	PT15A	PT19A	PT23D	I/O
B18	PT12D	PT13D	PT14D	PT18D	PT22D	I/O
A18	PT12C	PT13C	PT14C	PT18C	PT22A	I/O
B17	PT12B	PT13B	PT14B	PT18B	PT21D	I/O-D6
C18	PT12A	PT13A	PT14A	PT18A	PT21A	I/O
A17	PT11D	PT12D	PT13D	PT17D	PT20D	I/O
D17	PT11C	PT12C	PT13C	PT17A	PT20A	I/O
B16	PT11B	PT12B	PT13B	PT16D	PT19D	I/O
C17	PT11A	PT12A	PT13A	PT16A	PT19A	I/O-D5
A16	PT10D	PT11D	PT12D	PT15D	PT18D	I/O
B15	PT10C	PT11C	PT12C	PT15A	PT18A	I/O
A15	PT10B	PT11B	PT12B	PT14D	PT17D	I/O
C16	PT10A	PT11A	PT12A	PT14A	PT17A	I/O-D4
B14	PT9D	PT10D	PT11D	PT13D	PT16D	I/O
D15	PT9C	PT10C	PT11C	PT13C	PT16C	I/O
A14	PT9B	PT10B	PT11B	PT13B	PT16B	I/O
C15	PT9A	PT10A	PT11A	PT13A	PT16A	I/O-D3
B13	PT8D	PT9D	PT10D	PT12D	PT15D	I/O
D13	PT8C	PT9C	PT10C	PT12C	PT15C	I/O
A13	PT8B	PT9B	PT10B	PT12B	VDD5	I/O-VDD5
C14	PT8A	PT9A	PT10A	PT12A	PT15A	I/O-D2
B12	PT7D	PT8D	PT9D	PT11D	PT14D	I/O-D1
C13	PT7C	PT8C	PT9C	PT11A	PT14A	I/O

Notes:
The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 6 x 6 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
E28	PL1D	PL1D	PL1D	I/O
D29	PL1C	PL1C	PL1A	I/O
D30	PL1B	PL1B	PL2D	I/O
D31	PL1A	PL1A	PL2A	I/O
F28	PL2D	PL2D	PL3D	I/O-A0
E29	PL2C	PL2C	PL3C	I/O
E30	PL2B	PL2B	PL3B	I/O
E31	PL2A	PL2A	PL3A	I/O
F29	PL3D	PL3D	PL4D	I/O
F30	PL3C	PL3C	PL4C	I/O
F31	PL3B	PL3B	PL4B	I/O
H28	PL3A	PL3A	PL4A	I/O
G29	PL4D	PL4D	PL5D	I/O-$V_{DD}5$
G30	PL4C	PL4C	PL5C	I/O
G31	PL4B	PL4B	PL5B	I/O
J28	PL4A	PL4A	PL6D	I/O
H29	PL5D	PL5D	PL7D	I/O
H30	PL5C	PL5C	PL7C	I/O
J29	PL5B	PL5B	PL7B	I/O
K28	PL5A	PL5A	PL8D	I/O-A1
J30	PL6D	PL6D	PL9D	I/O
J31	PL6C	PL6C	PL9C	I/O
K29	PL6B	PL6B	PL9B	I/O
K30	PL6A	PL6A	PL9A	I/O-A2
K31	PL7D	PL7D	PL10D	I/O
L29	PL7C	PL7C	PL10C	I/O
M28	PL7B	PL7B	PL10B	I/O
L30	PL7A	PL7A	PL10A	I/O-A3
L31	—	PL8D	PL11D	I/O-$V_{DD}5$
M29	PL8D	PL8C	PL11C	I/O
N28	PL8C	PL8A	PL11A	I/O
M30	PL8B	PL9D	PL12D	I/O
N29	—	PL9C	PL12C	I/O
N30	PL8A	PL9A	PL12A	I/O-A4
P28	PL9D	PL10D	PL13D	I/O-A5
N31	—	PL10C	PL13C	I/O
P29	PL9C	PL10A	PL13A	I/O
P30	PL9B	PL11D	PL14D	I/O
P31	PL9A	PL11A	PL14A	I/O-A6
R29	PL10D	PL12D	PL15D	I/O
R30	PL10C	PL12C	PL15C	I/O
R31	PL10B	PL12B	PL15B	I/O
T29	PL10A	PL12A	PL15A	I/O-A7

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-$V_{DD}5$ are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to $V_{DD}5$ for the OR2TxxA series.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series FPGAs include circuitry designed to protect the chips from damaging substrate injection currents and prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	–65	150	°C
Supply Voltage with Respect to Ground	V_{DD}	–0.5	7.0	V
$V_{DD}5$ Supply Voltage with Respect to Ground (OR2TxxA)	$V_{DD}5$	V_{DD}	7.0	V
Input Signal with Respect to Ground OR2TxxA only	—	–0.5	V_{DD} + 0.3 $V_{DD}5$ + 0.3	V
Signal Applied to High-impedance Output OR2TxxA only	—	–0.5	V_{DD} + 0.3 $V_{DD}5$ + 0.3	V
Maximum Soldering Temperature	—	—	260	°C

Recommended Operating Conditions

Mode	OR2CxxA		OR2TxxA/OR2TxxB		
	Temperature Range (Ambient)	Supply Voltage (V_{DD})	Temperature Range (Ambient)	Supply Voltage (V_{DD})	Supply Voltage* ($V_{DD}5$)
Commercial	0 °C to 70 °C	5 V ± 5%	0 °C to 70 °C	3.0 V to 3.6 V	V_{DD} to 5.25 V
Industrial	–40 °C to +85 °C	5 V ± 10%	–40 °C to +85 °C	3.0 V to 3.6 V	V_{DD} to 5.25 V

Notes:
During powerup and powerdown sequencing, V_{DD} is allowed to be at a higher voltage level than $V_{DD}5$ for up to 100 ms.

During powerup sequencing of OR2TxxA devices V_{DD} should reach 1.0 V before voltage applied to $V_{DD}5$ can be greater than the voltage applied to V_{DD}.

The maximum recommended junction temperature (T_J) during operation is 125 °C.

* $V_{DD}5$ not used in OR2TxxB devices.

Timing Characteristics (continued)

Table 36A. OR2CxxA and OR2TxxA Asynchronous Memory Write Characteristics (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C. OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation (TJ = 85 °C, VDD = min):												
Write Cycle Time	TWC	7.8	—	6.3	—	5.7	—	5.2	—	5.1	—	ns
Write Enable (WREN) Pulse Width (A4/B4)	TPW	2.5	—	2.0	—	1.8	—	1.7	—	1.6	—	ns
Setup Time (TJ = 85 °C, VDD = min):												
Address to WREN (A[3:0]/B[3:0] to A4/B4)	MEM*_AWRSET	0.1	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Data to WREN (WD[3:0] to A4/B4)	MEM*_DWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Address to WPE (A[3:0]/B[3:0] to C0)	MEM*_APWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
Data to WPE (WD[3:0] to C0)	MEM*_DPWRSET	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns
WPE to WREN (C0 to A4/B4)	MEM*_WPESET	2.0	—	1.5	—	1.4	—	1.1	—	1.1	—	ns
Hold Time (TJ = all, VDD = all):												
Address from WREN (A[3:0]/B[3:0] from A4/B4)	MEM*_WRAHLD	1.7	—	1.8	—	1.6	—	1.6	—	1.5	—	ns
Data from WREN (WD[3:0] from A4/B4)	MEM*_WRDHLD	2.0	—	1.9	—	1.5	—	1.6	—	1.6	—	ns
Address from WPE (A[3:0/B[3:0] to C0)	MEM*_PWRAHLD	3.3	—	2.8	—	2.5	—	2.4	—	2.3	—	ns
Data from WPE (WD[3:0] to C0)	MEM*_PWRDHLD	3.4	—	2.9	—	2.6	—	2.4	—	2.3	—	ns
WPE from WREN (C0 from A4/B4)	MEM*_WPEHLD	0.0	—	0.0	—	0.0	—	0.0	—	0.0	—	ns

Table 36B. OR2TxxB Asynchronous Memory Write Characteristics (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Write Operation (TJ = 85 °C, VDD = min):						
Write Cycle Time	TWC	5.1	—	4.2	—	ns
Write Enable (WREN) Pulse Width (A4/B4)	TPW	1.7	—	1.4	—	ns
Setup Time (TJ = 85 °C, VDD = min):						
Address to WREN (A[3:0]/B[3:0] to A4/B4)	MEM*_AWRSET	0.0	—	0.0	—	ns
Data to WREN (WD[3:0] to A4/B4)	MEM*_DWRSET	0.0	—	0.0	—	ns
Address to WPE (A[3:0]/B[3:0] to C0)	MEM*_APWRSET	0.0	—	0.0	—	ns
Data to WPE (WD[3:0] to C0)	MEM*_DPWRSET	0.0	—	0.0	—	ns
WPE to WREN (C0 to A4/B4)	MEM*_WPESET	1.0	—	0.8	—	ns
Hold Time (TJ = all, VDD = all):						
Address from WREN (A[3:0]/B[3:0] from A4/B4)	MEM*_WRAHLD	0.9	—	0.7	—	ns
Data from WREN (WD[3:0] from A4/B4)	MEM*_WRDHLD	1.6	—	1.3	—	ns
Address from WPE (A[3:0/B[3:0] to C0)	MEM*_PWRAHLD	2.3	—	1.9	—	ns
Data from WPE (WD[3:0] to C0)	MEM*_PWRDHLD	2.3	—	1.9	—	ns
WPE from WREN (C0 from A4/B4)	MEM*_WPEHLD	0.0	—	0.0	—	ns

Timing Characteristics (continued)

Table 43A. OR2CxxA and OR2TxxA OR2CxxA/OR2TxxA Global Clock to Output Delay (Pin-to-Pin)—Output on Same Side of the Device as the Clock Pin

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C; CL = 50 pF.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C; CL = 50 pF.

Description (TJ = 85 °C, VDD = min)	Device	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CLK Input Pin → OUTPUT Pin (Fast)	OR2C/2T04A	—	10.3	—	9.8	—	8.6	—	—	—	—	ns
	OR2C06A	—	10.4	—	9.9	—	8.7	—	—	—	—	ns
	OR2C/2T08A	—	10.5	—	10.0	—	8.8	—	—	—	—	ns
	OR2C/2T10A	—	10.6	—	10.1	—	8.9	—	—	—	—	ns
	OR2C12A	—	10.7	—	10.2	—	9.0	—	—	—	—	ns
	OR2C/2T15A	—	10.8	—	10.3	—	9.1	—	8.3	—	6.7	ns
	OR2C/2T26A	—	11.0	—	10.5	—	9.2	—	8.4	—	6.9	ns
	OR2C/2T40A	—	11.4	—	10.8	—	9.5	—	8.6	—	7.0	ns
CLK Input Pin → OUTPUT Pin (Slewlim)	OR2C/2T04A	—	12.5	—	11.7	—	10.0	—	—	—	—	ns
	OR2C06A	—	12.6	—	11.8	—	10.1	—	—	—	—	ns
	OR2C/2T08A	—	12.7	—	11.9	—	10.2	—	—	—	—	ns
	OR2C/2T10A	—	12.8	—	12.0	—	10.3	—	—	—	—	ns
	OR2C12A	—	12.9	—	12.1	—	10.4	—	—	—	—	ns
	OR2C/2T15A	—	13.0	—	12.2	—	10.5	—	9.5	—	7.4	ns
	OR2C/2T26A	—	13.2	—	12.3	—	10.6	—	9.6	—	7.5	ns
	OR2C/2T40A	—	13.6	—	12.6	—	10.9	—	9.8	—	7.7	ns
CLK Input Pin → OUTPUT Pin (Sinklim)	OR2C/2T04A	—	14.7	—	13.7	—	13.1	—	—	—	—	ns
	OR2C06A	—	14.8	—	13.8	—	13.2	—	—	—	—	ns
	OR2C/2T08A	—	14.9	—	13.9	—	13.3	—	—	—	—	ns
	OR2C/2T10A	—	15.0	—	14.0	—	13.4	—	—	—	—	ns
	OR2C12A	—	15.1	—	14.1	—	13.5	—	—	—	—	ns
	OR2C/2T15A	—	15.2	—	14.2	—	13.6	—	12.1	—	10.0	ns
	OR2C/2T26A	—	15.3	—	14.3	—	13.7	—	12.2	—	10.7	ns
	OR2C/2T40A	—	15.7	—	14.6	—	14.0	—	12.4	—	10.9	ns

Notes:
The pin-to-pin timing information from ispLEVER is more accurate than this table. For earlier versions of *ORCA* Foundry, the pin-to-pin timing parameters in this table should be used instead of results reported by *ORCA* Foundry.

This clock delay is for a fully routed clock tree that uses the primary clock network. It includes both the input buffer delay, the clock routing to the PFU CLK input, the clock→Q of the FF, and the delay through the output buffer. The delay will be reduced if any of the clock branches are not used. The given timing requires that the input clock pin be located at one of the four center PICs on any side of the device and that the direct FF→I/O routing be used.

If the clock pin is not located at one of the four center PICs, this delay must be increased by up to the following amounts: OR2C/2T04A = 1.5%, OR2C06A = 2.0%, OR2C/2T08A = 3.1%, OR2C/2T10A = 3.9%, OR2C12A = 4.9%, OR2C/2T15A = 5.7%, OR2C/2T26A = 8.1%, OR2C/2T40A = 12.5%.

Timing Characteristics (continued)

Table 46B. OR2TxxB Programmable I/O Cell Timing Characteristics

OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Inputs (TJ = 85 °C, VDD = min)						
Input Rise Time	TR	—	500	—	500	ns
Input Fall Time	TF	—	500	—	500	ns
Pad to In Delay	PAD_IN_DEL	—	1.1	—	1.0	ns
Pad to Nearest PFU Latch Output	CHIP_LATCH	—	3.3	—	2.4	ns
Delay Added to General Routing (input buffer in delay mode for OR2T15B and smaller devices)	—	—	6.6	—	6.1	ns
Delay Added to General Routing (input buffer in delay mode for OR2T40B)	—	—	8.9	—	8.2	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2T15B and smaller devices)	—	—	6.4	—	6.0	ns
Delay Added to Direct-FF Routing (input buffer in delay mode for OR2T40B)	—	—	8.7	—	8.0	ns
Outputs (TJ = 85 °C, VDD = min, CL = 50 pF)						
PFU CK to Pad Delay (DOUT[3:0] to PAD):						
Fast	DOUT_DEL(F)	—	2.8	—	2.5	ns
Slewlim	DOUT_DEL(SL)	—	3.6	—	3.3	ns
Sinklim	DOUT_DEL(SI)	—	8.3	—	8.0	ns
Output to Pad Delay (OUT[3:0] to PAD):						
Fast	OUT_DEL(F)	—	2.8	—	2.5	ns
Slewlim	OUT_DEL(SL)	—	3.6	—	3.3	ns
Sinklim	OUT_DEL(SI)	—	8.3	—	8.0	ns
3-state Enable Delay (TS[3:0] to PAD):						
Fast	TS_DEL(F)	—	3.0	—	2.7	ns
Slewlim	TS_DEL(SL)	—	3.8	—	3.4	ns
Sinklim	TS_DEL(SI)	—	9.1	—	8.7	ns

Notes:
If the input buffer is placed in delay mode, the chip hold time to the nearest PFU latch is guaranteed to be 0 if the clock is routed using the primary clock network; (TJ = all, VDD = all). It should also be noted that any signals routed on the clock lines or using the TRIDI buffers directly from the input buffer do not get delayed at any time.

The delays for all input buffers assume an input rise/fall time of ≤1 V/ns.

Timing Characteristics (continued)

Table 50. Series 2 Asynchronous Peripheral Configuration Mode Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA/B Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA/B Industrial: VDD = 3.0 V to 3.6 V,
–40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Min	Max	Unit
$\overline{WR}$, $\overline{CS0}$, and CS1 Pulse Width	TWR	100	—	ns
D[7:0] Setup Time	TS	20	—	ns
D[7:0] Hold Time	TH	0	—	ns
RDY Delay	TRDY	—	60	ns
RDY Low	TB	1	8	CCLK Periods
Earliest $\overline{WR}$ After RDY Goes High*	TWR2	0	—	ns
$\overline{RD}$ to D7 Enable/Disable	TDEN	—	60	ns
CCLK to DOUT	TD	—	30	ns

* This parameter is valid whether the end of not RDY is determined from the RDY/RCLK pin or from the D7 pin.

Notes:
Serial data is transmitted out on DOUT on the falling edge of CCLK after the byte is input D[7:0].

D[6:0] timing is the same as the write data port of the D7 waveform because D[6:0] are not enabled.

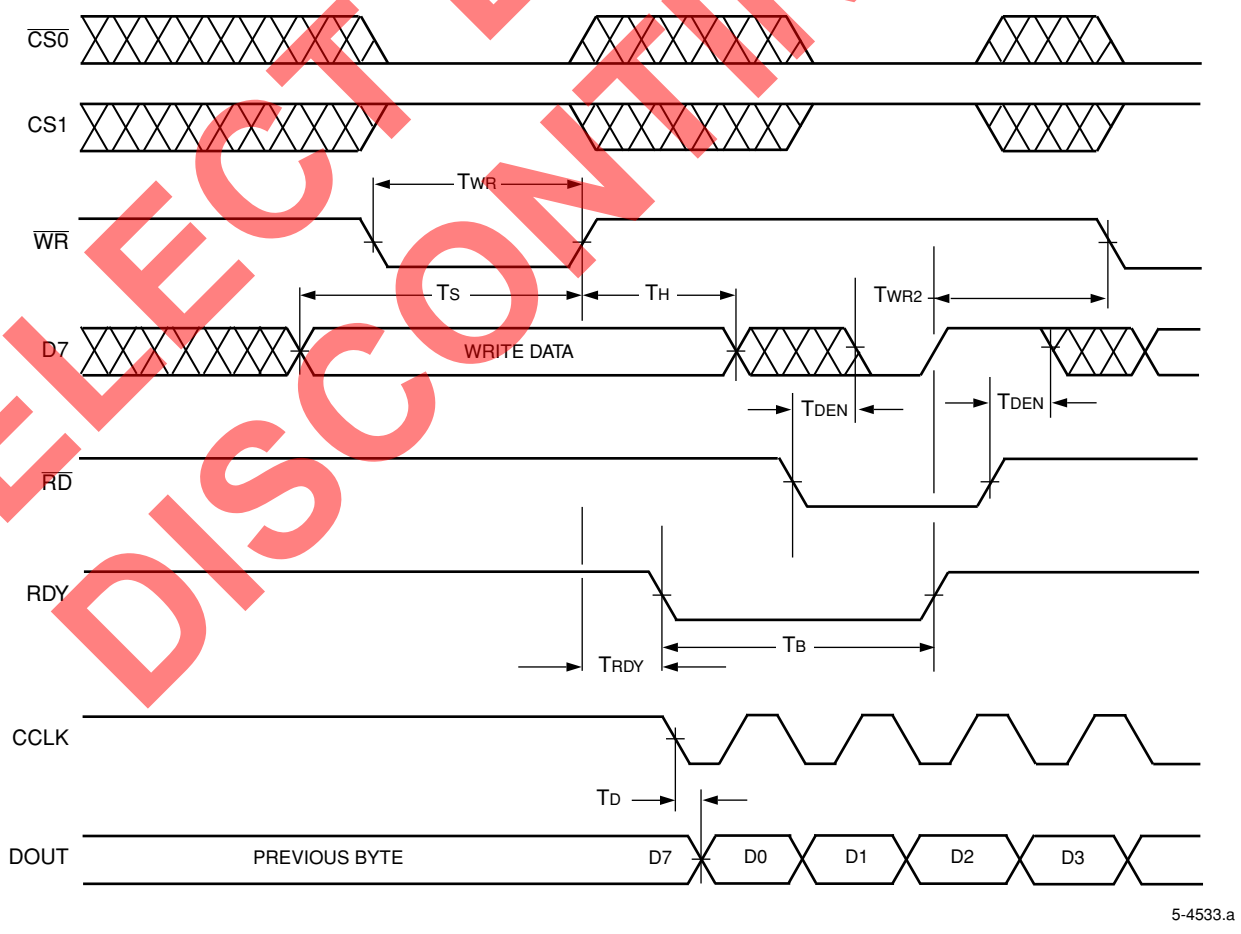


Figure 68. Asynchronous Peripheral Configuration Mode Timing Diagram

Timing Characteristics (continued)

Table 51A. OR2CxxA/OR2TxxA Synchronous Peripheral Configuration Mode Timing Characteristics

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Min	Max	Unit
D[7:0] Setup Time	TS	20	—	ns
D[7:0] Hold Time	TH	0	—	ns
CCLK High Time	TCH	50	—	ns
CCLK Low Time	TCL	50	—	ns
CCLK Frequency	FC	—	10	MHz
CCLK to DOUT	TD	—	30	ns

Note: Serial data is transmitted out on DOUT 1.5 clock cycles after the byte is input D[7:0].

Table 51B. OR2TxxB Synchronous Peripheral Configuration Mode Timing Characteristics

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Min	Max	Unit
D[7:0] Setup Time	TS	15	—	ns
D[7:0] Hold Time	TH	0	—	ns
CCLK High Time	TCH	12.5	—	ns
CCLK Low Time	TCL	12.5	—	ns
CCLK Frequency	FC	—	40	MHz
CCLK to DOUT	TD	—	10	ns

Note: Serial data is transmitted out on DOUT 1.5 clock cycles after the byte is input D[7:0].

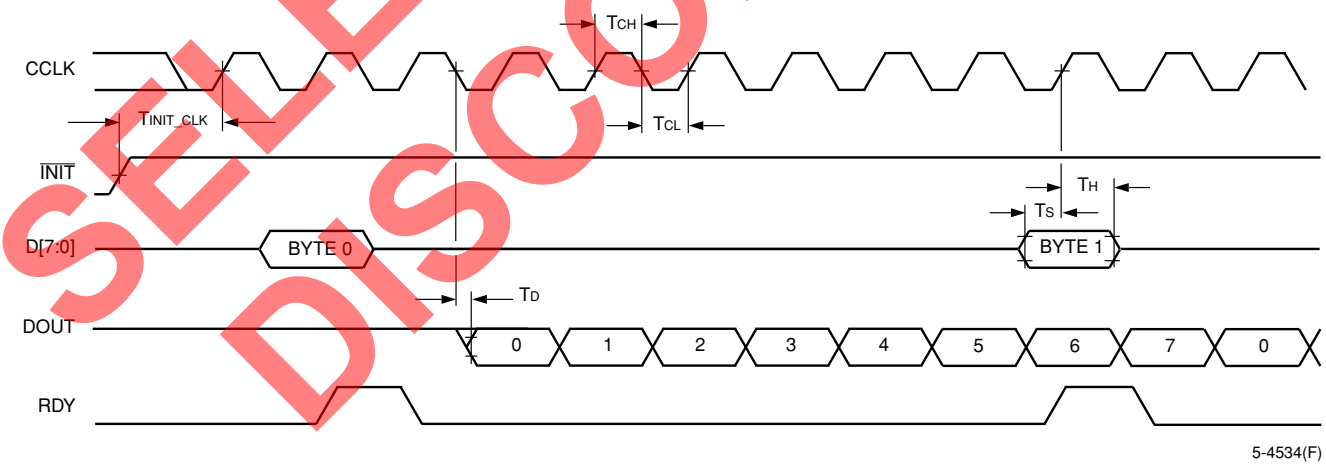


Figure 69. Synchronous Peripheral Configuration Mode Timing Diagram

Package Outline Drawings (continued)

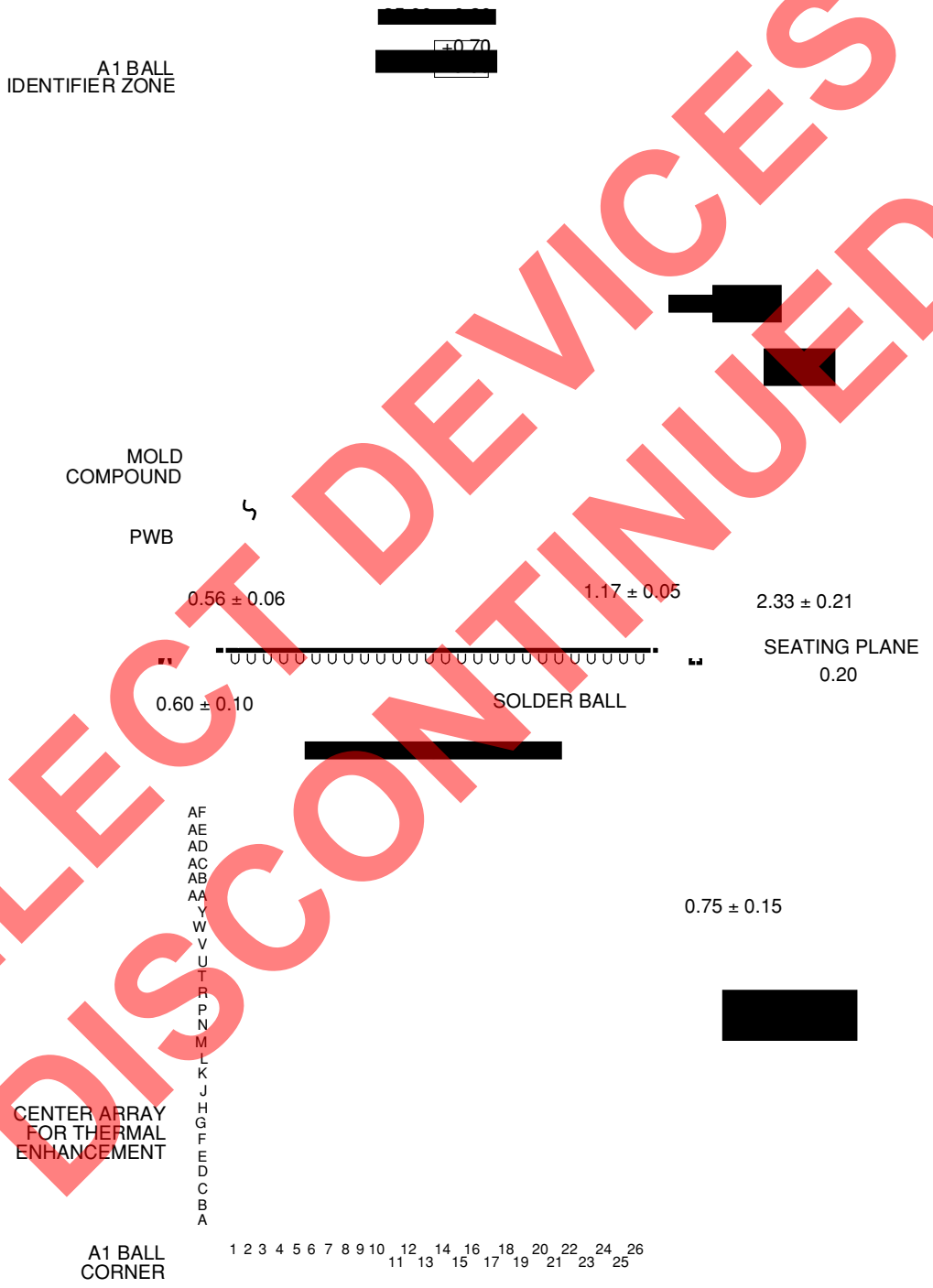
240-Pin SQFP2

Dimensions are in millimeters.

Package Outline Drawings (continued)

352-Pin PBGA

Dimensions are in millimeters.



5-4407r.4

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2C12A	OR2C12A4M84-D[2]	4	PLCC	84	C	D
	OR2C12A4S208-DB[2]	4	SQFP	208	C	DB
	OR2C12A4S240-DB[2]	4	SQFP	240	C	DB
	OR2C12A4BA256-DB[2]	4	PBGA	256	C	DB
	OR2C12A4S304-DB[2]	4	SQFP	304	C	DB
	OR2C12A4BA352-DB[2]	4	PLCC	352	C	DB
	OR2C12A3S208-DB[2]	3	SQFP	208	C	DB
	OR2C12A3S240-DB[2]	3	SQFP	240	C	DB
OR2C15A	OR2C15A4M84-D[2]	4	PLCC	84	C	D
	OR2C15A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C15A4S208-DB[2]	4	SQFP	208	C	DB
	OR2C15A4S240-DB[2]	4	SQFP	240	C	DB
	OR2C15A4BA256-DB[2]	4	PBGA	256	C	DB
	OR2C15A4S304-DB[2]	4	SQFP	304	C	DB
	OR2C15A4BA352-DB[2]	4	EBGA	352	C	DB
OR2C26A	OR2C26A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C26A4PS240-DB[2]	4	SQFP2	240	C	DB
	OR2C26A4PS304-DB[2]	4	SQFP2	304	C	DB
OR2C40A	OR2C40A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C40A4PS240-DB[2]	4	SQFP2	240	C	DB
	OR2C40A4PS304-DB[2]	4	SQFP2	304	C	DB
OR2T04A	OR2T04A5T100-DB[2]	5	TQFP	100	C	DB
	OR2T04A5T144-DB[2]	5	TQFP	144	C	DB
	OR2T04A5S208-DB[2]	5	SQFP	208	C	DB
	OR2T04A4T100-DB[2]	4	TQFP	100	C	DB
	OR2T04A4T144-DB[2]	4	TQFP	144	C	DB
	OR2T04A4S208-DB[2]	4	SQFP	208	C	DB
OR2T08A	OR2T08A5J160-DB[2]	5	QFP	160	C	DB
	OR2T08A5S208-DB[2]	5	SQFP	208	C	DB
	OR2T08A5S240-DB[2]	5	SQFP	240	C	DB
	OR2T08A5BA256-DB[2]	5	PBGA	256	C	DB
	OR2T08A4J160-DB[2]	4	QFP	160	C	DB
	OR2T08A4S208-DB[2]	4	SQFP	208	C	DB
	OR2T08A4S240-DB[2]	4	SQFP	240	C	DB
	OR2T08A4BA256-DB[2]	4	PBGA	256	C	DB