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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2304
Total RAM Bits	36864
Number of I/O	171
Number of Gates	63600
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/or2t26a6s208i-db

Description

The *ORCA* Series 2 series of SRAM-based FPGAs are an enhanced version of the ATT2C/2T architecture. The latest *ORCA* series includes patented architectural enhancements that make functions faster and easier to design while conserving the use of PLCs and routing resources.

The Series 2 devices can be used as drop-in replacements for the ATT2Cxx/ATT2Txx series, respectively, and they are also bit stream compatible with each other. The usable gate counts associated with each series are provided in Table 1. Both series are offered in a variety of packages, speed grades, and temperature ranges.

The *ORCA* series FPGA consists of two basic elements: programmable logic cells (PLCs) and programmable input/output cells (PICs). An array of PLCs is surrounded by PICs as shown in Figure 1. Each PLC contains a programmable function unit (PFU). The PLCs and PICs also contain routing resources and configuration RAM. All logic is done in the PFU. Each PFU contains four 16-bit look-up tables (LUTs) and four latches/flip-flops (FFs).

The PLC architecture provides a balanced mix of logic and routing that allows a higher utilized gate/PFU than alternative architectures. The routing resources carry logic signals between PFUs and I/O pads. The routing in the PLC is symmetrical about the horizontal and vertical axes. This improves routability by allowing a bus of signals to be routed into the PLC from any direction.

Some examples of the resources required and the performance that can be achieved using these devices are represented in Table 2.

Table 2. ORCA Series 2CA System Performance

Function	# PFUs	Speed Grade		Unit
		-3	-4	
16-bit loadable up/down counter	4	66.7	87.0	MHz
16-bit accumulator	4	66.7	87.0	MHz
8 x 8 parallel multiplier: — Multiplier mode, unpipelined[1] — ROM mode, unpipelined[2] — Multiplier mode, pipelined[3]	 22 9 44	 19.3 55.6 69.0	 25.1 71.9 82.0	 MHz MHz MHz
32 x 16 RAM: — Single port (read and write/cycle)[4] — Single port[5] — Dual port[6]	 9 9 16	 28.6 52.6 52.6	 36.2 69.0 83.3	 MHz MHz MHz
36-bit parity check (internal)	4	11.0	9.1	ns
32-bit address decode (internal)	3.25	9.5	7.5	ns

1. Implemented using 4 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 16 x 12 ROMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 4 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (28 of 44 PFUs contain only pipelining registers).
4. Implemented using 16 x 4 synchronous single-port RAM mode allowing both read and write per clock cycle, including write/read address multiplexer.
5. Implemented using 16 x 4 synchronous single-port RAM mode allowing either read or write per clock cycle, including write/read address multiplexer.
6. Implemented using 16 x 2 synchronous dual-port RAM mode.

Programmable Logic Cells (continued)

Figure 23. PLC Architecture

Programmable Input/Output Cells

(continued)

PIC Routing Resources

The PIC routing is designed to route 4-bit wide buses efficiently. For example, any four consecutive I/O pads can have both their input and output signals routed into one PLC. Using only PIC routing, either the input or output data can be routed to/from a single PLC from/to any eight pads in a row, as in Figure 25.

The connections between PLCs and the I/O pad are provided by two basic types of routing resources. These are routing resources internal to the PIC and routing resources used for PIC-PLC connection. Figure 26 and Figure 27 show a high-level and detailed view of these routing resources, respectively.

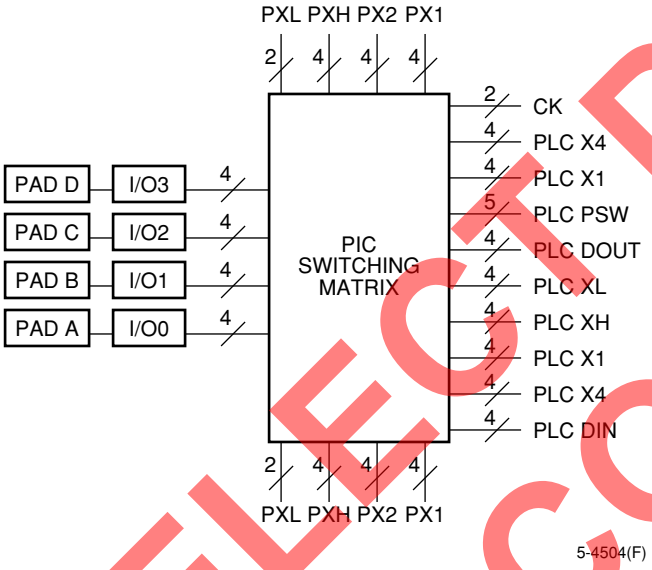


Figure 25. Simplified PIC Routing Diagram

The PIC's name is represented by a two-letter designation to indicate on which side of the device it is located followed by a number to indicate in which row or column it is located. The first letter, P, designates that the cell is a PIC and not a PLC. The second letter indicates the side of the array where the PIC is located. The four sides are left (L), right (R), top (T), and bottom (B). The individual I/O pad is indicated by a single letter (either A, B, C, or D) placed at the end of the PIC name. As an example, PL10A indicates a pad located on the left side of the array in the tenth row.

Each PIC has four pads and each pad can be configured as an input, an output (3-statable), a direct output, or a bidirectional I/O. When the pads are used as inputs, the external signals are provided to the internal circuitry at IN[3:0]. When the pads are used to provide direct inputs to the latches/FFs, they are connected through DIN[3:0]. When the pads are used as outputs, the internal signals connect to the pads through OUT[3:0]. When the pads are used as direct outputs, the output from the latches/flip-flops in the PLCs to the PIC is designated DOUT[3:0]. When the outputs are 3-statable, the 3-state enable signals are TS[3:0].

Routing Resources Internal to the PIC

For inter-PIC routing, the PIC contains 14 lines used to route signals around the perimeter of the FPGA. Figure 25 shows these lines running vertically for a PIC located on the left side. Figure 26 shows the lines running horizontally for a PIC located at the top of the FPGA.

PXL Lines. Each PIC has two PXL lines, labeled PXL[1:0]. Like the XL lines of the PLC, the PXL lines span the entire edge of the FPGA.

PXH Lines. Each PIC has four PXH lines, labeled PXH[3:0]. Like the XH lines of the PLC, the PXH lines span half the edge of the FPGA.

PX2 Lines. There are four PX2 lines in each PIC, labeled PX2[3:0]. The PX2 lines pass through two adjacent PICs before being broken. These are used to route nets around the perimeter equally a distance of two or more PICs.

PX1 Lines. Each PIC has four PX1 lines, labeled PX1[3:0]. The PX1 lines are one PIC long and are extended to adjacent PICs by enabling CIPs.

Interquad Routing

In all the *ORCA* Series 2 devices, the PLC array is split into four equal quadrants. In between these quadrants, routing has been added to route signals between the quadrants, especially to the quadrant in the opposite corner. The two types of interquad blocks, vertical and horizontal, are pitch matched to PICs. Vertical interquad blocks (vIQ) run between quadrants on the left and right, while horizontal interquad blocks (hIQ) run between top and bottom quadrants. Since hIQ and vIQ blocks have the same logic, only the hIQ block is described below.

The interquad routing connects XL and XH lines. It does not affect local routing (XSW, X1, X4, fast carry), so local routing is the same, whether PLC-PLC connections cross quadrants or not. There are no connections to the local lines in the interquad blocks. Figure 28 presents a (not to scale) view of interquad routing.

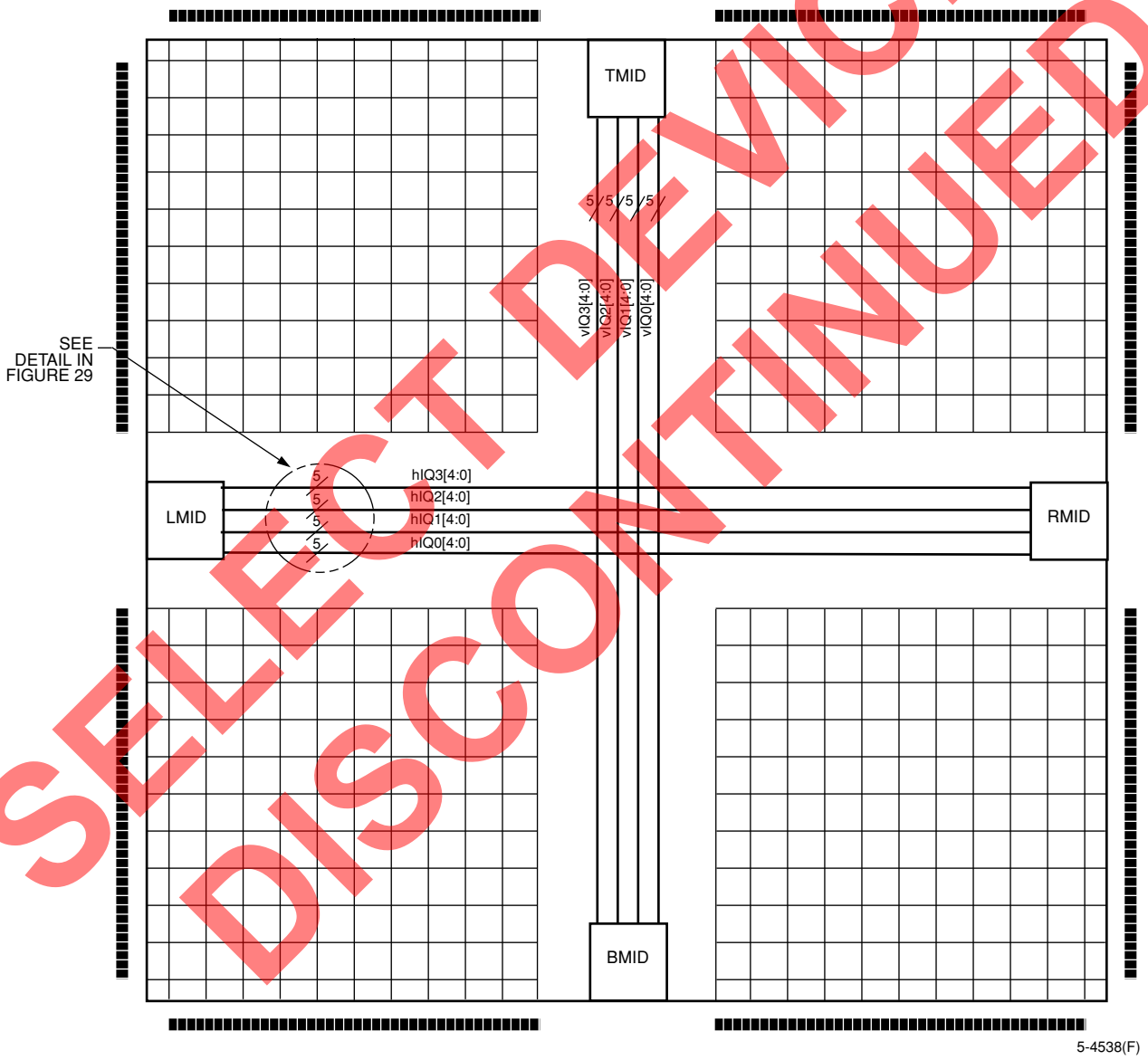


Figure 28. Interquad Routing

Pin Information (continued)

Table 19. OR2C04A, OR2C12A, and OR2C/2T15A 84-Pin PLCC Pinout

Pin	2C04A Pad	2C12A Pad	2C/2T15A Pad	Function
1	VSS	VSS	VSS	VSS
2	PT5A	PT9A	PT10A	I/O-D2
3	VSS	VSS	VSS	VSS
4	PT4D	PT8D	PT9D	I/O-D1
5	PT4A	PT8A	PT9A	I/O-D0/DIN
6	PT3A	PT7A	PT8A	I/O-DOUT
7	PT2D	PT6D	PT7D	I/O-VDD5
8	PT2A	PT5A	PT6A	I/O-TDI
9	PT1D	PT3A	PT4A	I/O-TMS
10	PT1A	PT1A	PT1A	I/O-TCK
11	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO	RD_DATA/TDO
12	VDD	VDD	VDD	VDD
13	VSS	VSS	VSS	VSS
14	PL1C	PL2D	PL2D	I/O-A0
15	PL1A	PL4A	PL5A	I/O-A1
16	PL2D	PL5A	PL6A	I/O-A2
17	PL2A	PL6A	PL7A	I/O-A3
18	PL3A	PL7A	PL8A	I/O-A4
19	PL4D	PL8D	PL9D	I/O-A5
20	PL4A	PL8A	PL9A	I/O-A6
21	PL5A	PL9A	PL10A	I/O-A7
22	VDD	VDD	VDD	VDD
23	PL6A	PL10A	PL11A	I/O-A8
24	VSS	VSS	VSS	VSS
25	PL7D	PL11D	PL12D	I/O-A9
26	PL7A	PL11A	PL12A	I/O-A10
27	PL8A	PL12A	PL13A	I/O-A11
28	PL9D	PL13D	PL14D	I/O-A12
29	PL9A	PL14B	PL15B	I/O-A13
30	PL10D	PL16D	PL17D	I/O-A14
31	PL10A	PL18A	PL20A	I/O-A15
32	CCLK	CCLK	CCLK	CCLK
33	VDD	VDD	VDD	VDD
34	VSS	VSS	VSS	VSS
35	PB1A	PB1A	PB1A	I/O-A16
36	PB1D	PB3D	PB4D	I/O-A17
37	PB2A	PB5B	PB6B	I/O
38	PB2D	PB6D	PB7D	I/O
39	PB3A	PB7A	PB8A	I/O
40	PB4A	PB8A	PB9A	I/O
41	PB4D	PB8D	PB9D	I/O
42	PB5A	PB9A	PB10A	I/O
43	VSS	VSS	VSS	VSS

Note: The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout

Pin	2C/2T04A Pad	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
3	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	PL1D	I/O
4	PL1C	PL1A	PL2D	PL2D	PL2D	PL2D	PL2D	PL3D	I/O-A0
5	PL1B	PL2D	PL3D	PL3D	PL3D	PL4D	PL4D	PL5D	I/O-VDD5
6	See Note	PL2C	PL3C	PL3C	PL3A	PL4A	PL4A	PL6D	I/O
7	PL1A	PL2A	PL3A	PL3A	PL4A	PL5A	PL5A	PL8D	I/O-A1
8	PL2D	PL3D	PL4D	PL4A	PL5A	PL6A	PL6A	PL9A	I/O-A2
9	PL2C	PL3C	PL4C	PL5C	PL6D	PL7D	PL7D	PL10D	I/O
10	PL2B	PL3B	PL4B	PL5B	PL6B	PL7B	PL7B	PL10B	I/O
11	PL2A	PL3A	PL4A	PL5A	PL6A	PL7A	PL7A	PL10A	I/O-A3
12	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
13	PL3D	PL4D	PL5D	PL6D	PL7D	PL8D	PL8D	PL11D	I/O
14	PL3C	PL4C	PL5C	PL6C	PL7C	PL8C	PL8A	PL11A	I/O
15	PL3B	PL4B	PL5B	PL6B	PL7B	PL8B	PL9D	PL12D	I/O
16	PL3A	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL12A	I/O-A4
17	PL4D	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL13D	I/O-A5
18	PL4C	PL5C	PL6C	PL7C	PL8C	PL9C	PL10A	PL13A	I/O
19	PL4B	PL5B	PL6B	PL7B	PL8B	PL9B	PL11D	PL14D	I/O
20	PL4A	PL5A	PL6A	PL7A	PL8A	PL9A	PL11A	PL14A	I/O-A6
21	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
22	PL5D	PL6D	PL7D	PL8D	PL9D	PL10D	PL12D	PL15D	I/O
23	PL5C	PL6C	PL7C	PL8C	PL9C	PL10C	PL12C	PL15C	I/O
24	PL5B	PL6B	PL7B	PL8B	PL9B	PL10B	PL12B	PL15B	I/O
25	PL5A	PL6A	PL7A	PL8A	PL9A	PL10A	PL12A	PL15A	I/O-A7
26	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
27	PL6D	PL7D	PL8D	PL9D	PL10D	PL11D	PL13D	PL16D	I/O
28	PL6C	PL7C	PL8C	PL9C	PL10C	PL11C	PL13C	PL16C	I/O-VDD5
29	PL6B	PL7B	PL8B	PL9B	PL10B	PL11B	PL13B	PL16B	I/O
30	PL6A	PL7A	PL8A	PL9A	PL10A	PL11A	PL13A	PL16A	I/O-A8
31	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
32	PL7D	PL8D	PL9D	PL10D	PL11D	PL12D	PL14D	PL17D	I/O-A9
33	PL7C	PL8C	PL9C	PL10C	PL11C	PL12C	PL14A	PL17A	I/O
34	PL7B	PL8B	PL9B	PL10B	PL11B	PL12B	PL15D	PL18D	I/O
35	PL7A	PL8A	PL9A	PL10A	PL11A	PL12A	PL15A	PL18A	I/O-A10
36	PL8D	PL9D	PL10D	PL11D	PL12D	PL13D	PL16D	PL19D	I/O
37	PL8C	PL9C	PL10C	PL11C	PL12C	PL13C	PL16A	PL19A	I/O
38	PL8B	PL9B	PL10B	PL11B	PL12B	PL13B	PL17D	PL20D	I/O
39	PL8A	PL9A	PL10A	PL11A	PL12A	PL13A	PL17A	PL20A	I/O-A11
40	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
41	PL9D	PL10D	PL11D	PL12D	PL13D	PL14D	PL18D	PL21D	I/O-A12
42	PL9C	PL10C	PL11C	PL12C	PL13B	PL14B	PL18B	PL21B	I/O
43	PL9B	PL10B	PL11B	PL12B	PL14D	PL15D	PL19D	PL22D	I/O

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 23. OR2C/2T04A, OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 208-Pin SQFP/SQFP2 Pinout (continued)

Pin	*2C/2T04A Pad*	*2C06A Pad*	*2C/2T08A Pad*	*2C/2T10A Pad*	*2C12A Pad*	*2C/2T15A/B Pad*	*2C/2T26A Pad*	*2C/2T40A/B Pad*	*Function*
87	PB7C	PB8C	PB9C	PB10C	PB11C	PB12C	PB15A	PB18A	I/O
88	PB7D	PB8D	PB9D	PB10D	PB11D	PB12D	PB15D	PB18D	I/O
89	PB8A	PB9A	PB10A	PB11A	PB12A	PB13A	PB16A	PB19A	I/O-HDC
90	PB8B	PB9B	PB10B	PB11B	PB12B	PB13B	PB16D	PB19D	I/O
91	PB8C	PB9C	PB10C	PB11C	PB12C	PB13C	PB17A	PB20A	I/O
92	PB8D	PB9D	PB10D	PB11D	PB12D	PB13D	PB17D	PB20D	I/O
93	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
94	PB9A	PB10A	PB11A	PB12A	PB13A	PB14A	PB18A	PB21A	I/O-$\overline{\text{LDC}}$
95	PB9B	PB10B	PB11D	PB13A	PB13D	PB14D	PB18D	PB22D	I/O
96	PB9C	PB10C	PB12A	PB13B	PB14A	PB15A	PB19A	PB23A	I/O
97	PB9D	PB10D	PB12B	PB13C	PB14D	PB15D	PB19D	PB24D	I/O
98	PB10A	PB11A	PB12C	PB13D	PB15A	PB16A	PB20A	PB25A	I/O-$\overline{\text{INIT}}$
99	PB10B	PB11C	PB12D	PB14A	PB16A	PB17A	PB21A	PB26A	I/O
100	PB10C	PB11D	PB13A	PB15A	PB17A	PB18A	PB22A	PB27A	I/O
101	PB10D	PB12A	PB13D	PB15D	PB18A	PB19D	PB23D	PB28D	I/O
102	See Note	PB12D	PB14D	PB16D	PB18D	PB20D	PB24D	PB30D	I/O
103	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
104	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
105	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
106	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
107	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
108	PR10A	PR12A	PR14A	PR16A	PR18A	PR20A	PR24A	PR30A	I/O-M0
109	PR10B	PR12D	PR13A	PR15A	PR18D	PR19A	PR23A	PR28A	I/O
110	PR10C	PR11A	PR13D	PR15D	PR17B	PR18A	PR22A	PR27A	I/O
111	PR10D	PR11B	PR12A	PR14A	PR16A	PR17A	PR21A	PR26A	I/O
112	PR9A	PR10A	PR11A	PR13B	PR15D	PR16D	PR20D	PR23D	I/O-M1
113	PR9B	PR10B	PR11B	PR13C	PR14A	PR15A	PR19A	PR22A	I/O
114	PR9C	PR10C	PR11C	PR12A	PR14D	PR15D	PR19D	PR22D	I/O-VDD5
115	PR9D	PR10D	PR11D	PR12B	PR13A	PR14A	PR18A	PR21A	I/O
116	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
117	PR8A	PR9A	PR10A	PR11A	PR12A	PR13A	PR17A	PR20A	I/O-M2
118	PR8B	PR9B	PR10B	PR11B	PR12B	PR13B	PR17D	PR20D	I/O
119	PR8C	PR9C	PR10C	PR11C	PR12C	PR13C	PR16A	PR19A	I/O
120	PR8D	PR9D	PR10D	PR11D	PR12D	PR13D	PR16D	PR19D	I/O
121	PR7A	PR8A	PR9A	PR10A	PR11A	PR12A	PR15A	PR18A	I/O-M3
122	PR7B	PR8B	PR9B	PR10B	PR11B	PR12B	PR15D	PR18D	I/O
123	PR7C	PR8C	PR9C	PR10C	PR11C	PR12C	PR14A	PR17A	I/O
124	PR7D	PR8D	PR9D	PR10D	PR11D	PR12D	PR14D	PR17D	I/O
125	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
126	PR6A	PR7A	PR8A	PR9A	PR10A	PR11A	PR13A	PR16A	I/O
127	PR6B	PR7B	PR8B	PR9B	PR10B	PR11B	PR13B	PR16B	I/O
128	PR6C	PR7C	PR8C	PR9C	PR10C	PR11C	PR13C	PR16C	I/O
129	PR6D	PR7D	PR8D	PR9D	PR10D	PR11D	PR13D	PR16D	I/O

Notes:
The OR2C04A and OR2T04A do not have bond pads connected to 208-pin SQFP package pin numbers 6, 45, 47, 56, 60, 102, 153, 154, 166, 201, and 203.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 24. OR2C06A, OR2C/2T08A, OR2C/2T10A, OR2C12A, OR2C/2T15A/B, OR2C/2T26A, and OR2C/2T40A/B 240-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C06A Pad	2C/2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15B Pad	2C/2T26A Pad	2C/2T40A/B Pad	Function
127	PR12D	PR13D	PR15D	PR17B	PR18A	PR22A	PR27A	I/O
128	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
129	PR11A	PR12A	PR14A	PR16A	PR17A	PR21A	PR26A	I/O
130	PR11B	PR12B	PR14C	PR16D	PR17D	PR21D	PR25A	I/O
131	PR11C	PR12C	PR14D	PR15A	PR16A	PR20A	PR24A	I/O
132	PR11D	PR12D	PR13A	PR15C	PR16C	PR20C	PR24D	I/O
133	PR10A	PR11A	PR13B	PR15D	PR16D	PR20D	PR23D	I/O-M1
134	PR10B	PR11B	PR13C	PR14A	PR15A	PR19A	PR22A	I/O
135	PR10C	PR11C	PR12A	PR14D	PR15D	PR19D	PR22D	I/O-VDD5
136	PR10D	PR11D	PR12B	PR13A	PR14A	PR18A	PR21A	I/O
137	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
138	PR9A	PR10A	PR11A	PR12A	PR13A	PR17A	PR20A	I/O-M2
139	PR9B	PR10B	PR11B	PR12B	PR13B	PR17D	PR20D	I/O
140	PR9C	PR10C	PR11C	PR12C	PR13C	PR16A	PR19A	I/O
141	PR9D	PR10D	PR11D	PR12D	PR13D	PR16D	PR19D	I/O
142	PR8A	PR9A	PR10A	PR11A	PR12A	PR15A	PR18A	I/O-M3
143	PR8B	PR9B	PR10B	PR11B	PR12B	PR15D	PR18D	I/O
144	PR8C	PR9C	PR10C	PR11C	PR12C	PR14A	PR17A	I/O
145	PR8D	PR9D	PR10D	PR11D	PR12D	PR14D	PR17D	I/O
146	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
147	PR7A	PR8A	PR9A	PR10A	PR11A	PR13A	PR16A	I/O
148	PR7B	PR8B	PR9B	PR10B	PR11B	PR13B	PR16B	I/O
149	PR7C	PR8C	PR9C	PR10C	PR11C	PR13C	PR16C	I/O
150	PR7D	PR8D	PR9D	PR10D	PR11D	PR13D	PR16D	I/O
151	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
152	PR6A	PR7A	PR8A	PR9A	PR10A	PR12A	PR15A	I/O
153	PR6B	PR7B	PR8B	PR9B	PR10B	PR12B	PR15B	I/O
154	PR6C	PR7C	PR8C	PR9C	PR10C	PR12C	PR15C	I/O
155	PR6D	PR7D	PR8D	PR9D	PR10D	PR12D	PR15D	I/O
156	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
157	PR5A	PR6A	PR7A	PR8A	PR9A	PR11A	PR14A	I/O-VDD5
158	PR5B	PR6B	PR7B	PR8B	PR9B	PR11D	PR14D	I/O
159	PR5C	PR6C	PR7C	PR8C	PR9C	PR10A	PR13A	I/O
160	PR5D	PR6D	PR7D	PR8D	PR9D	PR10D	PR13D	I/O
161	PR4A	PR5A	PR6A	PR7A	PR8A	PR9A	PR12A	I/O-CS1
162	PR4B	PR5B	PR6B	PR7B	PR8B	PR9D	PR12D	I/O
163	PR4C	PR5C	PR6C	PR7C	PR8C	PR8A	PR11A	I/O
164	PR4D	PR5D	PR6D	PR7D	PR8D	PR8D	PR11D	I/O
165	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
166	PR3A	PR4A	PR5A	PR6A	PR7A	PR7A	PR10A	I/O-$\overline{CS0}$
167	PR3B	PR4B	PR4B	PR6B	PR7B	PR7B	PR10B	I/O
168	PR3C	PR4C	PR4C	PR5B	PR6B	PR6B	PR9B	I/O

Notes:
The OR2C/2T08A and OR2C/2T10A do not have bond pads connected to 240-pin SQFP package pin numbers 113 and 188.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 25. OR2C06A, OR2T08A, OR2C/2T10A, OR2C12A, and OR2C/2T15A/B 256-Pin PBGA Pinout

Pin	2C06A Pad	2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	Function
C2	PL1D	PL1D	PL1D	PL1D	PL1D	I/O
D2	PL1C	PL1B	PL1B	PL1C	PL1C	I/O
D3	PL1B	PL1A	PL1A	PL1B	PL1B	I/O
E4	PL1A	PL2D	PL2D	PL2D	PL2D	I/O-A0
C1	—	PL2C	PL2C	PL2C	PL2A	I/O
D1	—	PL2B	PL2B	PL2B	PL3D	I/O
E3	—	PL2A	PL2A	PL2A	PL3A	I/O
E2	PL2D	PL3D	PL3D	PL3D	PL4D	I/O-VDD5
E1	PL2C	PL3C	PL3C	PL3A	PL4A	I/O
F3	PL2B	PL3B	PL3B	PL4D	PL5D	I/O
G4	PL2A	PL3A	PL3A	PL4A	PL5A	I/O-A1
F2	—	—	PL4D	PL5D	PL6D	I/O
F1	PL3D	PL4D	PL4A	PL5A	PL6A	I/O-A2
G3	PL3C	PL4C	PL5C	PL6D	PL7D	I/O
G2	PL3B	PL4B	PL5B	PL6B	PL7B	I/O
G1	PL3A	PL4A	PL5A	PL6A	PL7A	I/O-A3
H3	PL4D	PL5D	PL6D	PL7D	PL8D	I/O
H2	PL4C	PL5C	PL6C	PL7C	PL8C	I/O
H1	PL4B	PL5B	PL6B	PL7B	PL8B	I/O
J4	PL4A	PL5A	PL6A	PL7A	PL8A	I/O-A4
J3	PL5D	PL6D	PL7D	PL8D	PL9D	I/O-A5
J2	PL5C	PL6C	PL7C	PL8C	PL9C	I/O
J1	PL5B	PL6B	PL7B	PL8B	PL9B	I/O
K2	PL5A	PL6A	PL7A	PL8A	PL9A	I/O-A6
K3	PL6D	PL7D	PL8D	PL9D	PL10D	I/O
K1	PL6C	PL7C	PL8C	PL9C	PL10C	I/O
L1	PL6B	PL7B	PL8B	PL9B	PL10B	I/O
L2	PL6A	PL7A	PL8A	PL9A	PL10A	I/O-A7
L3	PL7D	PL8D	PL9D	PL10D	PL11D	I/O
L4	PL7C	PL8C	PL9C	PL10C	PL11C	I/O-VDD5
M1	PL7B	PL8B	PL9B	PL10B	PL11B	I/O
M2	PL7A	PL8A	PL9A	PL10A	PL11A	I/O-A8
M3	PL8D	PL9D	PL10D	PL11D	PL12D	I/O-A9
M4	PL8C	PL9C	PL10C	PL11C	PL12C	I/O
N1	PL8B	PL9B	PL10B	PL11B	PL12B	I/O
N2	PL8A	PL9A	PL10A	PL11A	PL12A	I/O-A10
N3	PL9D	PL10D	PL11D	PL12D	PL13D	I/O
P1	PL9C	PL10C	PL11C	PL12C	PL13C	I/O
P2	PL9B	PL10B	PL11B	PL12B	PL13B	I/O
R1	PL9A	PL10A	PL11A	PL12A	PL13A	I/O-A11

Notes:
The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The OR2C/2T08A do not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 4 x 4 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 25. OR2C06A, OR2T08A, OR2C/2T10A, OR2C12A, and OR2C/2T15A/B 256-Pin PBGA Pinout (continued)

Pin	2C06A Pad	2T08A Pad	2C/2T10A Pad	2C12A Pad	2C/2T15A/B Pad	Function
E19	PR2B	PR3B	PR3B	PR4B	PR5B	I/O
D20	PR2C	PR3C	PR3C	PR4D	PR5D	I/O
E18	PR2D	PR3D	PR3D	PR3A	PR4A	I/O-VDD5
D19	PR1A	PR2A	PR2A	PR2A	PR3A	I/O-$\overline{WR}$
C20	PR1B	PR2B	PR2B	PR2B	PR3B	I/O
E17	PR1C	PR2C	PR2C	PR2C	PR2A	I/O
D18	PR1D	PR2D	PR2D	PR2D	PR2D	I/O
C19	—	PR1A	PR1A	PR1A	PR1A	I/O
B20	—	PR1B	PR1B	PR1B	PR1B	I/O
C18	—	PR1C	PR1C	PR1C	PR1C	I/O
B19	—	PR1D	PR1D	PR1D	PR1D	I/O
A20	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$	$\overline{RD\_CFGN}$
A19	—	PT14D	PT16D	PT18D	PT20D	I/O
B18	PT12D	PT14C	PT16C	PT18C	PT20C	I/O
B17	PT12C	PT14B	PT16B	PT18B	PT20A	I/O
C17	PT12B	PT14A	PT16A	PT18A	PT19D	I/O
D16	PT12A	PT13D	PT15D	PT17D	PT19A	I/O-RDY/RCLK
A18	—	PT13C	PT15C	PT17A	PT18A	I/O
A17	PT11D	PT13B	PT15B	PT16D	PT17D	I/O
C16	PT11C	PT13A	PT15A	PT16C	PT17C	I/O
B16	PT11B	PT12D	PT14D	PT16A	PT17A	I/O
A16	PT11A	PT12C	PT13D	PT15D	PT16D	I/O-D7
C15	—	PT12B	PT13C	PT15A	PT16A	I/O
D14	PT10D	PT12A	PT13B	PT14D	PT15D	I/O-VDD5
B15	PT10C	PT11D	PT13A	PT14A	PT15A	I/O
A15	PT10B	PT11C	PT12D	PT13D	PT14D	I/O
C14	PT10A	PT11B	PT12B	PT13B	PT14B	I/O-D6
B14	PT9D	PT11A	PT12A	PT13A	PT14A	I/O
A14	PT9C	PT10D	PT11D	PT12D	PT13D	I/O
C13	—	PT10C	PT11C	PT12C	PT13C	I/O
B13	PT9B	PT10B	PT11B	PT12B	PT13B	I/O
A13	PT9A	PT10A	PT11A	PT12A	PT13A	I/O-D5
D12	PT8D	PT9D	PT10D	PT11D	PT12D	I/O
C12	PT8C	PT9C	PT10C	PT11C	PT12C	I/O
B12	PT8B	PT9B	PT10B	PT11B	PT12B	I/O
A12	PT8A	PT9A	PT10A	PT11A	PT12A	I/O-D4
B11	PT7D	PT8D	PT9D	PT10D	PT11D	I/O
C11	PT7C	PT8C	PT9C	PT10C	PT11C	I/O
A11	PT7B	PT8B	PT9B	PT10B	PT11B	I/O
A10	PT7A	PT8A	PT9A	PT10A	PT11A	I/O-D3

Notes:
The W3 pin on the 256-pin PBGA package is unconnected for all devices listed in this table.

The OR2C/2T08A do not have bond pads connected to the 256-pin PBGA package pins F2 and Y17.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

The pins labeled VSS-ETC are the 4 x 4 array of thermal balls located at the center of the package. The balls can be attached to the ground plane of the board for enhanced thermal capability (see Table 29), or they can be left unconnected.

Pin Information (continued)

Table 26. OR2C12A, OR2C15A, OR2C26A, and OR2C40A 304-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C12A Pad	2C15A Pad	2C26A Pad	2C40A Pad	Function
90	PB3D	PB4D	PB4D	PB5D	I/O-A17
91	PB4A	PB5A	PB5A	PB6A	I/O
92	PB4D	PB5D	PB5D	PB6D	I/O
93	PB5A	PB6A	PB6A	PB7A	I/O
94	PB5B	PB6B	PB6B	PB7D	I/O
95	PB5C	PB6C	PB6C	PB8A	I/O
96	PB5D	PB6D	PB6D	PB8D	I/O
97	PB6A	PB7A	PB7A	PB9A	I/O
98	PB6B	PB7B	PB7B	PB9D	I/O
99	PB6C	PB7C	PB7C	PB10A	I/O
100	PB6D	PB7D	PB7D	PB10D	I/O
101	VDD	VDD	VDD	VDD	VDD
102	PB7A	PB8A	PB8A	PB11A	I/O
103	PB7B	PB8B	PB8D	PB11D	I/O
104	PB7C	PB8C	PB9A	PB12A	I/O
105	PB7D	PB8D	PB9D	PB12D	I/O
106	PB8A	PB9A	PB10A	PB13A	I/O
107	PB8B	PB9B	PB10D	PB13D	I/O
108	PB8C	PB9C	PB11A	PB14A	I/O
109	PB8D	PB9D	PB11D	PB14D	I/O
110	VSS	VSS	VSS	VSS	VSS
111	PB9A	PB10A	PB12A	PB15A	I/O
112	PB9B	PB10B	PB12B	PB15B	I/O
113	PB9C	PB10C	PB12C	PB15C	I/O
114	PB9D	PB10D	PB12D	PB15D	I/O
115	VSS	VSS	VSS	VSS	VSS
116	PB10A	PB11A	PB13A	PB16A	I/O
117	PB10B	PB11B	PB13B	PB16B	I/O
118	PB10C	PB11C	PB13C	PB16C	I/O
119	PB10D	PB11D	PB13D	PB16D	I/O
120	VSS	VSS	VSS	VSS	VSS
121	PB11A	PB12A	PB14A	PB17A	I/O
122	PB11B	PB12B	PB14D	PB17D	I/O
123	PB11C	PB12C	PB15A	PB18A	I/O
124	PB11D	PB12D	PB15D	PB18D	I/O
125	PB12A	PB13A	PB16A	PB19A	I/O-HDC
126	PB12B	PB13B	PB16D	PB19D	I/O
127	PB12C	PB13C	PB17A	PB20A	I/O
128	PB12D	PB13D	PB17D	PB20D	I/O
129	VDD	VDD	VDD	VDD	VDD
130	PB13A	PB14A	PB18A	PB21A	I/O-$\overline{\text{LDC}}$
131	PB13B	PB14B	PB18B	PB21D	I/O
132	PB13C	PB14C	PB18C	PB22A	I/O
133	PB13D	PB14D	PB18D	PB22D	I/O
134	PB14A	PB15A	PB19A	PB23A	I/O

Note: The OR2TxxA and OR2TxxB series are not offered in the 304-pin SQFP/SQFP2 packages.

Pin Information (continued)

Table 26. OR2C12A, OR2C15A, OR2C26A, and OR2C40A 304-Pin SQFP/SQFP2 Pinout (continued)

Pin	2C12A Pad	2C15A Pad	2C26A Pad	2C40A Pad	Function
135	PB14B	PB15B	PB19B	PB24A	I/O
136	PB14D	PB15D	PB19D	PB24D	I/O
137	PB15A	PB16A	PB20A	PB25A	I/O-$\overline{\text{INIT}}$
138	PB15D	PB16D	PB20D	PB25D	I/O
139	PB16A	PB17A	PB21A	PB26A	I/O
140	PB16D	PB17D	PB21D	PB26D	I/O
141	VSS	VSS	VSS	VSS	VSS
142	PB17A	PB18A	PB22A	PB27A	I/O
143	PB17B	PB18B	PB22B	PB27B	I/O
144	PB17C	PB18D	PB22D	PB27D	I/O
145	PB17D	PB19A	PB23A	PB28A	I/O
146	PB18A	PB19D	PB23D	PB28D	I/O
147	PB18B	PB20A	PB24A	PB29A	I/O
148	PB18C	PB20B	PB24B	PB29D	I/O
149	PB18D	PB20D	PB24D	PB30D	I/O
150	VSS	VSS	VSS	VSS	VSS
151	DONE	DONE	DONE	DONE	DONE
152	VDD	VDD	VDD	VDD	VDD
153	VSS	VSS	VSS	VSS	VSS
154	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
155	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$	$\overline{\text{PRGM}}$
156	PR18A	PR20A	PR24A	PR30A	I/O-M0
157	PR18B	PR20C	PR24C	PR29A	I/O
158	PR18C	PR20D	PR24D	PR29D	I/O
159	PR18D	PR19A	PR23A	PR28A	I/O
160	PR17A	PR19D	PR23D	PR28D	I/O
161	PR17B	PR18A	PR22A	PR27A	I/O
162	PR17C	PR18B	PR22B	PR27B	I/O
163	PR17D	PR18D	PR22D	PR27D	I/O
164	VSS	VSS	VSS	VSS	VSS
165	PR16A	PR17A	PR21A	PR26A	I/O
166	PR16D	PR17D	PR21D	PR25A	I/O
167	PR15A	PR16A	PR20A	PR24A	I/O
168	PR15C	PR16C	PR20C	PR24D	I/O
169	PR15D	PR16D	PR20D	PR23D	I/O-M1
170	PR14A	PR15A	PR19A	PR22A	I/O
171	PR14C	PR15C	PR19C	PR22C	I/O
172	PR14D	PR15D	PR19D	PR22D	I/O
173	PR13A	PR14A	PR18A	PR21A	I/O
174	PR13C	PR14C	PR18C	PR21C	I/O
175	PR13D	PR14D	PR18D	PR21D	I/O
176	VDD	VDD	VDD	VDD	VDD
177	PR12A	PR13A	PR17A	PR20A	I/O-M2
178	PR12B	PR13B	PR17D	PR20D	I/O
179	PR12C	PR13C	PR16A	PR19A	I/O

Note: The OR2TxxA and OR2TxxB series are not offered in the 304-pin SQFP/SQFP2 packages.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
T28	PL11D	PL13D	PL16D	I/O
T30	PL11C	PL13C	PL16C	I/O-VDD5
U31	PL11B	PL13B	PL16B	I/O
U30	PL11A	PL13A	PL16A	I/O-A8
U29	PL12D	PL14D	PL17D	I/O-A9
V31	—	PL14C	PL17C	I/O
V30	PL12C	PL14A	PL17A	I/O
V29	PL12B	PL15D	PL18D	I/O
W31	—	PL15C	PL18C	I/O
V28	PL12A	PL15A	PL18A	I/O-A10
W30	PL13D	PL16D	PL19D	I/O
W29	—	PL16C	PL19C	I/O
Y30	PL13C	PL16A	PL19A	I/O
W28	PL13B	PL17D	PL20D	I/O
Y29	PL13A	PL17A	PL20A	I/O-A11
AA31	PL14D	PL18D	PL21D	I/O-A12
AA30	PL14C	PL18C	PL21C	I/O
Y28	PL14B	PL18B	PL21B	I/O
AA29	PL14A	PL18A	PL21A	I/O
AB31	PL15D	PL19D	PL22D	I/O
AB30	PL15C	PL19C	PL22C	I/O
AB29	PL15B	PL19B	PL22B	I/O-A13
AC31	PL15A	PL19A	PL22A	I/O
AC30	PL16D	PL20D	PL23D	I/O
AB28	PL16C	PL20C	PL23C	I/O
AC29	PL16B	PL20B	PL24D	I/O
AD30	PL16A	PL20A	PL25D	I/O
AD29	PL17D	PL21D	PL25A	I/O-A14
AC28	PL17C	PL21C	PL26C	I/O
AE31	PL17B	PL21B	PL26B	I/O
AE30	PL17A	PL21A	PL26A	I/O
AE29	PL18D	PL22D	PL27D	I/O-VDD5
AD28	PL18C	PL22C	PL27C	I/O
AF31	PL18B	PL22B	PL27B	I/O
AF30	PL18A	PL22A	PL27A	I/O
AF29	PL19D	PL23D	PL28D	I/O
AG31	PL19C	PL23C	PL28C	I/O
AG30	PL19B	PL23B	PL28B	I/O
AG29	PL19A	PL23A	PL28A	I/O
AF28	PL20D	PL24D	PL29A	I/O
AH31	PL20C	PL24C	PL30C	I/O
AH30	PL20B	PL24B	PL30B	I/O
AH29	PL20A	PL24A	PL30A	I/O-A15
AG28	CCLK	CCLK	CCLK	CCLK

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Pin Information (continued)

Table 28. OR2T15A, OR2T26A, and OR2T40A/B 432-Pin EBGA Pinout (continued)

Pin	2T15A Pad	2T26A Pad	2T40A/B Pad	Function
B4	PT20B	PT24B	PT29B	I/O
A4	PT20A	PT24A	PT29A	I/O
D6	PT19D	PT23D	PT28D	I/O
C5	PT19C	PT23C	PT28C	I/O
B5	PT19B	PT23B	PT28B	I/O
A5	PT19A	PT23A	PT28A	I/O-RDY/RCLK
C6	PT18D	PT22D	PT27D	I/O
B6	PT18C	PT22C	PT27C	I/O
A6	PT18B	PT22B	PT27B	I/O
D8	PT18A	PT22A	PT27A	I/O
C7	PT17D	PT21D	PT26D	I/O
B7	PT17C	PT21C	PT26C	I/O
A7	PT17B	PT21B	PT26B	I/O
D9	PT17A	PT21A	PT26A	I/O
C8	PT16D	PT20D	PT25D	I/O-D7
B8	PT16C	PT20C	PT25C	I/O
C9	PT16B	PT20B	PT25B	I/O
D10	PT16A	PT20A	PT25A	I/O
B9	PT15D	PT19D	PT24D	I/O-VDD5
A9	PT15C	PT19C	PT24C	I/O
C10	PT15B	PT19B	PT24B	I/O
B10	PT15A	PT19A	PT23D	I/O
A10	PT14D	PT18D	PT22D	I/O
C11	PT14C	PT18C	PT22A	I/O
D12	PT14B	PT18B	PT21D	I/O-D6
B11	PT14A	PT18A	PT21A	I/O
A11	PT13D	PT17D	PT20D	I/O
C12	PT13C	PT17A	PT20A	I/O
D13	—	PT16D	PT19D	I/O-VDD5
B12	PT13B	PT16B	PT19B	I/O
C13	PT13A	PT16A	PT19A	I/O-D5
B13	PT12D	PT15D	PT18D	I/O
D14	—	PT15B	PT18B	I/O
A13	PT12C	PT15A	PT18A	I/O
C14	PT12B	PT14D	PT17D	I/O
B14	—	PT14B	PT17B	I/O
A14	PT12A	PT14A	PT17A	I/O-D4
C15	PT11D	PT13D	PT16D	I/O
B15	PT11C	PT13C	PT16C	I/O
A15	PT11B	PT13B	PT16B	I/O
C16	PT11A	PT13A	PT16A	I/O-D3
D16	PT10D	PT12D	PT15D	I/O
B16	PT10C	PT12C	PT15C	I/O
A17	PT10B	PT12B	PT15B	I/O-VDD5

Notes:
The OR2T15A pin AG2 is not connected in the 432-pin EBGA package.

The pins labeled I/O-VDD5 are user I/Os for the OR2CxxA and OR2TxxB series, but they are connected to VDD5 for the OR2TxxA series.

Timing Characteristics (continued)

Table 35A. OR2CxxA and OR2TxxA Asynchronous Memory Read Characteristics (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C.
OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Operation (TJ = 85 °C, VDD = min):												
Read Cycle Time	TRC	3.6	—	2.7	—	2.4	—	2.3	—	2.0	—	ns
Data Valid after Address (A[3:0], B[3:0] to F[3:0])	MEM*_ADEL	—	2.8	—	2.1	—	1.7	—	1.4	—	1.3	ns
Read Operation, Clocking Data into Latch/Flip-flop (TJ = 85 °C, VDD = min):												
Address to Clock Setup Time (A[3:0], B[3:0] to CK)	MEM*_ASET	1.8	—	1.2	—	1.1	—	1.0	—	1.0	—	ns
Clock to PFU Out (CK to Q[3:0])—Register	REG_DEL	—	2.0	—	1.9	—	1.5	—	1.3	—	1.0	ns

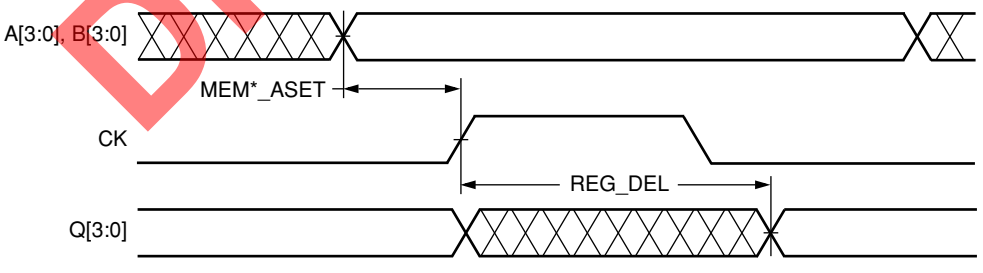
Table 35B. OR2TxxB Asynchronous Memory Read Characteristics (MA/MB Modes)

OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Read Operation (TJ = 85 °C, VDD = min):						
Read Cycle Time	TRC	1.9	—	1.8	—	ns
Data Valid after Address (A[3:0], B[3:0] to F[3:0])	MEM*_ADEL	—	1.3	—	1.0	ns
Read Operation, Clocking Data into Latch/Flip-flop (TJ = 85 °C, VDD = min):						
Address to Clock Setup Time (A[3:0], B[3:0] to CK)	MEM*_ASET	0.9	—	0.8	—	ns
Clock to PFU Out (CK to Q[3:0])—Register	REG_DEL	—	1.0	—	1.0	ns

5-3226(F).r4

Figure 55. Read Operation—Flip-Flop Bypass



5-3227(F).r4

Figure 56. Read Operation—LUT Memory Loading Flip-Flops

Timing Characteristics (continued)

Table 37A. OR2CxxA and OR2TxxA Asynchronous Memory Read During Write Operation (MA/MB Modes)

OR2CxxA Commercial: VDD = 5.0 V ± 5%, 0 °C ≤ TA ≤ 70 °C; OR2CxxA Industrial: VDD = 5.0 V ± 10%, –40 °C ≤ TA ≤ +85 °C. OR2TxxA Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxA Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed										Unit
		-3		-4		-5		-6		-7		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read During Write Operation (TJ = 85 °C, VDD = min):												
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.9	—	4.8	—	3.9	—	4.0	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	6.4	—	5.8	—	4.7	—	4.7	—	4.5	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	3.6	—	3.1	—	2.5	—	2.5	—	2.2	ns

Table 37B. OR2TxxB Asynchronous Memory Read During Write Operation (MA/MB Modes)

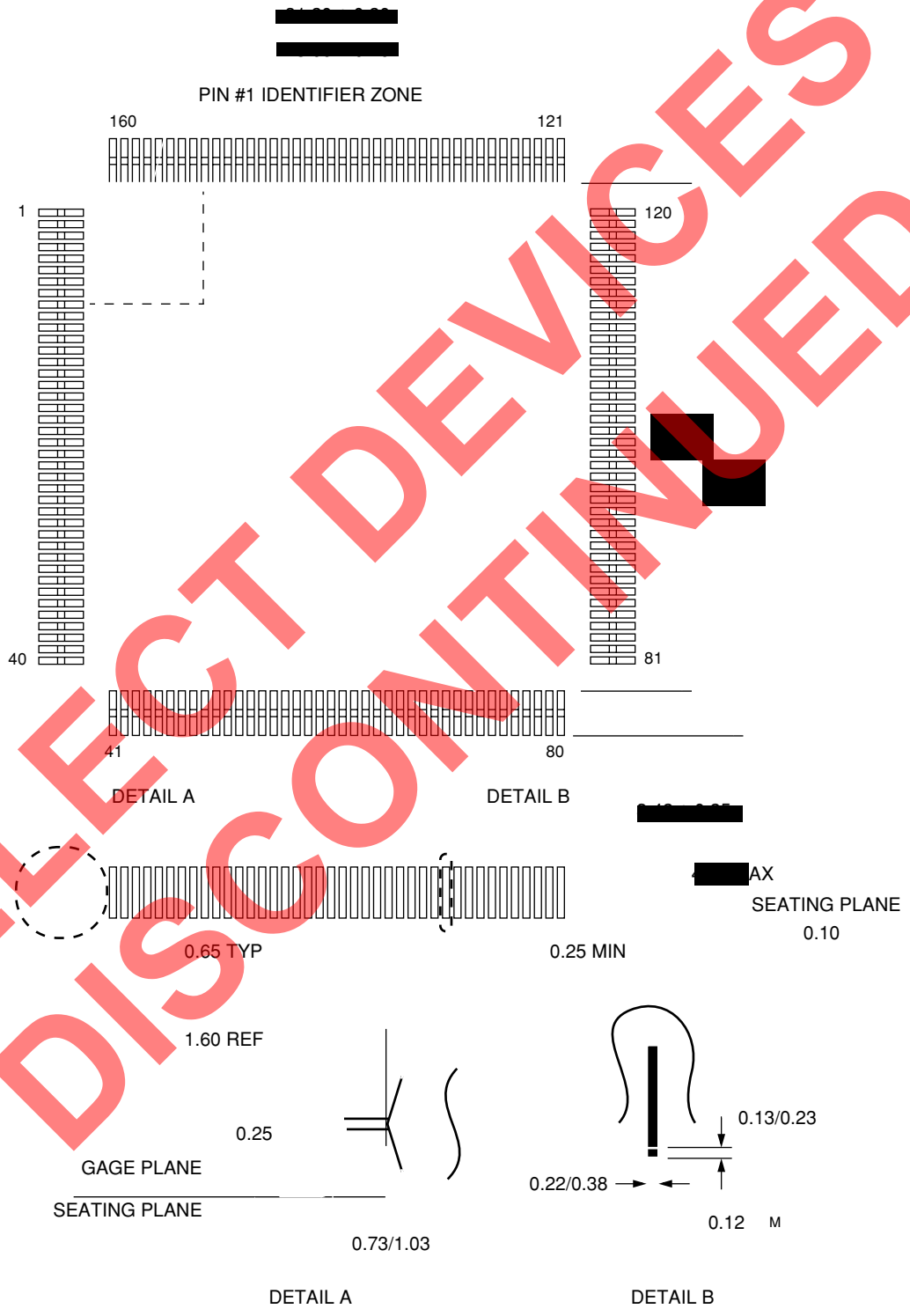
OR2TxxB Commercial: VDD = 3.0 V to 3.6 V, 0 °C ≤ TA ≤ 70 °C; OR2TxxB Industrial: VDD = 3.0 V to 3.6 V, –40 °C ≤ TA ≤ +85 °C.

Parameter	Symbol	Speed				Unit
		-7		-8		
		Min	Max	Min	Max	
Read During Write Operation (TJ = +85 °C, VDD = min):						
Write Enable (WREN) to PFU Output Delay (A4/B4 to F[3:0])	MEM*_WRDEL	—	4.5	—	3.9	ns
Write-port Enable (WPE) to PFU Output Delay (C0 to F[3:0])	MEM*_PWRDEL	—	4.6	—	4.0	ns
Data to PFU Output Delay (WD[3:0] to F[3:0])	MEM*_DDEL	—	2.7	—	2.4	ns

Package Outline Drawings (continued)

160-Pin QFP

Dimensions are in millimeters.



Package Outline Drawings (continued)

208-Pin SQFP2

Dimensions are in millimeters.

5-3828(F)

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2C12A	OR2C12A4M84-D[2]	4	PLCC	84	C	D
	OR2C12A4S208-DB[2]	4	SQFP	208	C	DB
	OR2C12A4S240-DB[2]	4	SQFP	240	C	DB
	OR2C12A4BA256-DB[2]	4	PBGA	256	C	DB
	OR2C12A4S304-DB[2]	4	SQFP	304	C	DB
	OR2C12A4BA352-DB[2]	4	PLCC	352	C	DB
	OR2C12A3S208-DB[2]	3	SQFP	208	C	DB
	OR2C12A3S240-DB[2]	3	SQFP	240	C	DB
OR2C15A	OR2C15A4M84-D[2]	4	PLCC	84	C	D
	OR2C15A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C15A4S208-DB[2]	4	SQFP	208	C	DB
	OR2C15A4S240-DB[2]	4	SQFP	240	C	DB
	OR2C15A4BA256-DB[2]	4	PBGA	256	C	DB
	OR2C15A4S304-DB[2]	4	SQFP	304	C	DB
	OR2C15A4BA352-DB[2]	4	EBGA	352	C	DB
OR2C26A	OR2C26A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C26A4PS240-DB[2]	4	SQFP2	240	C	DB
	OR2C26A4PS304-DB[2]	4	SQFP2	304	C	DB
OR2C40A	OR2C40A4PS208-DB[2]	4	SQFP2	208	C	DB
	OR2C40A4PS240-DB[2]	4	SQFP2	240	C	DB
	OR2C40A4PS304-DB[2]	4	SQFP2	304	C	DB
OR2T04A	OR2T04A5T100-DB[2]	5	TQFP	100	C	DB
	OR2T04A5T144-DB[2]	5	TQFP	144	C	DB
	OR2T04A5S208-DB[2]	5	SQFP	208	C	DB
	OR2T04A4T100-DB[2]	4	TQFP	100	C	DB
	OR2T04A4T144-DB[2]	4	TQFP	144	C	DB
	OR2T04A4S208-DB[2]	4	SQFP	208	C	DB
OR2T08A	OR2T08A5J160-DB[2]	5	QFP	160	C	DB
	OR2T08A5S208-DB[2]	5	SQFP	208	C	DB
	OR2T08A5S240-DB[2]	5	SQFP	240	C	DB
	OR2T08A5BA256-DB[2]	5	PBGA	256	C	DB
	OR2T08A4J160-DB[2]	4	QFP	160	C	DB
	OR2T08A4S208-DB[2]	4	SQFP	208	C	DB
	OR2T08A4S240-DB[2]	4	SQFP	240	C	DB
	OR2T08A4BA256-DB[2]	4	PBGA	256	C	DB

Commercial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2T40B	OR2T40B8PS208-DB[2]	8	SQFP2	208	C	DB
	OR2T40B8BA352-DB[2]	8	PBGA	352	C	DB
	OR2T40B8BC432-DB[2]	8	EBGA	432	C	DB
	OR2T40B7PS208-DB[2]	7	SQFP2	208	C	DB
	OR2T40B7BA352-DB[2]	7	PBGA	352	C	DB
	OR2T40B7BC432-DB[2]	7	EBGA	432	C	DB

Industrial

Device Family	Part Number	Speed Grade	Package Type	Pin/Ball Count	Grade	Packing Designator
OR2C04A	OR2C04A3T100I-DB[2]	3	TQFP	100	I	DB
	OR2C04A3T144I-DB[2]	3	TQFP	144	I	DB
	OR2C04A3S208I-DB[2]	3	SQFP	208	I	DB
OR2C06A	OR2C06A3T100I-DB[2]	3	TQFP	100	I	DB
	OR2C06A3T144I-DB[2]	3	TQFP	144	I	DB
	OR2C06A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C06A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C06A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C06A3BA256I-DB[2]	3	PBGA	256	I	DB
OR2C08A	OR2C08A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C08A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C08A3S240I-DB[2]	3	SQFP	240	I	DB
OR2C10A	OR2C10A3J160I-DB[2]	3	QFP	160	I	DB
	OR2C10A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C10A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C10A3BA352I-DB[2]	3	QFP	352	I	DB
OR2C12A	OR2C12A3M84I-D[2]	3	SQFP	84	I	D
	OR2C12A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C12A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C12A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C12A3S304I-DB[2]	3	SPBGA	304	I	DB
	OR2C12A3BA352I-DB[2]	3	PLCC	352	I	DB
OR2C15A	OR2C15A3M84I-D[2]	3	PLCC	84	I	D
	OR2C15A3S208I-DB[2]	3	SQFP	208	I	DB
	OR2C15A3PS208I-DB[2]	3	SQFP2	208	I	DB
	OR2C15A3S240I-DB[2]	3	SQFP	240	I	DB
	OR2C15A3PS240I-DB[2]	3	SQFP2	240	I	DB
	OR2C15A3BA256I-DB[2]	3	PBGA	256	I	DB
	OR2C15A3BA352I-DB[2]	3	PBGA	352	I	DB