# Infineon Technologies - SAF-XC164N-16F20F BB Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, SPI, UART/USART |
| Peripherals | PWM, WDT |
| Number of I/O | 79 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 2.7V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | PG-TQFP-100-16 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164n-16f20f-bb |

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**Table 2 Pin Definitions and Functions**

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| $\overline{\text{RSTIN}}$ | 1 | I | Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164N. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles.<br>*Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.* |
| P20.12 | 2 | IO | For details, please refer to the description of **P20**. |
| $\overline{\text{NMI}}$ | 3 | I | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164N into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode.<br>If not used, pin $\overline{\text{NMI}}$ should be pulled high externally. |
| P0H.0-P0H.3 | 4…7 | IO | For details, please refer to the description of **PORT0**. |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **P9** | | IO | Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special).<br>The following Port 9 pins also serve for alternate functions: |
| P9.0 | 10 | I/O | CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., |
| | | I | EX7IN Fast External Interrupt 7 Input (alternate pin B) |
| P9.1 | 11 | I/O | CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., |
| | | I | EX6IN Fast External Interrupt 6 Input (alternate pin B) |
| P9.2 | 12 | I/O | CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., |
| | | I | EX7IN Fast External Interrupt 7 Input (alternate pin A) |
| P9.3 | 13 | I/O | CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., |
| | | I | EX6IN Fast External Interrupt 6 Input (alternate pin A) |
| P9.4 | 14 | I/O | CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp. |
| P9.5 | 15 | I/O | CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp. |
| **P5** | | I | Port 5 is a 14-bit input-only port.<br>Some pins of Port 5 serve as timer inputs: |
| P5.0 | 18 | I | No Alternate Function beside General Purpose Input |
| P5.1 | 19 | I | No Alternate Function beside General Purpose Input |
| P5.2 | 20 | I | No Alternate Function beside General Purpose Input |
| P5.3 | 21 | I | No Alternate Function beside General Purpose Input |
| P5.4 | 22 | I | No Alternate Function beside General Purpose Input |
| P5.5 | 23 | I | T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp. |
| P5.10 | 24 | I | T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp. |
| P5.11 | 25 | I | |
| P5.6 | 26 | I | |
| P5.7 | 27 | I | T6IN GPT2 Timer T6 Count/Gate Input |
| P5.12 | 30 | I | T5IN GPT2 Timer T5 Count/Gate Input |
| P5.13 | 31 | I | T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp. |
| P5.14 | 32 | I | T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp. |
| P5.15 | 33 | I | |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function | |
|---|---|---|---|---|
| **P4** | | IO | Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special).<br>Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines: | |
| P4.0 | 53 | O | $\overline{\text{A16}}$ | Least Significant Segment Address Line, |
| | | O | $\overline{\text{CS3}}$ | Chip Select 3 Output |
| P4.1 | 54 | O | $\overline{\text{A17}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS2}}$ | Chip Select 2 Output |
| P4.2 | 55 | O | $\overline{\text{A18}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS1}}$ | Chip Select 1 Output |
| P4.3 | 56 | O | $\overline{\text{A19}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS0}}$ | Chip Select 0 Output |
| P4.4 | 57 | O | A20 | Segment Address Line, |
| | | I | EX5IN | Fast External Interrupt 5 Input (alternate pin B) |
| P4.5 | 58 | O | A21 | Segment Address Line, |
| | | I | EX4IN | Fast External Interrupt 4 Input (alternate pin B) |
| P4.6 | 59 | O | A22 | Segment Address Line, |
| | | I | EX5IN | Fast External Interrupt 5 Input (alternate pin A) |
| P4.7 | 60 | O | A23 | Most Significant Segment Address Line, |
| | | I | EX4IN | Fast External Interrupt 4 Input (alternate pin A) |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| **PORT1** (cont'd) | | IO | …continued… |
| P1H.0 | 89 | I | $\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input, |
| | | I | EX0IN Fast External Interrupt 0 Input (default pin), |
| | | I/O | $\overline{\text{CC23IO}}$ CAPCOM2: CC23 Capture Inp./Compare Outp. |
| P1H.1 | 90 | I | $\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input, |
| | | I | EX1IN Fast External Interrupt 1 Input (default pin), |
| | | I/O | $\overline{\text{MRST1}}$ SSC1 Master-Receive/Slave-Transmit In/Out. |
| P1H.2 | 91 | I | $\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input, |
| | | I | EX2IN Fast External Interrupt 2 Input (default pin), |
| | | I/O | MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp. |
| P1H.3 | 92 | I | T7IN CAPCOM2: Timer T7 Count Input, |
| | | I/O | SCLK1 SSC1 Master Clock Output / Slave Clock Input, |
| | | I | EX3IN Fast External Interrupt 3 Input (default pin), |
| | | I | EX0IN Fast External Interrupt 0 Input (alternate pin A) |
| P1H.4 | 93 | I/O | CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp., |
| | | I | EX4IN Fast External Interrupt 4 Input (default pin) |
| P1H.5 | 94 | I/O | CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp., |
| | | I | EX5IN Fast External Interrupt 5 Input (default pin) |
| P1H.6 | 95 | I/O | CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp., |
| | | I | EX6IN Fast External Interrupt 6 Input (default pin) |
| P1H.7 | 96 | I/O | CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp., |
| | | I | EX7IN Fast External Interrupt 7 Input (default pin) |
| $\overline{\text{XTAL2}}$ | 99 | O | XTAL2: Output of the oscillator amplifier circuit |
| XTAL1 | 100 | I | XTAL1: Input to the oscillator amplifier and input to the internal clock generator<br>To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. |
| *res* | 28 | - | pin is reserved and connected to $V_{DDP}$ |
| *res* | 29 | - | pin is reserved and connected to $V_{SSP}$ |
| $V_{DDI}$ | 35, 97 | - | Digital Core Supply Voltage (On-Chip Modules):<br>+2.5 V during normal operation and idle mode.<br>Please refer to the **Operating Conditions** |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function |
|---|---|---|---|
| $V_{DDP}$ | 9, 17, 38, 61, 87 | - | Digital Pad Supply Voltage (Pin Output Drivers):<br>+5 V during normal operation and idle mode.<br>Please refer to the **Operating Conditions** |
| $V_{SSI}$ | 34, 98 | - | **Digital Ground.**<br>Connect decoupling capacitors to adjacent $V_{DD}$/$V_{SS}$ pin pairs as close as possible to the pins.<br>All $V_{SS}$ pins must be connected to the ground-line or ground-plane. |
| $V_{SSP}$ | 8, 16, 37, 62, 88 | - | |

## 3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes[1)], which are as follows:

– 16 … 24-bit Addresses, 16-bit Data, Demultiplexed
– 16 … 24-bit Addresses, 16-bit Data, Multiplexed
– 16 … 24-bit Addresses, 8-bit Data, Multiplexed
– 16 … 24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output. The high order address (segment) lines use Port 4. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines are assigned to Port 4.

Up to 4 external $\overline{CS}$ signals (3 windows plus default) can be generated in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

The EBC also controls accesses to resources connected to the on-chip LXBus. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

## 3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164N is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164N supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164N has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

**Table 4** shows all of the possible XC164N interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).*

**Table 4 XC164N Interrupt Nodes** (cont'd)

| Source of Interrupt or PEC Service Request | Control Register | Vector Location[1)] | Trap Number |
|---|---|---|---|
| CAPCOM6 Timer T13 | CCU6_T13IC | xx'0138$_H$ | 4E$_H$ / 78$_D$ |
| CAPCOM6 Emergency | CCU6_EIC | xx'013C$_H$ | 4F$_H$ / 79$_D$ |
| CAPCOM6 | CCU6_IC | xx'0140$_H$ | 50$_H$ / 80$_D$ |
| SSC1 Transmit | SSC1_TIC | xx'0144$_H$ | 51$_H$ / 81$_D$ |
| SSC1 Receive | SSC1_RIC | xx'0148$_H$ | 52$_H$ / 82$_D$ |
| SSC1 Error | SSC1_EIC | xx'014C$_H$ | 53$_H$ / 83$_D$ |
| Unassigned node | --- | xx'0150$_H$ | 54$_H$ / 84$_D$ |
| Unassigned node | --- | xx'0154$_H$ | 55$_H$ / 85$_D$ |
| Unassigned node | --- | xx'0158$_H$ | 56$_H$ / 86$_D$ |
| Unassigned node | --- | xx'015C$_H$ | 57$_H$ / 87$_D$ |
| Unassigned node | --- | xx'0164$_H$ | 59$_H$ / 89$_D$ |
| Unassigned node | --- | xx'0168$_H$ | 5A$_H$ / 90$_D$ |
| Unassigned node | --- | xx'016C$_H$ | 5B$_H$ / 91$_D$ |
| Unassigned node | --- | xx'0170$_H$ | 5C$_H$ / 92$_D$ |
| Unassigned node | --- | xx'0174$_H$ | 5D$_H$ / 93$_D$ |
| Unassigned node | --- | xx'0100$_H$ | 40$_H$ / 64$_D$ |
| Unassigned node | --- | xx'0104$_H$ | 41$_H$ / 65$_D$ |
| Unassigned node | --- | xx'012C$_H$ | 4B$_H$ / 75$_D$ |
| Unassigned node | --- | xx'00FC$_H$ | 3F$_H$ / 63$_D$ |
| Unassigned node | --- | xx'0160$_H$ | 58$_H$ / 88$_D$ |

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

2) The interrupt nodes assigned to ASC1 are only available in derivatives including the ASC1. Otherwise, they are unassigned nodes.

The XC164N also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

**Table 5** shows all of the possible exceptions or error conditions that can arise during run-time:

**Table 5 Hardware Trap Summary**

| Exception Condition | Trap Flag | Trap Vector | Vector Location[1)] | Trap Number | Trap Priority |
|---|---|---|---|---|---|
| Reset Functions: | – | | | | |
| – Hardware Reset | | RESET | xx’0000$_H$ | 00$_H$ | III |
| – Software Reset | | RESET | xx’0000$_H$ | 00$_H$ | III |
| – W-dog Timer Overflow | | RESET | xx’0000$_H$ | 00$_H$ | III |
| Class A Hardware Traps: | | | | | |
| – Non-Maskable Interrupt | NMI | NMITRAP | xx’0008$_H$ | 02$_H$ | II |
| – Stack Overflow | STKOF | STOTRAP | xx’0010$_H$ | 04$_H$ | II |
| – Stack Underflow | STKUF | STUTRAP | xx’0018$_H$ | 06$_H$ | II |
| – Software Break | SOFTBRK | SBRKTRAP | xx’0020$_H$ | 08$_H$ | II |
| Class B Hardware Traps: | | | | | |
| – Undefined Opcode | UNDOPC | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| – PMI Access Error | PACER | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| – Protected Instruction Fault | PRTFLT | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| – Illegal Word Operand Access | ILLOPA | BTRAP | xx’0028$_H$ | 0A$_H$ | I |
| Reserved | – | – | [2C$_H$ – 3C$_H$] | [0B$_H$ – 0F$_H$] | – |
| Software Traps<br>– TRAP Instruction | – | – | Any [xx’0000$_H$ – xx’01FC$_H$] in steps of 4$_H$ | Any [00$_H$ – 7F$_H$] | Current CPU Priority |

1) Register VECSEG defines the segment where the vector table is located to.

## 3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC164N. The user software running on the XC164N can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface or via the external bus interface for increased performance.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 break lines) to communicate with external circuitry. These interface signals are realized as alternate functions on Port 3 pins.

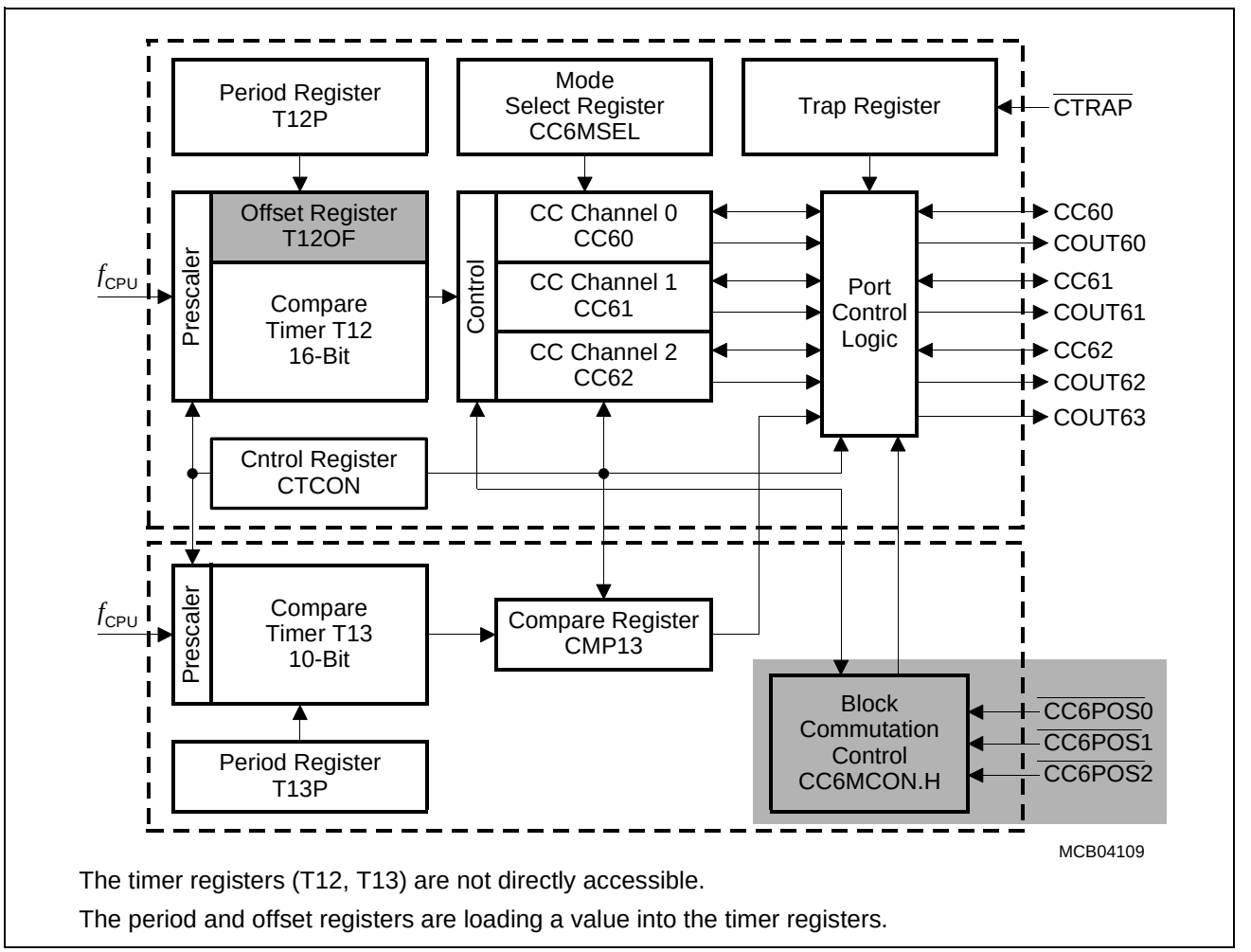
Complete system emulation is supported by the New Emulation Technology (NET) interface. Via this full-featured emulation interface (including internal buses, control, status, and pad signals) the XC164N chip can be connected to a NET carrier chip.

The use of the XC164N production chip together with the carrier chip provides superior emulation behavior, because the emulation system shows exactly the same functionality as the production chip (use of the identical silicon).

## 3.7 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.




The timer registers (T12, T13) are not directly accessible.

The period and offset registers are loading a value into the timer registers.

**Figure 6 CAPCOM6 Block Diagram**

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

## 3.16 Instruction Set Summary

Table 8 lists the instructions of the XC164N in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **“Instruction Set Manual”**.

This document also provides a detailled description of each instruction.

**Table 8 Instruction Set Summary**

| Mnemonic | Description | Bytes |
|---|---|---|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16-16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| (X)OR(B) | Bitwise (exclusive)OR, (word/byte operands) | 2 / 4 |
| BCLR / BSET | Clear/Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND / BOR / BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH / BFLDL | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL / SHR | Shift left/right direct word GPR | 2 |
| ROL / ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |

## 4.3 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164N. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 11 Operating Condition Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Digital supply voltage for the core | $V_{DDI}$ | 2.35 | 2.7 | V | Active mode, $f_{CPU} = f_{CPUmax}$ 1) |
| Digital supply voltage for IO pads | $V_{DDP}$ | 4.4 | 5.5 | V | Active mode 2) 3) |
| Supply Voltage Difference | $\Delta V_{DD}$ | -0.5 | – | V | $V_{DDP}$ - $V_{DDI}$ 4) |
| Digital ground voltage | $V_{SS}$ | 0 | | V | Reference voltage |
| Overload current | $I_{OV}$ | -5 | 5 | mA | Per IO pin 5)6) |
| | | -2 | 5 | mA | Per analog input pin 5)6) |
| Overload current coupling factor for analog inputs 7) | $K_{OVA}$ | – | $1.0 \times 10^{-4}$ | – | $I_{OV} > 0$ |
| | | – | $1.5 \times 10^{-3}$ | – | $I_{OV} < 0$ |
| Overload current coupling factor for digital I/O pins 7) | $K_{OVD}$ | – | $5.0 \times 10^{-3}$ | – | $I_{OV} > 0$ |
| | | – | $1.0 \times 10^{-2}$ | – | $I_{OV} < 0$ |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ | – | 50 | mA | 6) |
| External Load Capacitance | $C_L$ | – | 50 | pF | Pin drivers in **default** mode 8) |
| Ambient temperature | $T_A$ | 0 | 70 | °C | SAB-XC164N … |
| | | -40 | 85 | °C | SAF-XC164N … |
| | | -40 | 125 | °C | SAK-XC164N … |

1) $f_{CPUmax}$ = 40 MHz for devices marked …40F, $f_{CPUmax}$ = 20 MHz for devices marked …20F.

2) External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating level.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of $V_{DDP}$ = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

## 4.5 DC Parameters

**DC Characteristics**
(Operating Conditions apply)[1)]

| Parameter | Symbol | | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Input low voltage TTL (all except XTAL1) | $V_{IL}$ | SR | -0.5 | $0.2 \times V_{DDP}$ - 0.1 | V | – |
| Input low voltage XTAL1 | $V_{ILC}$ | SR | -0.5 | $0.3 \times V_{DDI}$ | V | – |
| Input low voltage (Special Threshold) | $V_{ILS}$ | SR | -0.5 | $0.45 \times V_{DDP}$ | V | 2) |
| Input high voltage TTL (all except XTAL1) | $V_{IH}$ | SR | $0.2 \times V_{DDP}$ + 0.9 | $V_{DDP}$ + 0.5 | V | – |
| Input high voltage XTAL1 | $V_{IHC}$ | SR | $0.7 \times V_{DDI}$ | $V_{DDI}$ + 0.5 | V | – |
| Input high voltage (Special Threshold) | $V_{IHS}$ | SR | $0.8 \times V_{DDP}$ - 0.2 | $V_{DDP}$ + 0.5 | V | 2) |
| Input Hysteresis (Special Threshold) | HYS | | $0.04 \times V_{DDP}$ | – | V | $V_{DDP}$ in [V], Series resistance = 0 Ω[2)] |
| Output low voltage | $V_{OL}$ | CC | – | 1.0 | V | $I_{OL} \le I_{OLmax}$ 3) |
| | | | – | 0.45 | V | $I_{OL} \le I_{OLnom}$ 3) 4) |
| Output high voltage[5)] | $V_{OH}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH} \ge I_{OHmax}$ 3) |
| | | | $V_{DDP}$ - 0.45 | – | V | $I_{OH} \ge I_{OHnom}$ 3) 4) |
| Input leakage current (Port 5)[6)] | $I_{OZ1}$ | CC | – | ±300 | nA | 0 V < $V_{IN}$ < $V_{DDP}$, $T_A \le 125$ °C |
| | | | | ±200 | nA | 0 V < $V_{IN}$ < $V_{DDP}$, $T_A \le 85$ °C[12)] |
| Input leakage current (all other)[6)] | $I_{OZ2}$ | CC | – | ±500 | nA | 0.45 V < $V_{IN}$ < $V_{DDP}$ |
| Configuration pull-up current[7)] | $I_{CPUH}$ 8) | | – | -10 | µA | $V_{IN} = V_{IHmin}$ |
| | $I_{CPUL}$ 9) | | -100 | – | µA | $V_{IN} = V_{ILmax}$ |

**DC Characteristics** (cont'd)
(Operating Conditions apply)[1)]

| Parameter | Symbol | | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Configuration pull-down current[10)] | $I_{CPDL}$ | 8) | – | 10 | µA | $V_{IN} = V_{ILmax}$ |
| | $I_{CPDH}$ | 9) | 120 | – | µA | $V_{IN} = V_{IHmin}$ |
| Level inactive hold current[11)] | $I_{LHI}$ | 8) | – | -10 | µA | $V_{OUT} = 0.5 \times V_{DDP}$ |
| Level active hold current[11)] | $I_{LHA}$ | 9) | -100 | – | µA | $V_{OUT}$ = 0.45 V |
| XTAL1 input current | $I_{IL}$ | CC | – | ±20 | µA | 0 V < $V_{IN}$ < $V_{DDI}$ |
| Pin capacitance[12)] (digital inputs/outputs) | $C_{IO}$ | CC | – | 10 | pF | |

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

2) This parameter is tested for P2, P3, P4, P9.

3) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

4) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

5) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

6) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor $K_{OV}$.

7) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0.

8) The maximum current may be drawn while the respective signal line remains inactive.

9) The minimum current must be drawn to drive the respective signal line active.

10) This specification is valid during Reset for configuration on ALE.

11) This specification is valid during Reset for pins P4.3-0, which can act as $\overline{CS}$ outputs.

12) Not subject to production test - verified by design/characterization.

**Table 12 Current Limits for Port Output Drivers**

| Port Output Driver Mode | Maximum Output Current ($I_{OLmax}$, $-I_{OHmax}$)[1] | Nominal Output Current ($I_{OLnom}$, $-I_{OHnom}$) |
|---|---|---|
| **Strong driver** | 10 mA | 2.5 mA |
| **Medium driver** | 4.0 mA | 1.0 mA |
| **Weak driver** | 0.5 mA | 0.1 mA |

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring port output pins the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma -I_{OH}$) must remain below 50 mA.

## Power Consumption XC164N

(Operating Conditions apply)

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Power supply current (active) with all peripherals active | $I_{DDI}$ | – | $15 + 2.6 \times f_{CPU}$ | mA | [1] $f_{CPU}$ in [MHz][2] |
| Pad supply current | $I_{DDP}$ | – | 5 | mA | [3] |
| Idle mode supply current with all peripherals active | $I_{IDX}$ | – | $15 + 1.2 \times f_{CPU}$ | mA | $f_{CPU}$ in [MHz][2] |
| Sleep and Power-down mode supply current caused by leakage[4] | $I_{PDL}$[5] | – | $128{,}000 \times e^{-\alpha}$ | mA | $V_{DDI}=V_{DDImax}$[6] $T_J$ in [°C] $\alpha = 4670/(273+T_J)$ |
| Sleep and Power-down mode supply current caused by leakage and the RTC running, clocked by the main oscillator[4] | $I_{PDM}$[7] | – | $0.6 + 0.02 \times f_{OSC} + I_{PDL}$ | mA | $V_{DDI}=V_{DDImax}$ $f_{OSC}$ in [MHz] |

1) During Flash programming or erase operations the supply current is increased by max. 5 mA.

2) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at $V_{DDImax}$ and maximum CPU clock frequency with all outputs disconnected and all inputs at $V_{IL}$ or $V_{IH}$.

3) The pad supply voltage pins ($V_{DDP}$) mainly provides the current consumed by the pin output drivers. A small amount of current is consumed even though no outputs are driven, because the drivers' input stages are switched and also the Flash module draws some power from the $V_{DDP}$ supply.

4) The total supply current in Sleep and Power-down mode is the sum of the temperature dependent leakage current and the frequency dependent current for RTC and main oscillator (if active).

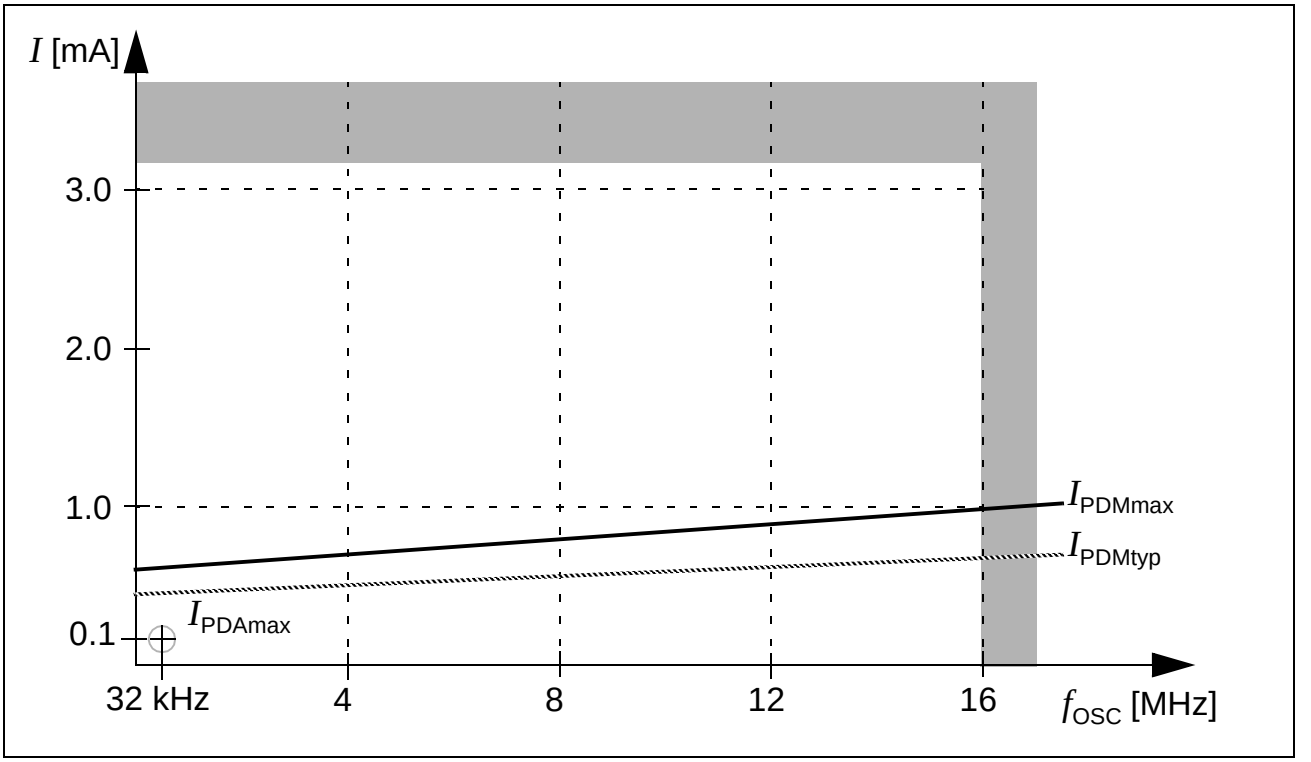



**Figure 11** **Sleep and Power Down Supply Current due to RTC and Oscillator running, as a Function of Oscillator Frequency**

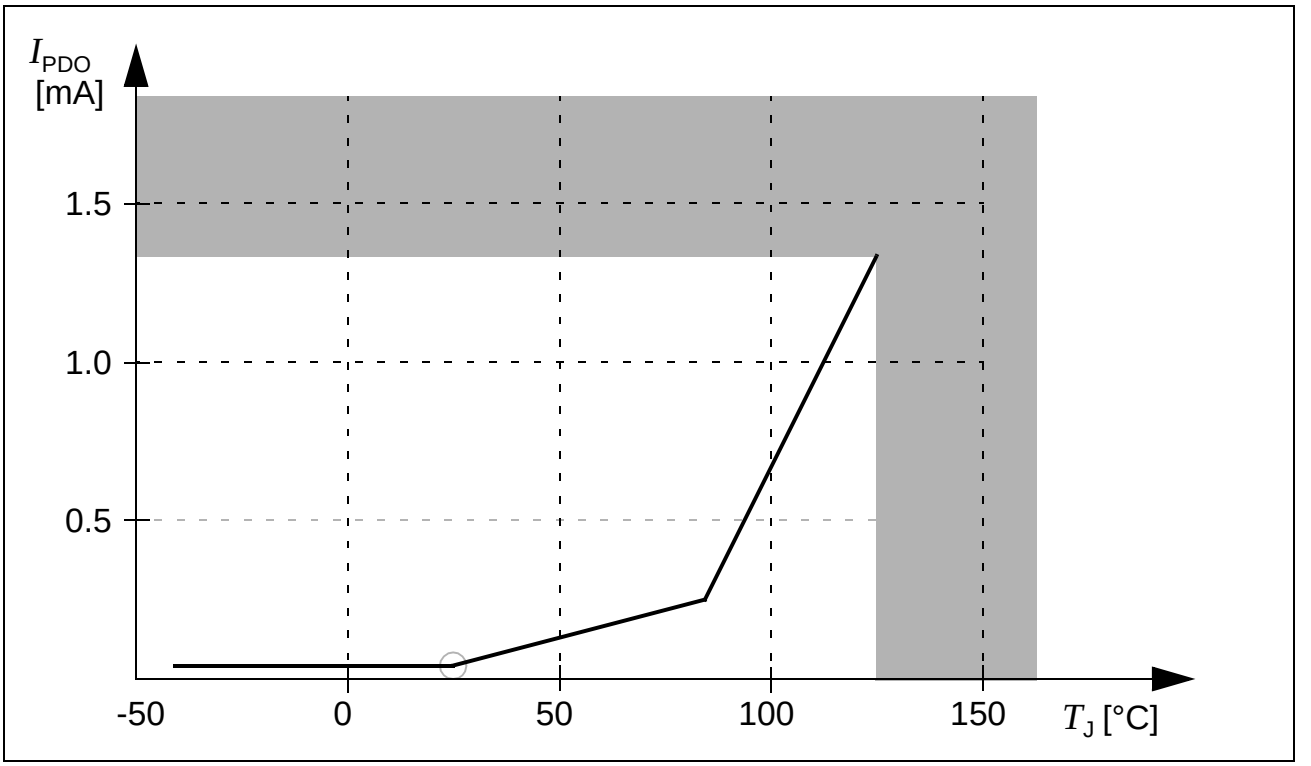



**Figure 12** **Sleep and Power Down Leakage Supply Current as a Function of Temperature**

# 5 Timing Parameters

## 5.1 Definition of Internal Timing

The internal operation of the XC164N is controlled by the internal master clock $f_{MC}$.

The master clock signal $f_{MC}$ can be generated from the oscillator clock signal $f_{OSC}$ via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate $f_{MC}$. This influence must be regarded when calculating the timings for the XC164N.

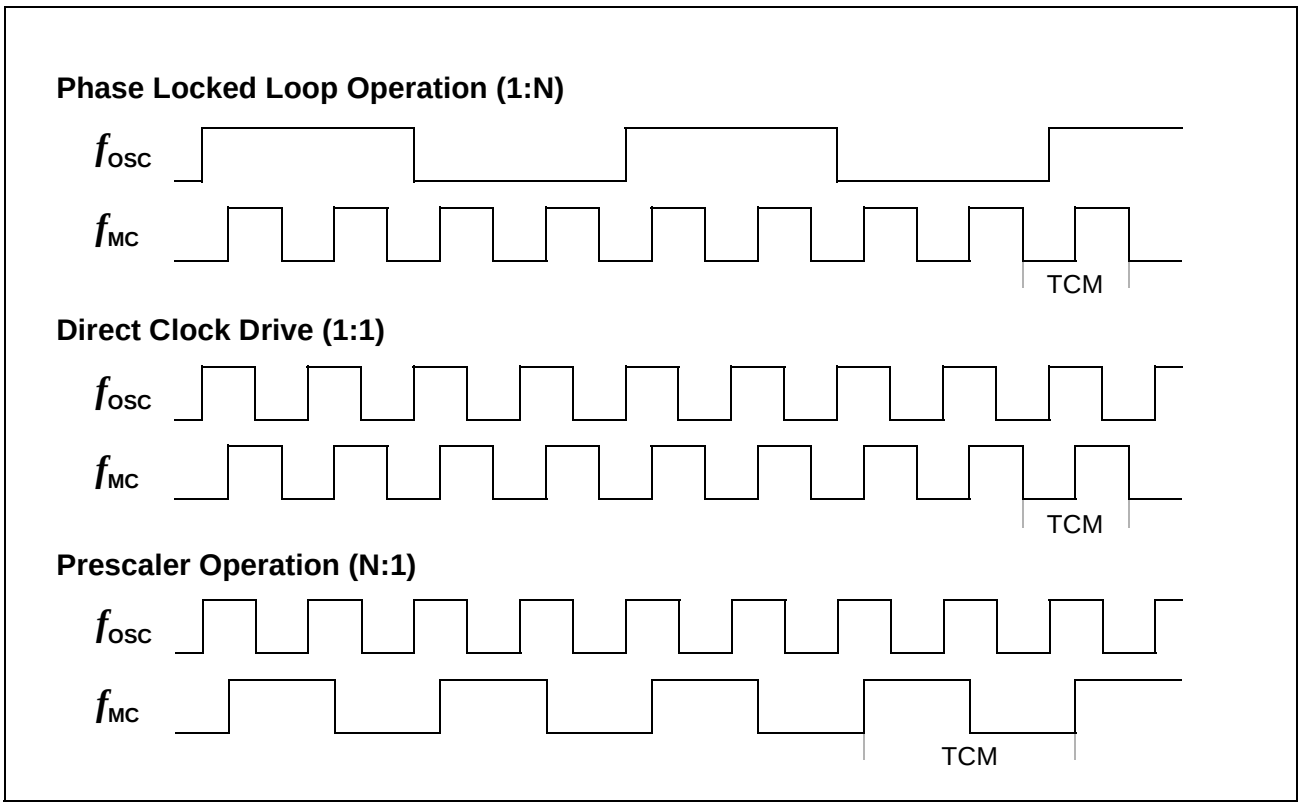



**Figure 13 Generation Mechanisms for the Master Clock**

*Note: The example for PLL operation shown in **Figure 13** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal $f_{CPU}$. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal $f_{SYS}$ which has the same frequency as the CPU clock signal $f_{CPU}$.

**Table 17 External Bus Cycle Timing** (Operating Conditions apply)

| Parameter | Symbol | | Limits | | Unit |
|---|---|---|---|---|---|
| | | | min. | max. | |
| Output valid delay for: RD, WR(L/H) | $tc_{10}$ | CC | 1 | 15 | ns |
| Output valid delay for: BHE, ALE | $tc_{11}$ | CC | -1 | 8 | ns |
| Output valid delay for: A23…A16, A15…A0 (on PORT1) | $tc_{12}$ | CC | 3 | 18 | ns |
| Output valid delay for: A15…A0 (on PORT0) | $tc_{13}$ | CC | 3 | 18 | ns |
| Output valid delay for: CS | $tc_{14}$ | CC | 3 | 16 | ns |
| Output valid delay for: D15…D0 (write data, mux-mode) | $tc_{15}$ | CC | 3 | 19 | ns |
| Output valid delay for: D15…D0 (write data, demux-mode) | $tc_{16}$ | CC | 2 | 16 | ns |
| Output hold time for: RD, WR(L/H) | $tc_{20}$ | CC | -3 | 4 | ns |
| Output hold time for: BHE, ALE | $tc_{21}$ | CC | 0 | 11 | ns |
| Output hold time for: A23…A16, A15…A0 (on PORT0) | $tc_{23}$ | CC | 1 | 13 | ns |
| Output hold time for: CS | $tc_{24}$ | CC | -2 | 4 | ns |
| Output hold time for: D15…D0 (write data) | $tc_{25}$ | CC | 1 | 13 | ns |
| Input setup time for: D15…D0 (read data) | $tc_{30}$ | SR | 29 | – | ns |
| Input hold time D15…D0 (read data)[1)] | $tc_{31}$ | SR | -5 | – | ns |

1) Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of RD. Therefore address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of RD

*Note: The shaded parameters have been verified by characterization. They are not subject to production test.*