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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | EBI/EMI, SPI, UART/USART |
| Peripherals | PWM, WDT |
| Number of I/O | 79 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.35V ~ 2.7V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | PG-TQFP-100-5 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164n-8f20f-bb |

| **Revision History:** | **2005-01** | V1.0 |
|---|---|---|
| Previous Version: | None | |

| Page | Subjects (major changes since last revision) |
|---|---|
| | |
| | |

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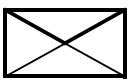


## 2.2 Pin Configuration and Definition

The pins of the XC164N are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) marks pins to be used as alternate external interrupt inputs.

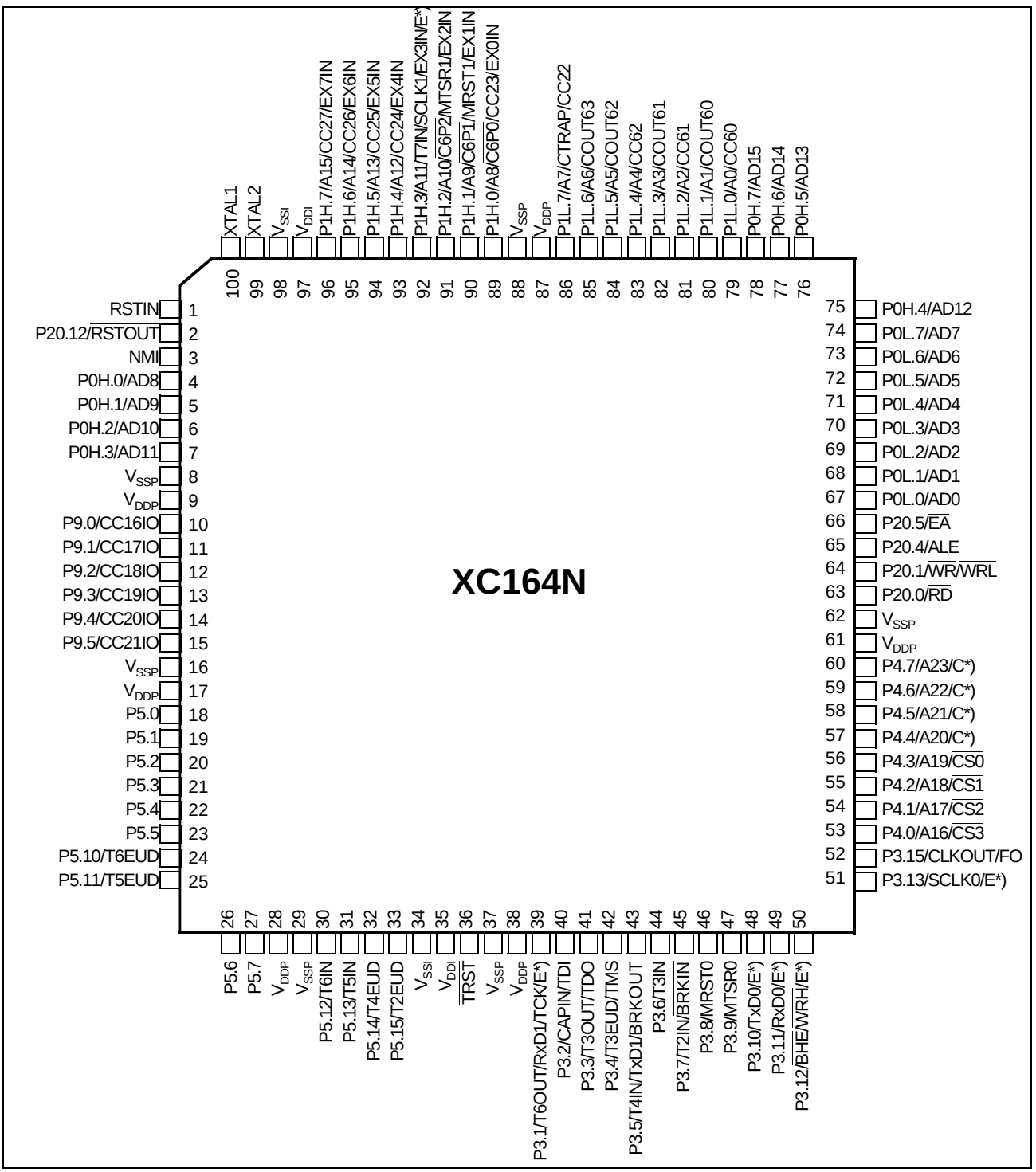



**Figure 2 Pin Configuration (top view)**

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Num. | Input Outp. | Function | |
|---|---|---|---|---|
| **P4** | | IO | Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special).<br>Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines: | |
| P4.0 | 53 | O | $\overline{\text{A16}}$ | Least Significant Segment Address Line, |
| | | O | $\overline{\text{CS3}}$ | Chip Select 3 Output |
| P4.1 | 54 | O | $\overline{\text{A17}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS2}}$ | Chip Select 2 Output |
| P4.2 | 55 | O | $\overline{\text{A18}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS1}}$ | Chip Select 1 Output |
| P4.3 | 56 | O | $\overline{\text{A19}}$ | Segment Address Line, |
| | | O | $\overline{\text{CS0}}$ | Chip Select 0 Output |
| P4.4 | 57 | O | A20 | Segment Address Line, |
| | | I | EX5IN | Fast External Interrupt 5 Input (alternate pin B) |
| P4.5 | 58 | O | A21 | Segment Address Line, |
| | | I | EX4IN | Fast External Interrupt 4 Input (alternate pin B) |
| P4.6 | 59 | O | A22 | Segment Address Line, |
| | | I | EX5IN | Fast External Interrupt 5 Input (alternate pin A) |
| P4.7 | 60 | O | A23 | Most Significant Segment Address Line, |
| | | I | EX4IN | Fast External Interrupt 4 Input (alternate pin A) |

so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

**1024 bytes (2 × 512 bytes)** of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC166 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

**Table 3 XC164N Memory Map[1)]**

| Address Area | Start Loc. | End Loc. | Area Size[2)] | Notes |
|---|---|---|---|---|
| Flash register space | $FF'F000_H$ | $FF'FFFF_H$ | 4 Kbytes | Flash only[3)] |
| *Reserved (Acc. trap)* | $F8'0000_H$ | $FF'EFFF_H$ | <0.5 Mbytes | Minus Flash regs |
| *Reserved for PSRAM* | $E0'0800_H$ | $F7'FFFF_H$ | <1.5 Mbytes | Minus PSRAM |
| Program SRAM | $E0'0000_H$ | $E0'07FF_H$ | 2 Kbytes | Maximum |
| *Reserved for pr. mem.* | $C2'0000_H$ | $DF'FFFF_H$ | < 2 Mbytes | Minus Flash |
| Program Flash | $C0'0000_H$ | $C1'FFFF_H$ | 128 Kbytes | up to 128 Kbytes |
| *Reserved* | $BF'0000_H$ | $BF'FFFF_H$ | 64 Kbytes | |
| External memory area | $40'0000_H$ | $BE'FFFF_H$ | < 8 Mbytes | Minus res. seg. |
| External IO area[4)] | $20'0800_H$ | $3F'FFFF_H$ | < 2 Mbytes | |
| *Reserved* | $20'0000_H$ | $20'07FF_H$ | 2 Kbytes | |
| External memory area | $01'0000_H$ | $1F'FFFF_H$ | < 2 Mbytes | Minus segment 0 |
| Data RAMs and SFRs | $00'8000_H$ | $00'FFFF_H$ | 32 Kbytes | Partly used |
| External memory area | $00'0000_H$ | $00'7FFF_H$ | 32 Kbytes | |

1) Accesses to the shaded areas generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) Not defined register locations return a trap code.

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164N instruction set which includes the following instruction classes:

– Standard Arithmetic Instructions
– DSP-Oriented Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

## 3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC164N is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC164N supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC164N has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

**Table 4** shows all of the possible XC164N interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

*Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).*

**Table 4 XC164N Interrupt Nodes** (cont'd)

| Source of Interrupt or PEC Service Request | Control Register | Vector Location[1)] | Trap Number |
|---|---|---|---|
| CAPCOM6 Timer T13 | CCU6_T13IC | xx'0138$_H$ | 4E$_H$ / 78$_D$ |
| CAPCOM6 Emergency | CCU6_EIC | xx'013C$_H$ | 4F$_H$ / 79$_D$ |
| CAPCOM6 | CCU6_IC | xx'0140$_H$ | 50$_H$ / 80$_D$ |
| SSC1 Transmit | SSC1_TIC | xx'0144$_H$ | 51$_H$ / 81$_D$ |
| SSC1 Receive | SSC1_RIC | xx'0148$_H$ | 52$_H$ / 82$_D$ |
| SSC1 Error | SSC1_EIC | xx'014C$_H$ | 53$_H$ / 83$_D$ |
| Unassigned node | --- | xx'0150$_H$ | 54$_H$ / 84$_D$ |
| Unassigned node | --- | xx'0154$_H$ | 55$_H$ / 85$_D$ |
| Unassigned node | --- | xx'0158$_H$ | 56$_H$ / 86$_D$ |
| Unassigned node | --- | xx'015C$_H$ | 57$_H$ / 87$_D$ |
| Unassigned node | --- | xx'0164$_H$ | 59$_H$ / 89$_D$ |
| Unassigned node | --- | xx'0168$_H$ | 5A$_H$ / 90$_D$ |
| Unassigned node | --- | xx'016C$_H$ | 5B$_H$ / 91$_D$ |
| Unassigned node | --- | xx'0170$_H$ | 5C$_H$ / 92$_D$ |
| Unassigned node | --- | xx'0174$_H$ | 5D$_H$ / 93$_D$ |
| Unassigned node | --- | xx'0100$_H$ | 40$_H$ / 64$_D$ |
| Unassigned node | --- | xx'0104$_H$ | 41$_H$ / 65$_D$ |
| Unassigned node | --- | xx'012C$_H$ | 4B$_H$ / 75$_D$ |
| Unassigned node | --- | xx'00FC$_H$ | 3F$_H$ / 63$_D$ |
| Unassigned node | --- | xx'0160$_H$ | 58$_H$ / 88$_D$ |

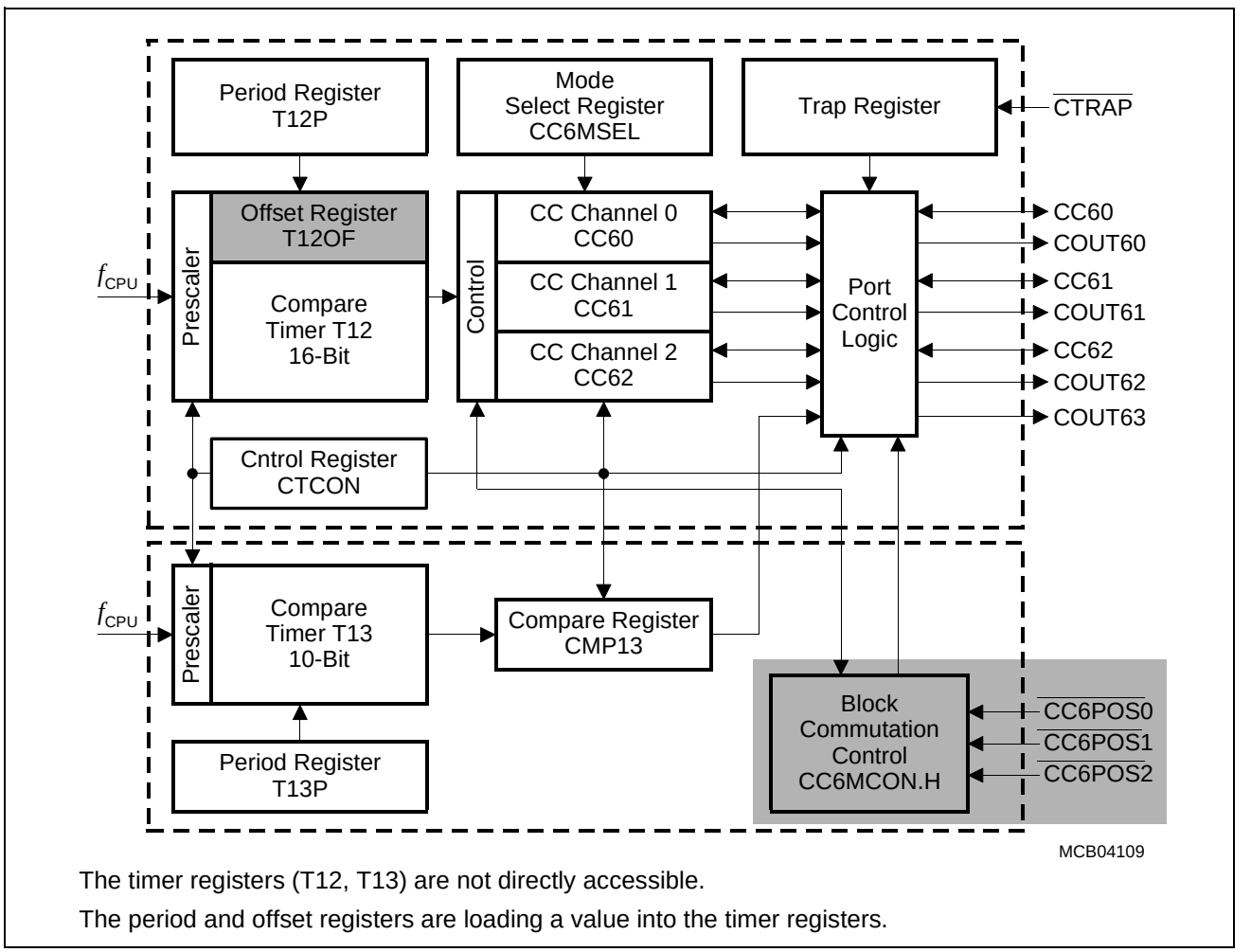
1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

2) The interrupt nodes assigned to ASC1 are only available in derivatives including the ASC1. Otherwise, they are unassigned nodes.

## 3.7 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.




The timer registers (T12, T13) are not directly accessible.

The period and offset registers are loading a value into the timer registers.

**Figure 6 CAPCOM6 Block Diagram**

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

## 3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer over-flow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

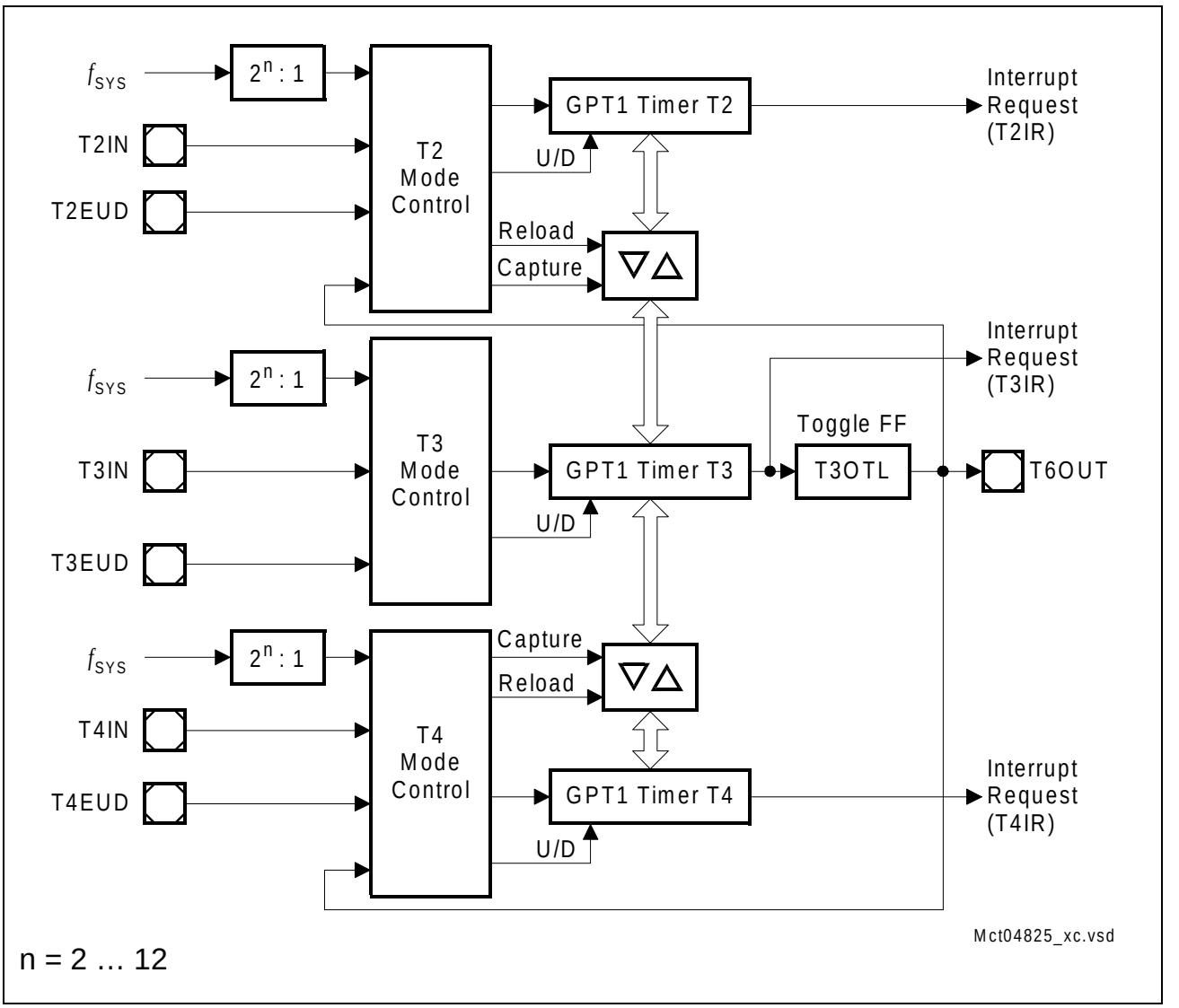



**Figure 7 Block Diagram of GPT1**

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM1/2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared

after the capture procedure. This allows the XC164N to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

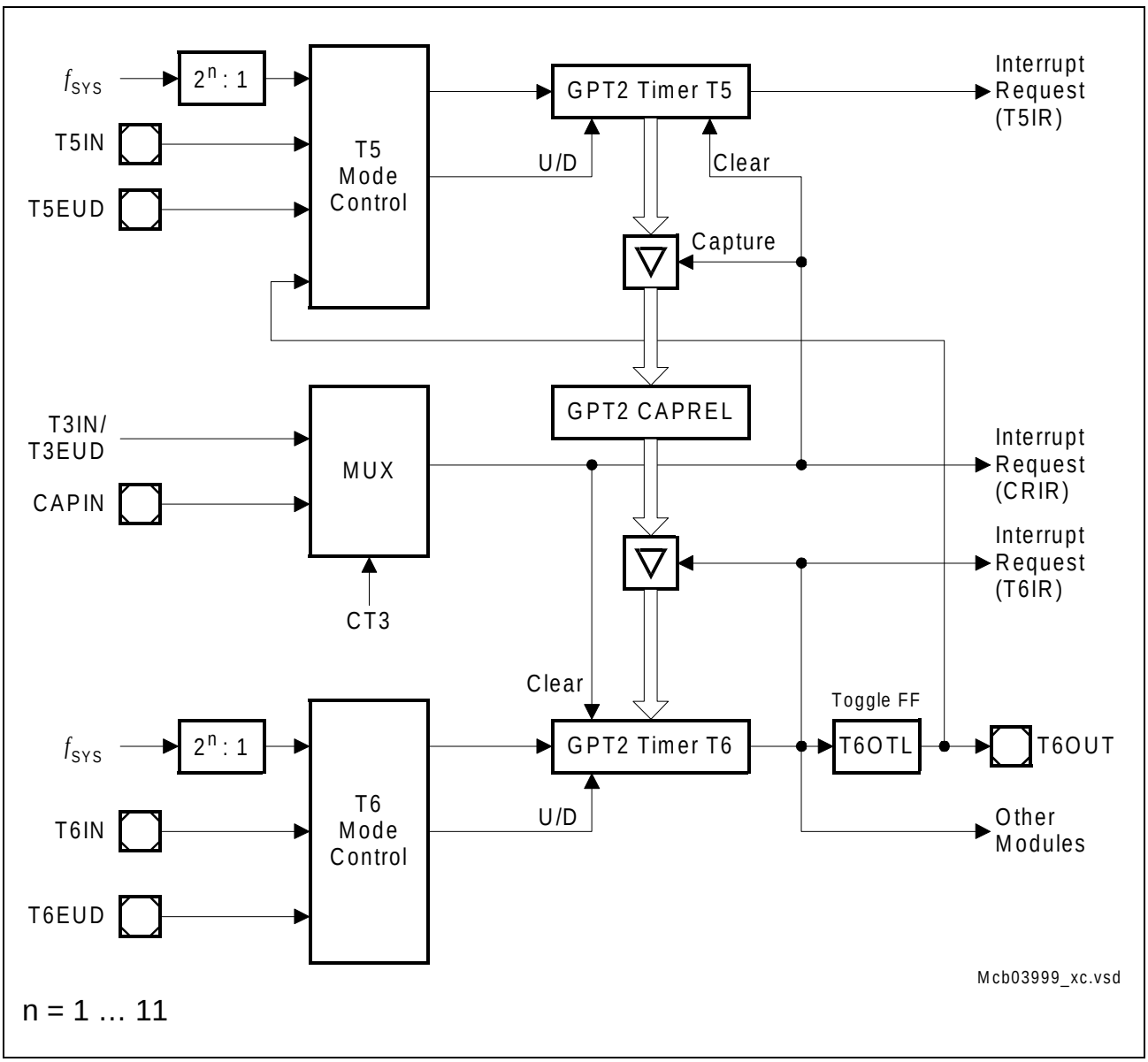



**Figure 8 Block Diagram of GPT2**

## 3.11 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

**Summary of Features**

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

## 3.12 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled until the EINIT instruction has been executed (compatible mode), or it can be disabled and enabled at any time by executing instructions DISWDT and ENWDT (enhanced mode). Thus, the chip’s start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and

generates an internal hardware reset and pulls the RSTOUT pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded and the low byte is cleared. Thus, time intervals between 13 µs and 419 ms can be monitored (@ 40 MHz).
The default Watchdog Timer interval after reset is 3.28 ms (@ 40 MHz).

## 3.13 Clock Generation

The Clock Generation Unit uses a programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC164N with high flexibility. The master clock $f_{MC}$ is the reference clock signal and is output to the external system. The CPU clock $f_{CPU}$ and the system clock $f_{SYS}$ are derived from the master clock either directly (1:1) or via a 2:1 prescaler ($f_{SYS} = f_{CPU} = f_{MC} / 2$). See also **Section 5.1**.

The on-chip oscillator can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

If the bypass mode is used (direct drive or prescaler) the PLL can deliver an independent clock to monitor the clock signal generated by the on-chip oscillator. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the Oscillator Watchdog (OWD) activates the PLL Unlock / OWD interrupt node and supplies the CPU with an emergency clock, the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

**The oscillator watchdog can be disabled** by switching the PLL off. This reduces power consumption, but also no interrupt request will be generated in case of a missing oscillator clock.

*Note: At the end of an external reset (EA = '0') the oscillator watchdog may be disabled via hardware by (externally) pulling the RD line low upon a reset, similar to the standard reset configuration.*

## 3.14 Parallel Ports

The XC164N provides up to 79 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of some I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs (except for pin RSTOUT).

# 4 Electrical Parameters

## 4.1 Absolute Maximum Ratings

**Table 9 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Storage temperature | $T_{ST}$ | -65 | 150 | °C | – |
| Junction temperature | $T_J$ | -40 | 150 | °C | under bias |
| Voltage on $V_{DDI}$ pins with respect to ground ($V_{SS}$) | $V_{DDI}$ | -0.5 | 3.25 | V | – |
| Voltage on $V_{DDP}$ pins with respect to ground ($V_{SS}$) | $V_{DDP}$ | -0.5 | 6.2 | V | – |
| Voltage on any pin with respect to ground ($V_{SS}$) | $V_{IN}$ | -0.5 | $V_{DDP}$ + 0.5 | V | – |
| Input current on any pin during overload condition | – | -10 | 10 | mA | – |
| Absolute sum of all input currents during overload condition | – | – | \|100\| | mA | – |

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.*

## 4.2 Package Properties

**Table 10 Package Parameters** (P-TQFP-100-16)

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Power dissipation | $P_{DISS}$ | – | 0.8 | W | – |
| Thermal Resistance | $R_{THA}$ | – | 29 | K/W | Chip-Ambient |

## 4.3 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC164N. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 11 Operating Condition Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Digital supply voltage for the core | $V_{DDI}$ | 2.35 | 2.7 | V | Active mode, $f_{CPU} = f_{CPUmax}$ 1) |
| Digital supply voltage for IO pads | $V_{DDP}$ | 4.4 | 5.5 | V | Active mode 2) 3) |
| Supply Voltage Difference | $\Delta V_{DD}$ | -0.5 | – | V | $V_{DDP}$ - $V_{DDI}$ 4) |
| Digital ground voltage | $V_{SS}$ | 0 | | V | Reference voltage |
| Overload current | $I_{OV}$ | -5 | 5 | mA | Per IO pin 5)6) |
| | | -2 | 5 | mA | Per analog input pin 5)6) |
| Overload current coupling factor for analog inputs 7) | $K_{OVA}$ | – | $1.0 \times 10^{-4}$ | – | $I_{OV} > 0$ |
| | | – | $1.5 \times 10^{-3}$ | – | $I_{OV} < 0$ |
| Overload current coupling factor for digital I/O pins 7) | $K_{OVD}$ | – | $5.0 \times 10^{-3}$ | – | $I_{OV} > 0$ |
| | | – | $1.0 \times 10^{-2}$ | – | $I_{OV} < 0$ |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ | – | 50 | mA | 6) |
| External Load Capacitance | $C_L$ | – | 50 | pF | Pin drivers in **default** mode 8) |
| Ambient temperature | $T_A$ | 0 | 70 | °C | SAB-XC164N … |
| | | -40 | 85 | °C | SAF-XC164N … |
| | | -40 | 125 | °C | SAK-XC164N … |

1) $f_{CPUmax}$ = 40 MHz for devices marked …40F, $f_{CPUmax}$ = 20 MHz for devices marked …20F.

2) External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating level.

3) The specified voltage range is allowed for operation. The range limits may be reached under extreme operating conditions. However, specified parameters, such as leakage currents, refer to the standard operating voltage range of $V_{DDP}$ = 4.75 V to 5.25 V.

4) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

5) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{DDP} + 0.5$ V ($I_{OV} > 0$) or $V_{OV} < V_{SS} - 0.5$ V ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits.
   Proper operation is not guaranteed if overload conditions occur on functional pins such as XTAL1, $\overline{RD}$, $\overline{WR}$, etc.
6) Not subject to production test - verified by design/characterization.
7) An overload current ($I_{OV}$) through a pin injects a certain error current ($I_{INJ}$) into the adjacent pins. This error current adds to the respective pin's leakage current ($I_{OZ}$). The amount of error current depends on the overload current and is defined by the overload coupling factor $K_{OV}$. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
   The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.
8) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability ($C_L$).

## 4.4 Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC164N and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

**CC** (**C**ontroller **C**haracteristics):
The logic of the XC164N will provide signals with the respective characteristics.

**SR** (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the XC164N.

For a period of $N \times$ TCM the accumulated PLL jitter is defined by the deviation $D_N$:

$D_N$ [ns] = $\pm(1.5 + 6.32 \times N / f_{MC})$; $f_{MC}$ in [MHz], $N$ = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for $K \times N < 95$. For longer periods the $K \times N = 95$ value can be used. This steady value can be approximated by: $D_{Nmax}$ [ns] = $\pm(1.5 + 600 / (K \times f_{MC}))$.

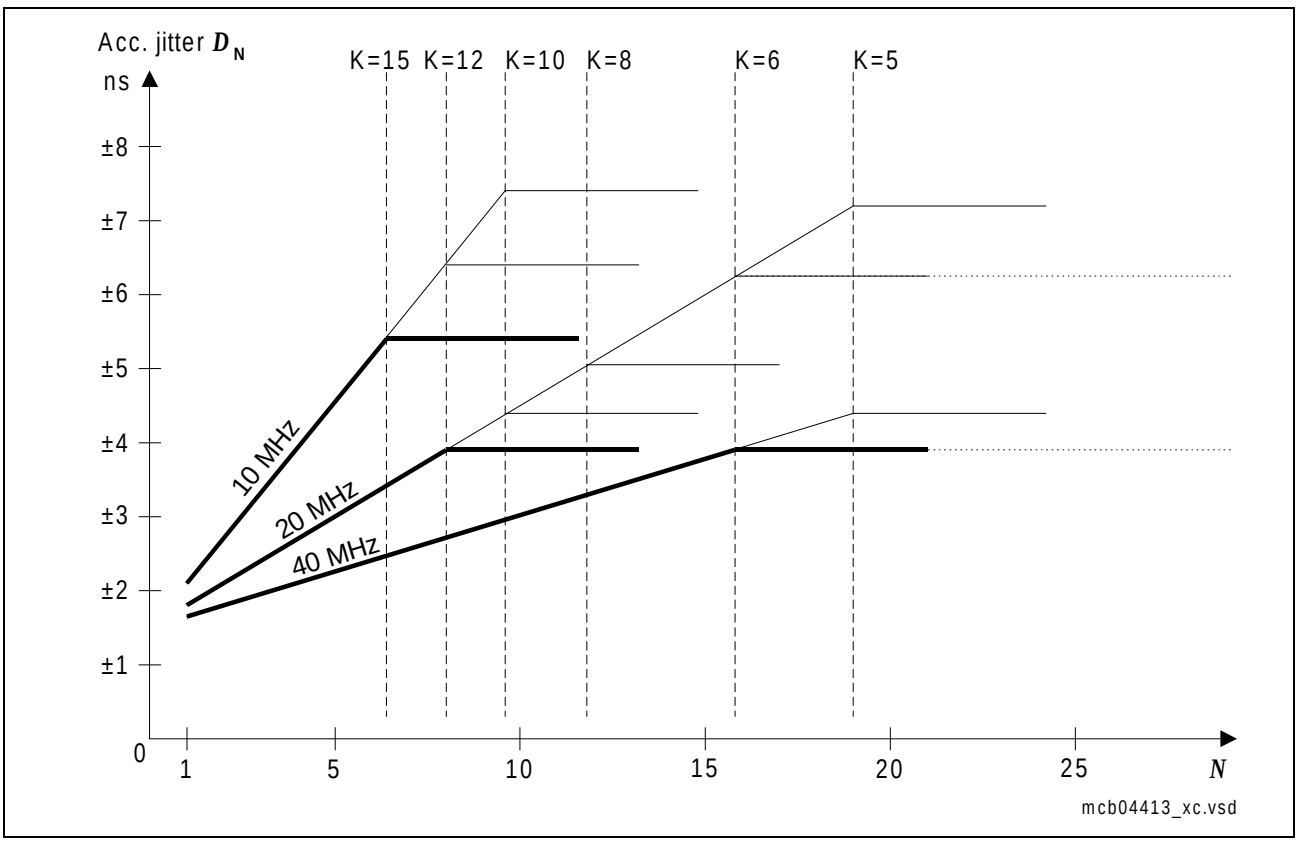



**Figure 14 Approximated Accumulated PLL Jitter**

*Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.*

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

**Table 13 VCO Bands for PLL Operation[1)]**

| PLLCON.PLLVB | VCO Frequency Range | Base Frequency Range |
|---|---|---|
| 00 | 100 … 150 MHz | 20 … 80 MHz |
| 01 | 150 … 200 MHz | 40 … 130 MHz |
| 10 | 200 … 250 MHz | 60 … 180 MHz |
| 11 | Reserved | |

1) Not subject to production test - verified by design/characterization.

## 5.2 External Clock Drive XTAL1

**Table 14 External Clock Drive Characteristics**
(Operating Conditions apply)

| Parameter | Symbol | | Limit Values | | Unit |
|---|---|---|---|---|---|
| | | | min. | max. | |
| Oscillator period | $t_{OSC}$ | SR | 20 | 250[1] | ns |
| High time[2] | $t_1$ | SR | 6 | – | ns |
| Low time[2] | $t_2$ | SR | 6 | – | ns |
| Rise time[2] | $t_3$ | SR | – | 8 | ns |
| Fall time[2] | $t_4$ | SR | – | 8 | ns |

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels $V_{ILC}$ and $V_{IHC}$.

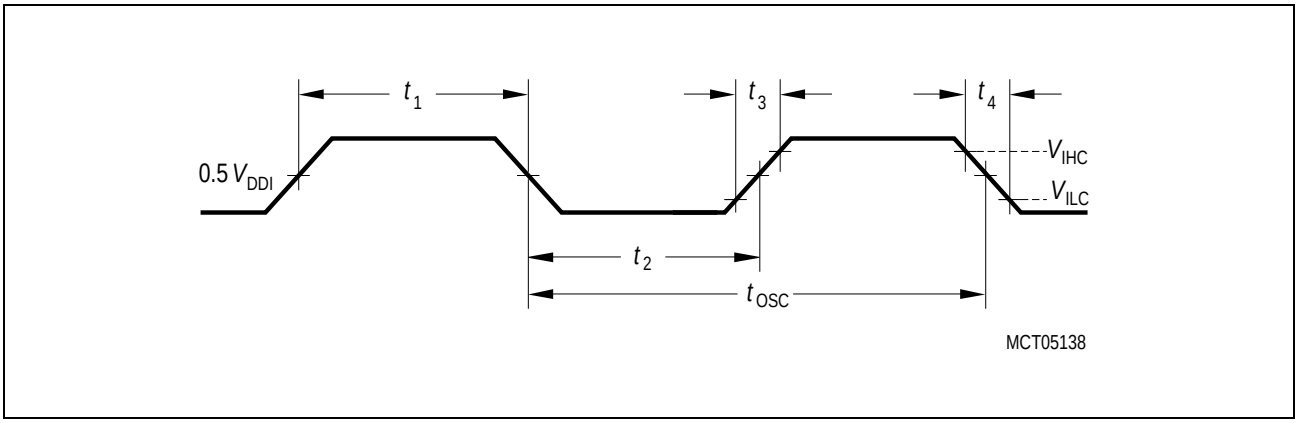



**Figure 15 External Clock Drive XTAL1**

*Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.*
*It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.*
*When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).*

## 5.3 Testing Waveforms

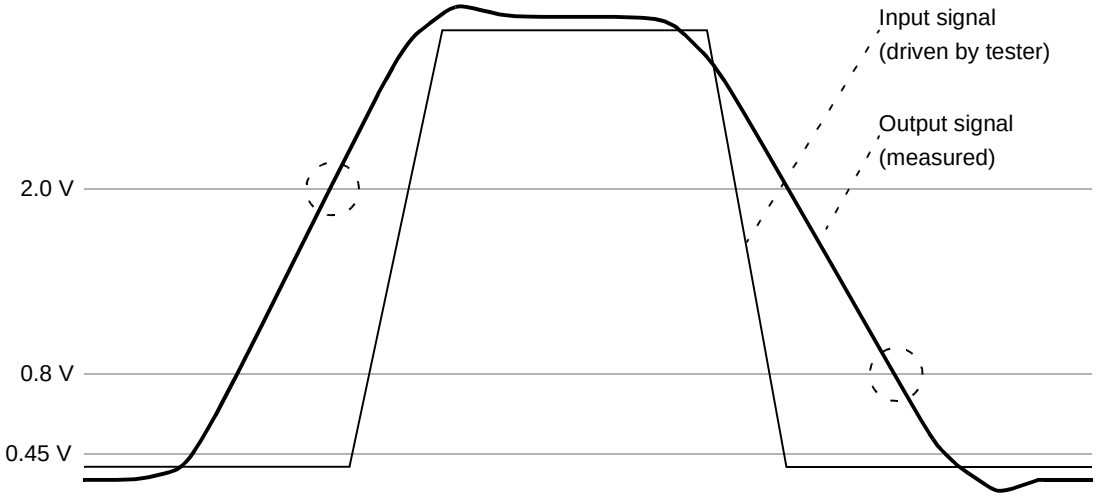
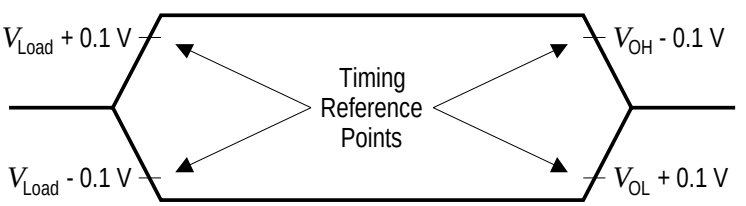



**Figure 16 Input Output Waveforms**




For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded $V_{OH}$ / $V_{OL}$ level occurs ($I_{OH}$ / $I_{OL}$ = 20 mA).

MCA00763

**Figure 17 Float Waveforms**

w w w . i n f i n e o n . c o m

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