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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	EBI/EMI, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	79
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	PG-TQFP-100-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc164n-8f40f-bb

Revision History:	**2005-01**	V1.0
Previous Version:	None	

Page	Subjects (major changes since last revision)

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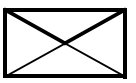

1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with up to 65 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 2 Kbytes On-Chip Data SRAM (DSRAM)
  - 2 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - up to 128 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - Two 16-Channel General Purpose Capture/Compare Units (12 Input/Output Pins)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip Real Time Clock
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Four Programmable Chip-Select Signals
- Up to 79 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader

Table 1 XC164N Derivative Synopsis

Derivative[1)]	Program Memory	On-Chip RAM	Inter-faces	Clock
SAF-XC164N-16F40F	128 Kbytes Flash	2Kbytes DPRAM, 2Kbytes DSRAM, 2Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1	40 MHz
SAF-XC164N-16F20F	128 Kbytes Flash	2Kbytes DPRAM, 2Kbytes DSRAM, 2Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1	20 MHz
SAF-XC164N-8F40F	64 Kbytes Flash	2Kbytes DPRAM, 2Kbytes DSRAM, 2Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1	40 MHz
SAF-XC164N-8F20F	64 Kbytes Flash	2Kbytes DPRAM, 2Kbytes DSRAM, 2Kbytes PSRAM	ASC0, ASC1, SSC0, SSC1	20 MHz

1) This Data Sheet is valid for devices starting with and including design step BA.

2.2 Pin Configuration and Definition

The pins of the XC164N are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) marks pins to be used as alternate external interrupt inputs.

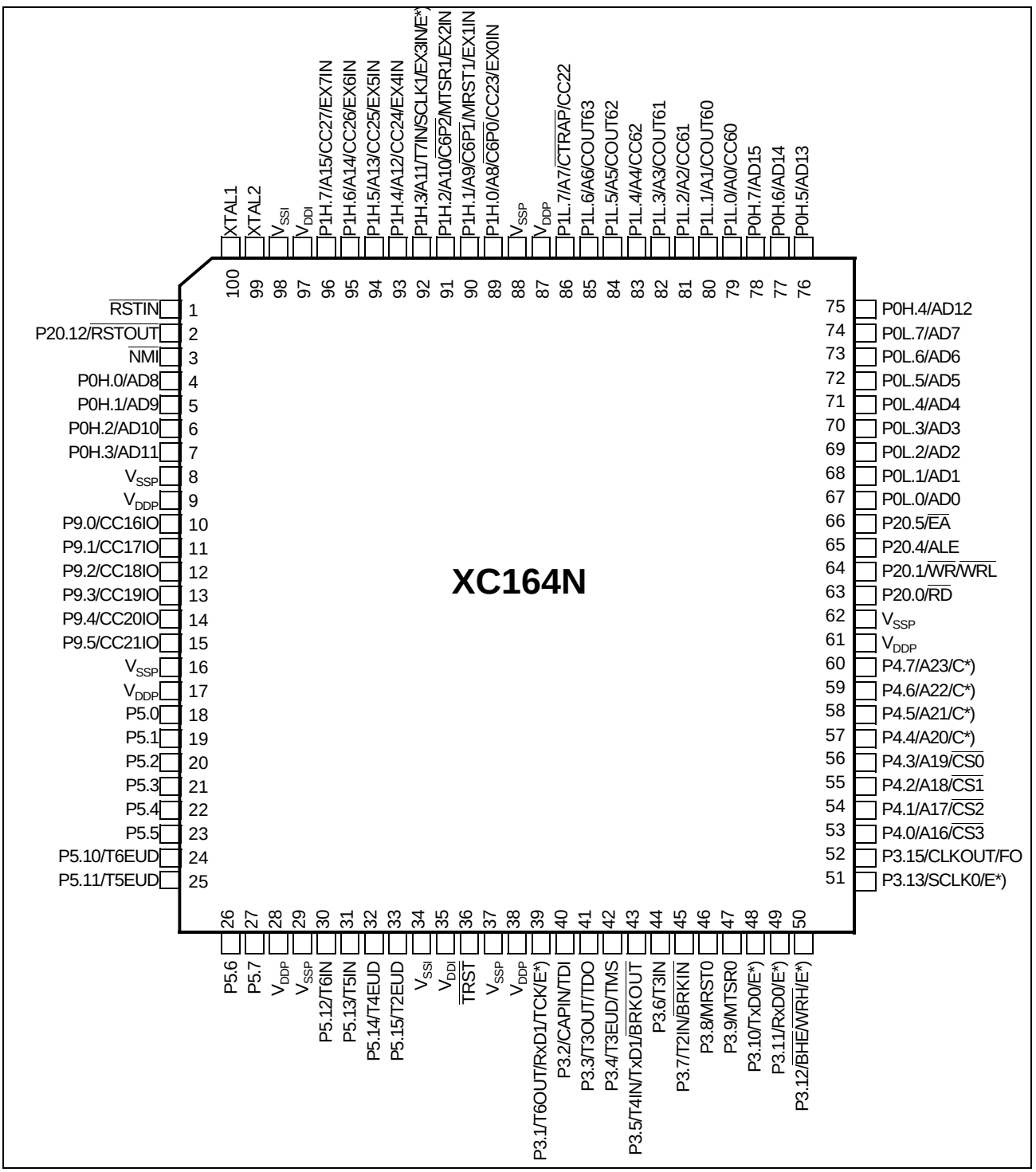

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT1 (cont'd)		IO	…continued…
P1H.0	89	I	$\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input,
		I	EX0IN Fast External Interrupt 0 Input (default pin),
		I/O	$\overline{\text{CC23IO}}$ CAPCOM2: CC23 Capture Inp./Compare Outp.
P1H.1	90	I	$\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input,
		I	EX1IN Fast External Interrupt 1 Input (default pin),
		I/O	$\overline{\text{MRST1}}$ SSC1 Master-Receive/Slave-Transmit In/Out.
P1H.2	91	I	$\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input,
		I	EX2IN Fast External Interrupt 2 Input (default pin),
		I/O	MTSR1 SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	92	I	T7IN CAPCOM2: Timer T7 Count Input,
		I/O	SCLK1 SSC1 Master Clock Output / Slave Clock Input,
		I	EX3IN Fast External Interrupt 3 Input (default pin),
		I	EX0IN Fast External Interrupt 0 Input (alternate pin A)
P1H.4	93	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.,
		I	EX4IN Fast External Interrupt 4 Input (default pin)
P1H.5	94	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.,
		I	EX5IN Fast External Interrupt 5 Input (default pin)
P1H.6	95	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.,
		I	EX6IN Fast External Interrupt 6 Input (default pin)
P1H.7	96	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.,
		I	EX7IN Fast External Interrupt 7 Input (default pin)
$\overline{\text{XTAL2}}$	99	O	XTAL2: Output of the oscillator amplifier circuit
XTAL1	100	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
res	28	-	pin is reserved and connected to V_{DDP}
res	29	-	pin is reserved and connected to V_{SSP}
V_{DDI}	35, 97	-	Digital Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
V_{DDP}	9, 17, 38, 61, 87	-	Digital Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**
V_{SSI}	34, 98	-	**Digital Ground.** Connect decoupling capacitors to adjacent V_{DD}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.
V_{SSP}	8, 16, 37, 62, 88	-	

3.1 Memory Subsystem and Organization

The memory space of the XC164N is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXbus. The system bus allows concurrent two-way communication for maximum transfer performance.

128 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and one 64-Kbyte sectors. Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
Programming typically takes 2 ms per 128-byte block (5 ms max.), erasing a sector typically takes 200 ms (500 ms max.).

2 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

2 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data.The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7)

1) Each two 8-Kbyte sectors are combined for write-protection purposes.

background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 wordwide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC164N instruction set which includes the following instruction classes:

– Standard Arithmetic Instructions
– DSP-Oriented Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Table 4 XC164N Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CCU6_IC	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
Unassigned node	---	xx'0150$_H$	54$_H$ / 84$_D$
Unassigned node	---	xx'0154$_H$	55$_H$ / 85$_D$
Unassigned node	---	xx'0158$_H$	56$_H$ / 86$_D$
Unassigned node	---	xx'015C$_H$	57$_H$ / 87$_D$
Unassigned node	---	xx'0164$_H$	59$_H$ / 89$_D$
Unassigned node	---	xx'0168$_H$	5A$_H$ / 90$_D$
Unassigned node	---	xx'016C$_H$	5B$_H$ / 91$_D$
Unassigned node	---	xx'0170$_H$	5C$_H$ / 92$_D$
Unassigned node	---	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	---	xx'0100$_H$	40$_H$ / 64$_D$
Unassigned node	---	xx'0104$_H$	41$_H$ / 65$_D$
Unassigned node	---	xx'012C$_H$	4B$_H$ / 75$_D$
Unassigned node	---	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	---	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

2) The interrupt nodes assigned to ASC1 are only available in derivatives including the ASC1. Otherwise, they are unassigned nodes.

3.6 Capture/Compare Units (CAPCOM1/2)

The CAPCOM units support generation and control of timing sequences on up to 32 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for each capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Both of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare function.
12 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM1/2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

3.9 Real Time Clock

The Real Time Clock (RTC) module of the XC164N is directly clocked via a separate clock driver with the prescaled on-chip oscillator frequency (f_{RTC} = f_{OSC} / 32). It is therefore independent from the selected clock generation mode of the XC164N.

The RTC basically consists of a chain of divider blocks:

- a selectable 8:1 divider (on - off)
- the reloadable 16-bit timer T14
- the 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

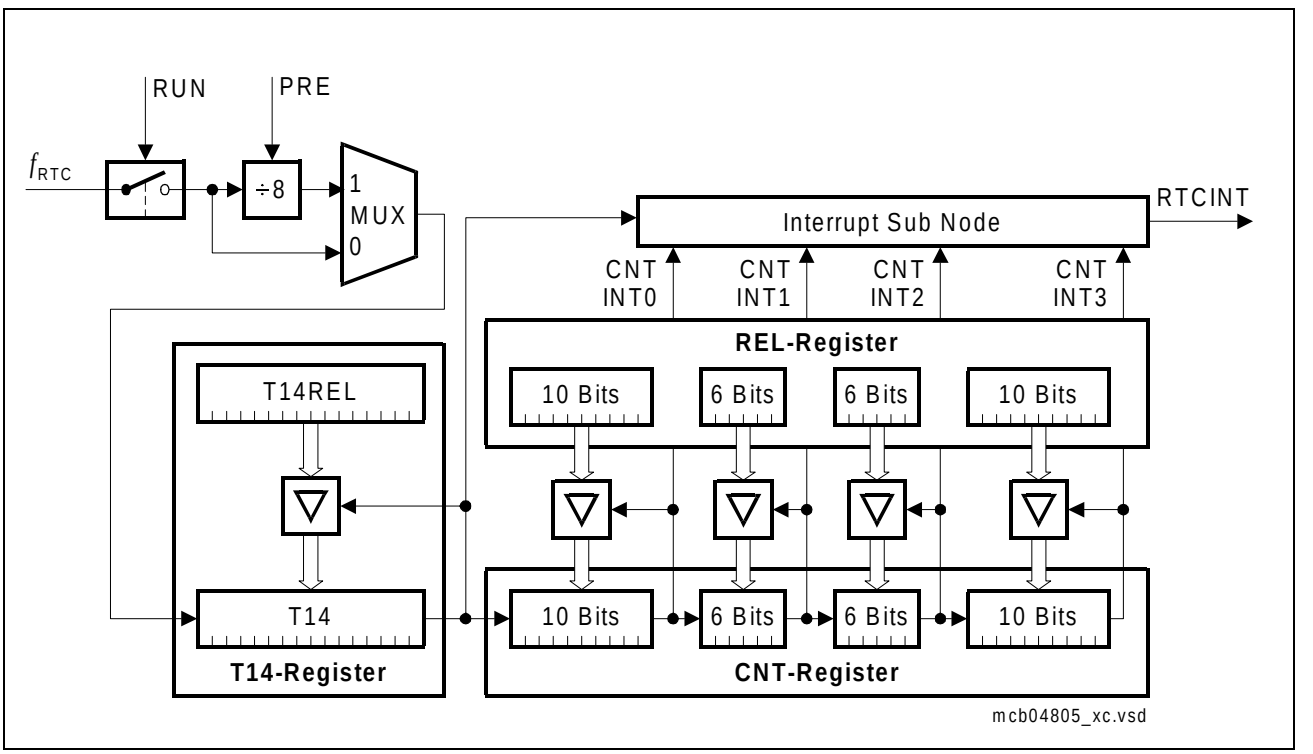

Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are not affected by a reset in order to maintain the correct system time even when intermediate resets are executed.

The RTC module can be used for different purposes:

- System clock to determine the current time and date,
  optionally during idle mode, sleep mode, and power down mode
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources, e.g. to wake up regularly from idle mode.
- 48-bit timer for long term measurements (maximum timespan is >100 years).
- Alarm interrupt for wake-up on a defined time

3.11 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

3.12 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled until the EINIT instruction has been executed (compatible mode), or it can be disabled and enabled at any time by executing instructions DISWDT and ENWDT (enhanced mode). Thus, the chip’s start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and

The edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected via registers POCONx.

The input threshold of some ports is selectable (TTL or CMOS like), where the special CMOS like input threshold reduces noise sensitivity due to the input hysteresis. The input threshold may be selected individually for each byte of the respective ports.

All port lines have programmable alternate input or output functions associated with them. All port lines that are not used for these alternate functions may be used as general purpose IO lines.

3.15 Power Management

The XC164N provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC164N into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC164N's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittend operation of the XC164N by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittend sleep phases greatly reduce the average power consumption of the system.

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH / POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Enter Power Down Mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	Signify End-of-Initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4
NOP	Null operation	2
CoMUL / CoMAC	Multiply (and accumulate)	4
CoADD / CoSUB	Add / Subtract	4
Co(A)SHR/CoSHL	(Arithmetic) Shift right / Shift left	4
CoLOAD/STORE	Load accumulator / Store MAC register	4
CoCMP/MAX/MIN	Compare (maximum/minimum)	4
CoABS / CoRND	Absolute value / Round accumulator	4
CoMOV/NEG/NOP	Data move / Negate accumulator / Null operation	4

5 Timing Parameters

5.1 Definition of Internal Timing

The internal operation of the XC164N is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC164N.

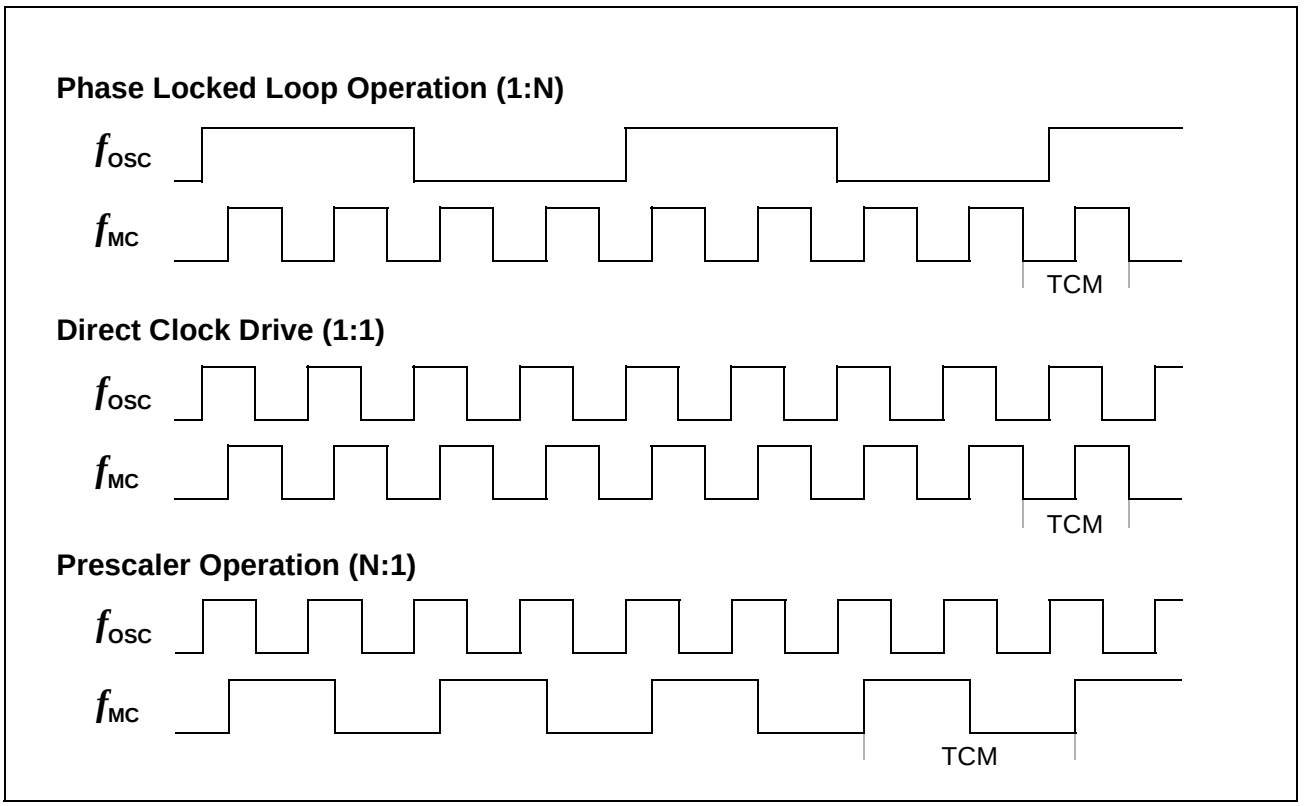

Figure 13 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 13** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU}.

For a period of $N \times$ TCM the accumulated PLL jitter is defined by the deviation D_N:

D_N [ns] = $\pm(1.5 + 6.32 \times N / f_{MC})$; f_{MC} in [MHz], N = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: $D_3 = \pm(1.5 + 6.32 \times 3 / 20) = 2.448$ ns.

This formula is applicable for $K \times N < 95$. For longer periods the $K \times N = 95$ value can be used. This steady value can be approximated by: D_{Nmax} [ns] = $\pm(1.5 + 600 / (K \times f_{MC}))$.

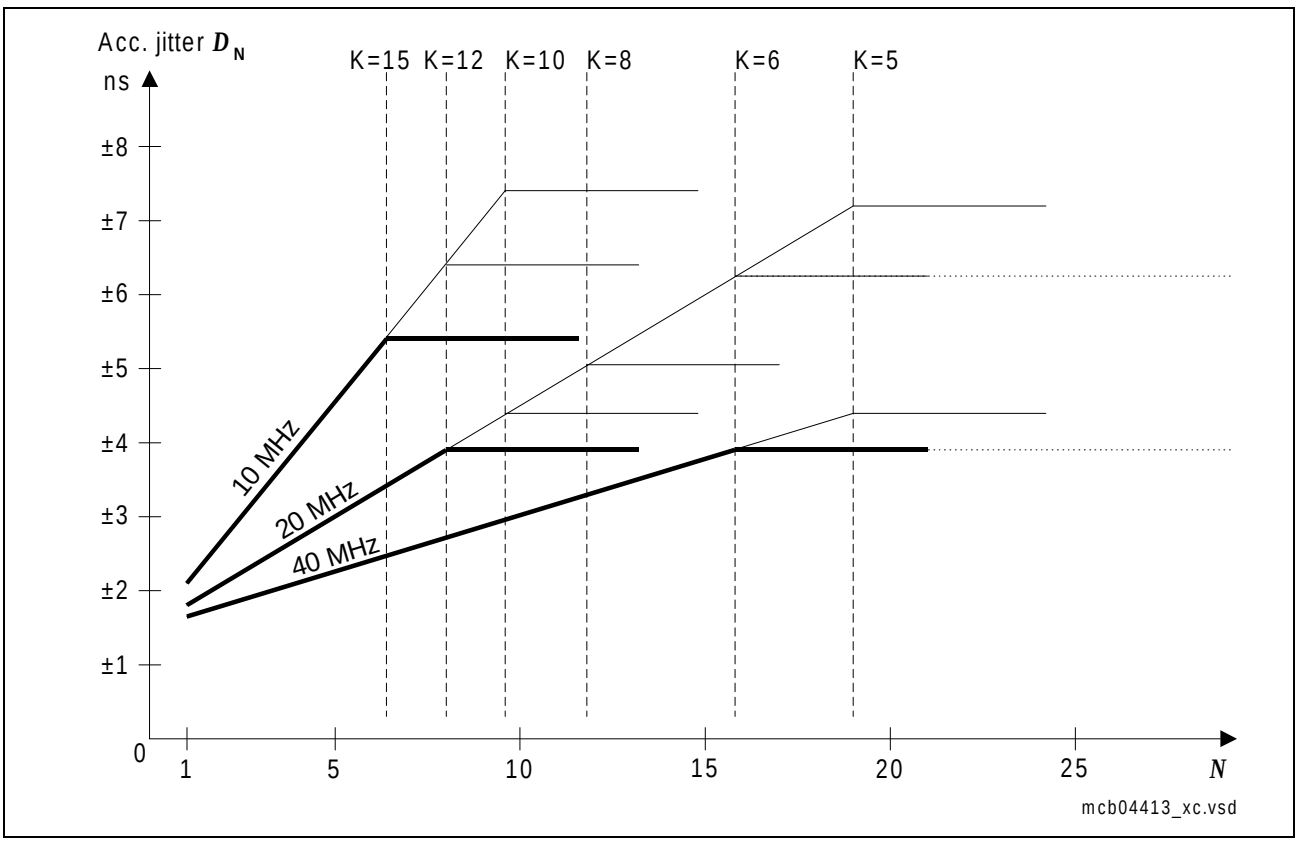

Figure 14 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 13 VCO Bands for PLL Operation[1)]

PLLCON.PLLVB	VCO Frequency Range	Base Frequency Range
00	100 … 150 MHz	20 … 80 MHz
01	150 … 200 MHz	40 … 130 MHz
10	200 … 250 MHz	60 … 180 MHz
11	Reserved	

1) Not subject to production test - verified by design/characterization.

Variable Memory Cycles

External bus cycles of the XC164N are executed in five subsequent cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

This table provides a summary of the phases and the respective choices for their duration. The specification of the external timing depends on the period of the CPU clock, which is called “TCP” and is used in **Table 16**

Table 16 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCP) can be extended by 0 … 3 TCP if the address window is changed	tp_{AB}	1 … 2 (5)	TCP
Command delay phase	tp_{C}	0 … 3	TCP
Write Data setup / MUX Tristate phase	tp_{D}	0 … 1	TCP
Access phase	tp_{E}	1 … 32	TCP
Address / Write Data hold phase	tp_{F}	0 … 3	TCP

Note: The bandwidth of a parameter (minimum and maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

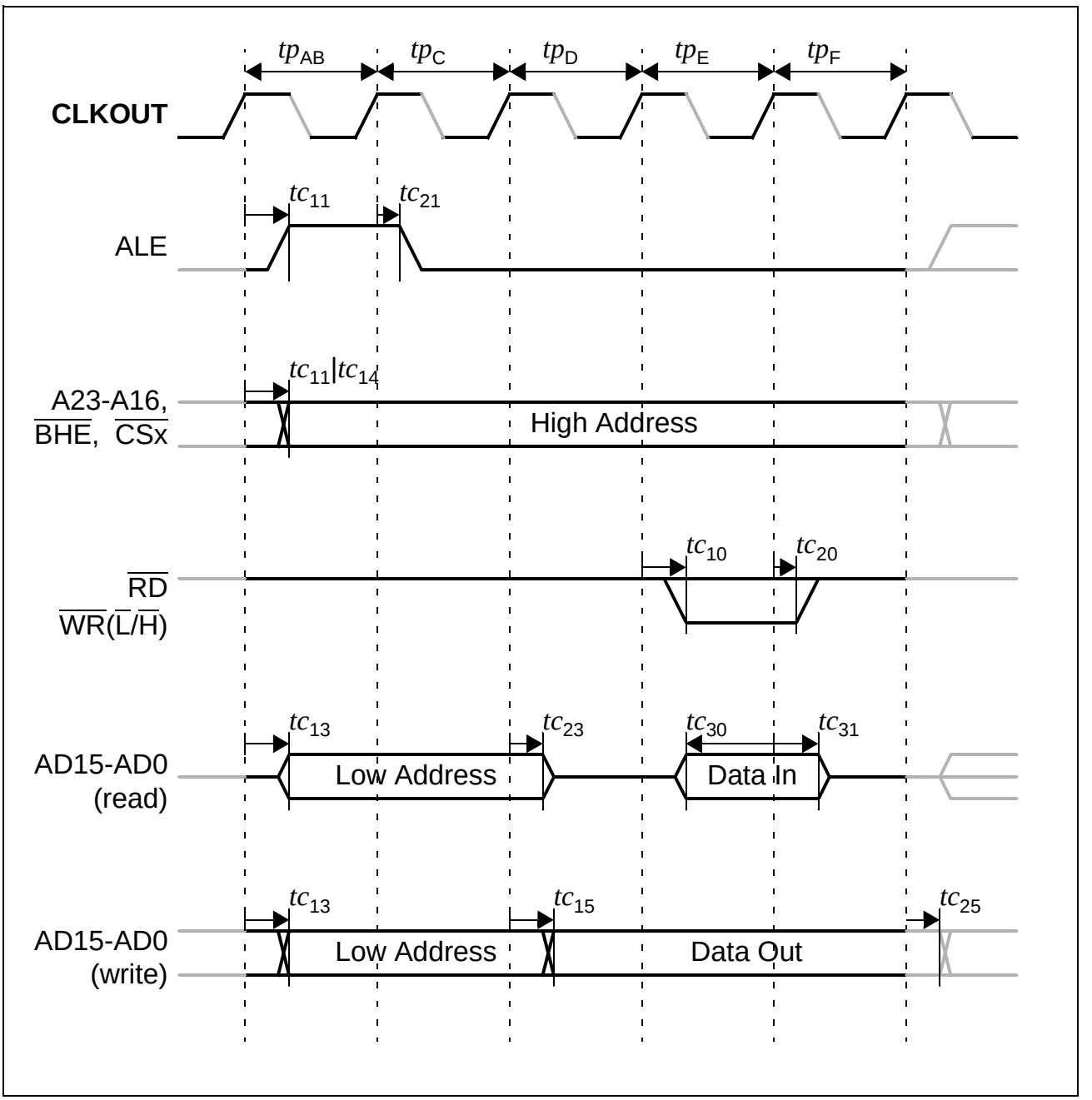

Figure 19 Multiplexed Bus Cycle