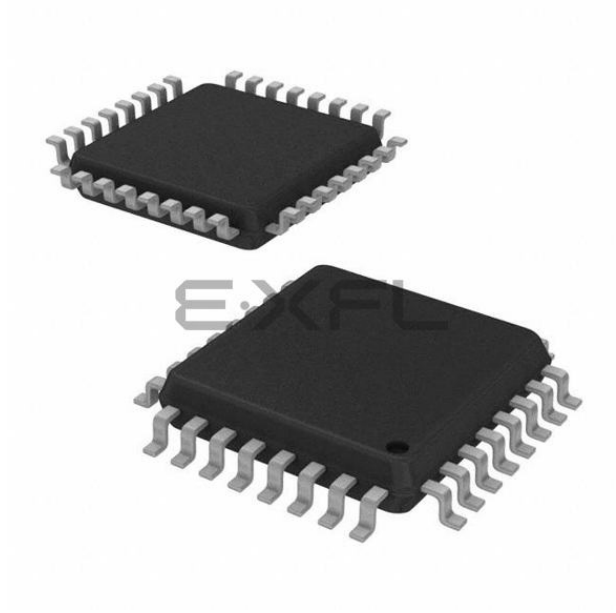

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800E |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8023vlc |

# Part 1 Overview

## 1.1 56F8033/56F8023 Features

### 1.1.1 Digital Signal Controller Core

- Efficient 16-bit 56800E family Digital Signal Controller (DSC) engine with dual Harvard architecture
- As many as 32 Million Instructions Per Second (MIPS) at 32MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, processor speed-independent, real-time debugging

### 1.1.2 Difference Between Devices

Table 1-1 outlines the key differences between the 56F8033 and 56F8023 devices.

**Table 1-1 Device Differences**

| On-Chip Memory | 56F8033 | 56F8023 |
|---|---|---|
| Program Flash (PFLASH) | 64KB | 32KB |
| Unified RAM (RAM) | 8KB | 4KB |

### 1.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal Flash
- On-chip memory
  - 64KB of Program Flash (56F80233 device)
    32KB of Program Flash (56F8023 device)
  - 8KB of Unified Data/Program RAM (56F8033 device)
    4KB of Unified Data/Program RAM (56F8023 device)
- EEPROM emulation capability using Flash

In **Table 2-2**, peripheral pins in bold identify reset state.

**Table 2-2 56F8033/56F8023 Pins**

| | | | Peripherals: | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Signal Name** | **GPIO** | **I2C** | **QSCI** | **QSPI** | **ADC** | **PWM** | **Quad Timer** | **Comp** | **Power & Ground** | **JTAG** | **Misc.** |
| 1 | **GPIOB6** | GPIOB6, RXD0, SDA, CLKIN | **B6** | SDA | RXD0 | | | | | | | | CLKIN |
| 2 | **GPIOB1** | GPIOB1, $\overline{SS0}$, SDA | **B1** | SDA | | $\overline{SS0}$ | | | | | | | |
| 3 | **GPIOB7** | GPIOB7, TXD0, SCL | **B7** | SCL | TXD0 | | | | | | | | |
| 4 | **GPIOB5** | GPIOB5, TA1, FAULT3, CLKIN | **B5** | | | | | FAULT3 | TA1 | | | | CLKIN |
| 5 | **GPIOC4** | GPIOC4, ANB0 & CMPBI3 | **C4** | | | | ANB0 | | | CMPBI3 | | | |
| 6 | **GPIOC5** | GPIOC5, ANB1 | **C5** | | | | ANB1 | | | | | | |
| 7 | **GPIOC6** | GPIOC6, ANB2, $V_{REFHB}$ | **C6** | | | | ANB2 $V_{REFHB}$ | | | | | | |
| 8 | **VDDA** | $V_{DDA}$ | | | | | | | | | $V_{DDA}$ | | |
| 9 | **VSSA** | $V_{SSA}$ | | | | | | | | | $V_{SSA}$ | | |
| 10 | **GPIOC2** | GPIOC2, ANA2, $V_{REFHA}$ | **C2** | | | | ANA2 $V_{REFHA}$ | | | | | | |
| 11 | **GPIOC1** | GPIOC1, ANA1 | **C1** | | | | ANA1 | | | | | | |
| 12 | **GPIOC0** | GPIOC0, ANA0 & CMPAI3 | **C0** | | | | ANA0 | | | CMPAI3 | | | |
| 13 | **VSS** | $V_{SS}$ | | | | | | | | | $V_{SS}$ | | |
| 14 | **TCK** | TCK, GPIOD2 | D2 | | | | | | | | | **TCK** | |
| 15 | **RESET** | $\overline{RESET}$, GPIOA7 | A7 | | | | | | | | | | **$\overline{RESET}$** |
| 16 | **GPIOB3** | GPIOB3, MOSI0, TA3, PSRC1 | **B3** | | | MOSI0 | | PSRC1 | TA3 | | | | |
| 17 | **GPIOB2** | GPIOB2, MISO0, TA2, PSRC0 | **B2** | | | MISO0 | | PSRC0 | TA2 | | | | |
| 18 | **GPIOA6** | GPIOA6, FAULT0, TA0 | **A6** | | | | | FAULT0 | TA0 | | | | |
| 19 | **GPIOB4** | GPIOB4, TA0, CLKO, PSRC2 | **B4** | | | | | PSRC2 | TA0 | | | | CLKO |
| 20 | **GPIOA5** | GPIOA5, PWM5, TA3, FAULT2 | **A5** | | | | | PWM5 FAULT2 | TA3 | | | | |
| 21 | **GPIOB0** | GPIOB0, SCLK0, SCL | **B0** | SCL | | SCLK0 | | | | | | | |
| 22 | **GPIOA4** | GPIOA4, PWM4, TA2, FAULT1 | **A4** | | | | | PWM4 FAULT1 | TA2 | | | | |
| 23 | **GPIOA2** | GPIOA2, PWM2 | **A2** | | | | | PWM2 | | | | | |
| 24 | **GPIOA3** | GPIOA3, PWM3 | **A3** | | | | | PWM3 | | | | | |
| 25 | **VCAP** | $V_{CAP}$ | | | | | | | | | **$V_{CAP}$** | | |
| 26 | **VDD** | $V_{DD}$ | | | | | | | | | **$V_{DD}$** | | |
| 27 | **VSS** | $V_{SS}$ | | | | | | | | | **$V_{SS}$** | | |
| 28 | **GPIOA1** | GPIOA1, PWM1 | **A1** | | | | | PWM1 | | | | | |

## Table 2-3 56F8033/56F8023 Signal and Package Information for the 32-Pin LQFP

| Signal Name | LQFP Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| **GPIOA1**<br><br>**(PWM1)** | 28 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM1** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA1. |
| **GPIOA2**<br><br>**(PWM2)** | 23 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM2** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA2. |
| **GPIOA3**<br><br>**(PWM3)** | 24 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM3** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA3. |
| **GPIOA4**<br><br>**(PWM4)**<br><br>**(TA2[1])**<br><br>**(FAULT1[2])** | 22 | Input/ Output<br><br>Output<br><br>Input/ Output<br><br>Input | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM4** — This is one of the six PWM output pins.<br><br>**TA2** — Timer A, Channel 2<br><br>**Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.<br><br>After reset, the default state is GPIOA4. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |

[1]The TA2 signal is also brought out on the GPIOB2-3 pin.
[2]The Fault1 signal is also brought out on the GPIOB4 pin.

**Return to Table 2-2**

## Table 2-3 56F8033/56F8023 Signal and Package Information for the 32-Pin LQFP

| Signal Name | LQFP Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| **GPIOB0** | 21 | Input/ Output | Input, internal pull-up enabled | **Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. |
| **(SCLK0)** | | Input/ Output | | **QSPI0 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. A Schmitt trigger input is used for noise immunity. |
| **(SCL[6])** | | Input/ Output | | **Serial Clock** — This pin serves as the $I^2C$ serial clock.<br><br>After reset, the default state is GPIOB0. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| [6]The SCL signal is also brought out on the GPIOB7 pin. | | | | |
| **GPIOB1** | 2 | Input/ Output | Input, internal pull-up enabled | **Port B GPIO** — This GPIO pin can be individually programmed as an input or output pin. |
| **($\overline{SS0}$)** | | Input/ Output | | **QSPI0 Slave Select** — $\overline{SS}$ is used in slave mode to indicate to the QSPI0 module that the current transfer is to be received. |
| **(SDA[7])** | | Input | | **Serial Data** — This pin serves as the $I^2C$ serial data line.<br><br>After reset, the default state is GPIOB1. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |
| [7]The SDA signal is also brought out on the GPIOB6 pin. | | | | |

**Return to Table 2-2**

## Table 4-12 Interrupt Control Registers Address Map (Continued) (ITCN_BASE = $00 F0E0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| ITCN_FIM0 | $8 | Fast Interrupt Match 0 Register |
| ITCN_FIVAL0 | $9 | Fast Interrupt Vector Address Low 0 Register |
| ITCN_FIVAH0 | $A | Fast Interrupt Vector Address High 0 Register |
| ITCN_FIM1 | $B | Fast Interrupt Match 1 Register |
| ITCN_FIVAL1 | $C | Fast Interrupt Vector Address Low 1 Register |
| ITCN_FIVAH1 | $D | Fast Interrupt Vector Address High 1 Register |
| ITCN_IRQP0 | $E | IRQ Pending Register 0 |
| ITCN_IRQP1 | $F | IRQ Pending Register 1 |
| ITCN_IRQP2 | $10 | IRQ Pending Register 2 |
| ITCN_IRQP3 | $11 | IRQ Pending Register 3 |
| | | Reserved |
| ITCN_ICTRL | $16 | Interrupt Control Register |
| | | Reserved |

## Table 4-13 SIM Registers Address Map (SIM_BASE = $00 F100)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| SIM_CTRL | $0 | Control Register |
| SIM_RSTAT | $1 | Reset Status Register |
| SIM_SWC0 | $2 | Software Control Register 0 |
| SIM_SWC1 | $3 | Software Control Register 1 |
| SIM_SWC2 | $4 | Software Control Register 2 |
| SIM_SWC3 | $5 | Software Control Register 3 |
| SIM_MSHID | $6 | Most Significant Half JTAG ID |
| SIM_LSHID | $7 | Least Significant Half JTAG ID |
| SIM_PWR | $8 | Power Control Register |
| | | Reserved |
| SIM_CLKOUT | $A | Clock Out Select Register |
| SIM_PCR | $B | Peripheral Clock Rate Register |
| SIM_PCE0 | $C | Peripheral Clock Enable Register 0 |
| SIM_PCE1 | $D | Peripheral Clock Enable Register 1 |
| SIM_SD0 | $E | Peripheral STOP Disable Register 0 |
| SIM_SD1 | $F | Peripheral STOP Disable Register 1 |
| SIM_IOSAHI | $10 | I/O Short Address Location High Register |
| SIM_IOSALO | $11 | I/O Short Address Location Low Register |
| SIM_PROT | $12 | Protection Register |
| SIM_GPSA0 | $13 | GPIO Peripheral Select Register 0 for GPIOA |

### Table 4-23 Digital-to-Analog Converter 0 Registers Address Map (DAC0_BASE = $00 F1C0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| DAC0_CTRL | $0 | Control Register |
| DAC0_DATA | $1 | Data Register |
| DAC0_STEP | $2 | Step Register |
| DAC0_MINVAL | $3 | Minimum Value Register |
| DAC0_MAXVAL | $4 | Maximum Value Register |

### Table 4-24 Comparator A Registers Address Map (CMPA_BASE = $00 F1E0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| CMPA_CTRL | $0 | Control Register |
| CMPA_STAT | $1 | Status Register |
| CMPA_FILT | $2 | Filter Register |

### Table 4-25 Comparator B Registers Address Map (CMPB_BASE = $00 F1F0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| CMPB_CTRL | $0 | Control Register |
| CMPB_STAT | $1 | Status Register |
| CMPB_FILT | $2 | Filter Register |

### Table 4-26 Queued Serial Communication Interface 0 Registers Address Map (QSCI0_BASE = $00 F200)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| QSCI0_RATE | $0 | Baud Rate Register |
| QSCI0_CTRL1 | $1 | Control Register 1 |
| QSCI0_CTRL2 | $2 | Control Register 2 |
| QSCI0_STAT | $3 | Status Register |
| QSCI0_DATA | $4 | Data Register |

## 5.4 Block Diagram

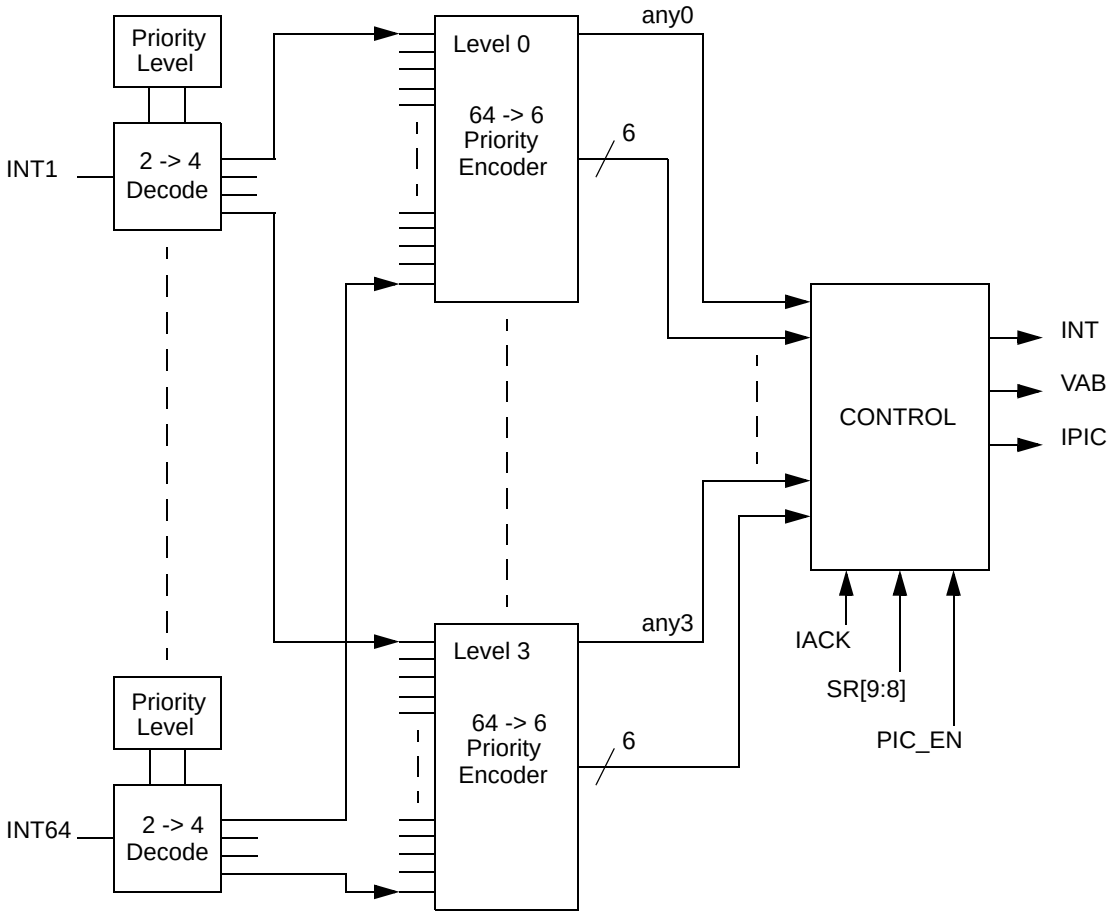



**Figure 5-1 Interrupt Controller Block Diagram**

## 5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode.

## 5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the

### 5.6.11.2 Fast Interrupt 0 Vector Address High (FIVAH0)—Bits 4–0

The upper five bits of the vector address used for Fast Interrupt 0. This register is combined with FIVAL0 to form the 21-bit vector address for Fast Interrupt 0 defined in the FIM0 register.

## 5.6.12 Fast Interrupt 1 Match Register (FIM1)

| Base + $B | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FAST INTERRUPT 1 | | | | | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-14 Fast Interrupt 1 Match Register (FIM1)**

### 5.6.12.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

### 5.6.12.2 Fast Interrupt 1 Vector Number (FAST INTERRUPT 1)—Bits 5–0

These values determine which IRQ will be Fast Interrupt 1. Fast Interrupts vector directly to a service routine based on values in the Fast Interrupt Vector Address registers without having to go to a jump table first. IRQs used as Fast Interrupts *must* be set to priority level 2. Unexpected results will occur if a Fast Interrupt vector is set to any other priority. A Fast Interrupt automatically becomes the highest priority level 2 interrupt, regardless of its location in the interrupt table prior to being declared as Fast Interrupt. Fast Interrupt 0 has priority over Fast Interrupt 1. To determine the vector number of each IRQ, refer to the vector table.

## 5.6.13 Fast Interrupt 1 Vector Address Low Register (FIVAL1)

| Base + $C | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | FAST INTERRUPT 1 VECTOR ADDRESS LOW | | | | | | | | | | | | | | | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-15 Fast Interrupt 1 Vector Address Low Register (FIVAL1)**

### 5.6.13.1 Fast Interrupt 1 Vector Address Low (FIVAL1)—Bits 15–0

The lower 16 bits of the vector address used for Fast Interrupt 1. This register is combined with FIVAH1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

## 5.6.14 Fast Interrupt 1 Vector Address High (FIVAH1)

| Base + $D | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FAST INTERRUPT 1 VECTOR ADDRESS HIGH | | | | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-16 Fast Interrupt 1 Vector Address High Register (FIVAH1)**

#### 6.3.11.2 Comparator A Clock Stop Disable (CMPA_SD)—Bit 14

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.3 Digital-to-Analog Converter 0 Clock Stop Disable (DAC1_SD)—Bit 13

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.4 Digital-to-Analog Converter 0 Clock Stop Disable (DAC0_SD)—Bit 12

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.5 Reserved—Bit 11

This bit field is reserved. It must be set to 0.

#### 6.3.11.6 Analog-to-Digital Converter Clock Stop Disable (ADC_SD)—Bit 10

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.7 Reserved—Bits 9–7

This bit field is reserved. Each bit must be set to 0.

#### 6.3.11.8 Inter-Integrated Circuit Clock Stop Disable (I2C_SD)—Bit 6

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.9 Reserved—Bit 5

This bit field is reserved. It must be set to 0.

#### 6.3.11.10 QSCI0 Clock Stop Disable (QSCI0_SD)—Bit 4

- 0 = The clock is disabled during Stop mode
- 1 = The clock is enabled during Stop mode if the clock to this peripheral is enabled in the SIM_PCE0 register

#### 6.3.11.11 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

#### 6.3.17.3 Configure GPIOB5 (GPS_B5)—Bits 12–11

This field selects the alternate function for GPIOB5.

- 00 = TA1 - Timer A1 (default)
- 01 = FAULT3 - PWM FAULT3 Input
- 10 = CLKIN - External Clock Input
- 11 = Reserved

#### 6.3.17.4 Configure GPIOB4 (GPS_B4)—Bits 10–8

This field selects the alternate function for GPIOB4.

- 000 = TA0 - Timer A0 (default)
- 001 = CLKO - Clock Output
- 010 = Reserved
- 011 = TB0 - Timer B0
- 100 = PSRC2 - PWM4 / PWM5 Pair External Source
- 11x = Reserved
- 1x1 = Reserved

#### 6.3.17.5 Configure GPIOB3 (GPS_B3)—Bits 7–6

This field selects the alternate function for GPIOB3.

- 00 = MOSI0 - QSPI0 Master Out/Slave In (default)
- 01 = TA3 - Timer A3
- 10 = PSRC1 - PWM2 / PWM3 Pair External Source
- 11 = Reserved

#### 6.3.17.6 Configure GPIOB2 (GPS_B2)—Bits 5–4

This field selects the alternate function for GPIOB2.

- 00 = MISO0 QSPI0 Master In/Slave Out (default)
- 01 = TA2 - Timer A2
- 10 = PSRC0 - PWM0 / PWM1 Pair External Source
- 11 = Reserved

#### 6.3.17.7 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

#### 6.3.17.8 Configure GPIOB1 (GPS_B1)—Bit 2

This field selects the alternate function for GPIOB1.

- 0 = $\overline{SS}$0 - QSPI0 Slave Select (default)
- 1 = SDA - I2C Serial Data

| Add. Offset | Register Acronym | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $0 | GPIOD_PUPEN | R | | | | | | | | | | | | | PU[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $1 | GPIOD_DATA | R | | | | | | | | | | | | | D[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $2 | GPIOD_DDIR | R | | | | | | | | | | | | | DD[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $3 | GPIOD_PEREN | R | | | | | | | | | | | | | PE[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| $4 | GPIOD_IASSRT | R | | | | | | | | | | | | | IA[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $5 | GPIOD_IEN | R | | | | | | | | | | | | | IEN[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $6 | GPIOD_IEPOL | R | | | | | | | | | | | | | IEPOL[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $7 | GPIOD_IPEND | R | | | | | | | | | | | | | IPR[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $8 | GPIOD_IEDGE | R | | | | | | | | | | | | | IES[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $9 | GPIOD_PPOUTM | R | | | | | | | | | | | | | OEN[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $A | GPIOD_RDATA | R | | | | | | | | | | | | | RAW DATA[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X | X | X | X | X |
| $B | GPIOD_DRIVE | R | | | | | | | | | | | | | DRIVE[15:0] | | | |
| | | W | | | | | | | | | | | | | | | | |
| | | RS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| R | 0 | Read as 0 |
| W | | Reserved |
| RS | | Reset |

**Figure 8-4 GPIOD Register Map Summary**

# Part 9 Joint Test Action Group (JTAG)

## 9.1 56F8033/56F8023 Information

Please contact your Freescale sales representative or authorized distributor for device/package-specific BSDL information.

The $\overline{\text{TRST}}$ pin is not available in this package. The pin is tied to $V_{DD}$ in the package.

The JTAG state machine is reset during POR and can also be reset via a soft reset by holding TMS high for five rising edges of TCK, as described in the **56F802X and 56F803X Peripheral Reference Manual**.

# Part 10 Specifications

## 10.1 General Characteristics

The 56F8033/56F8023 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V- and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels, combined with the ability to receive 5V levels without damage.

Absolute maximum ratings in **Table 10-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40ºC to 125ºC ambient temperature over the following supply ranges:
$V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6V$, $CL \leq 50pF$, $f_{OP} = 32MHz$

**CAUTION**

**This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.**

### Table 10-1 Absolute Maximum Ratings

($V_{SS}$ = 0V, $V_{SSA}$ = 0V)

| Characteristic | Symbol | Notes | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | | -0.3 | 4.0 | V |
| Analog Supply Voltage Range | $V_{DDA}$ | | - 0.3 | 4.0 | V |
| ADC High Voltage Reference | $V_{REFHx}$ | | - 0.3 | 4.0 | V |
| Voltage difference $V_{DD}$ to $V_{DDA}$ | $\Delta V_{DD}$ | | - 0.3 | 0.3 | V |
| Voltage difference $V_{SS}$ to $V_{SSA}$ | $\Delta V_{SS}$ | | - 0.3 | 0.3 | V |
| Digital Input Voltage Range | $V_{IN}$ | Pin Groups 1, 2 | - 0.3 | 6.0 | V |
| Oscillator Voltage Range | $V_{OSC}$ | Pin Group 4 | - 0.4 | 4.0 | V |
| Analog Input Voltage Range | $V_{INA}$ | Pin Group 3 | - 0.3 | 4.0 | V |
| Input clamp current, per pin ($V_{IN}$ < 0)[1] | $V_{IC}$ | | — | -20.0 | mA |
| Output clamp current, per pin ($V_O$ < 0)[1] | $V_{OC}$ | | — | -20.0 | mA |
| Output Voltage Range (Normal Push-Pull mode) | $V_{OUT}$ | Pin Group 1 | - 0.3 | 4.0 | V |
| Output Voltage Range (Open Drain mode) | $V_{OUTOD}$ | Pin Group 2 | - 0.3 | 6.0 | V |
| Ambient Temperature Industrial | $T_A$ | | - 40 | 105 | °C |
| Storage Temperature Range (Extended Industrial) | $T_{STG}$ | | - 55 | 150 | °C |

1. Continuous clamp current per pin is -2.0 mA

**Default Mode**

Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Pin Group 2: $\overline{\text{RESET}}$, GPIOA7

Pin Group 3: ADC and Comparator Analog Inputs

Pin Group 4: XTAL, EXTAL

## 10.1.1 ElectroStatic Discharge (ESD) Model

### Table 10-2 56F8033/56F8023 ESD Protection

| Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|
| ESD for Human Body Model (HBM) | 2000 | — | — | V |

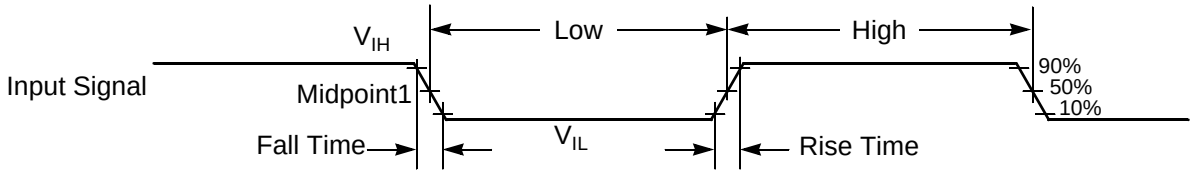
measured directly on the $V_{CAP}$ pin. The specifications for this regulator are shown in **Table 10-8**.

**Table 10-8. Regulator Parameters**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Short Circuit Current | $I_{SS}$ | — | 450 | 650 | mA |
| Short Circuit Tolerance ($V_{CAP}$ shorted to ground) | $T_{RSC}$ | — | — | 30 | minutes |

## 10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.




Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

**Figure 10-2 Input Signal Measurement References**

**Figure 10-3** shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached $V_{OL}$ or $V_{OH}$
- Data Invalid state, when a signal level is in transition between $V_{OL}$ and $V_{OH}$

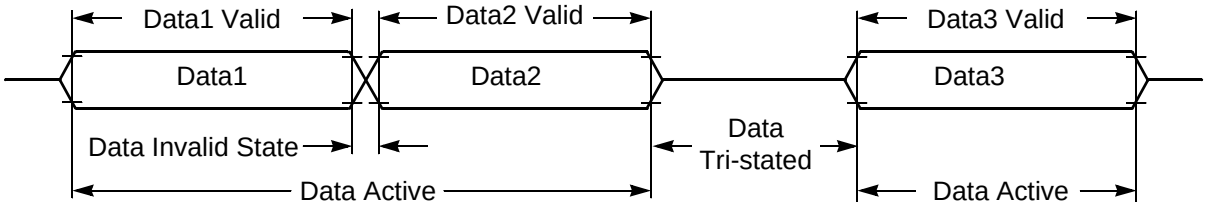



**Figure 10-3 Signal States**

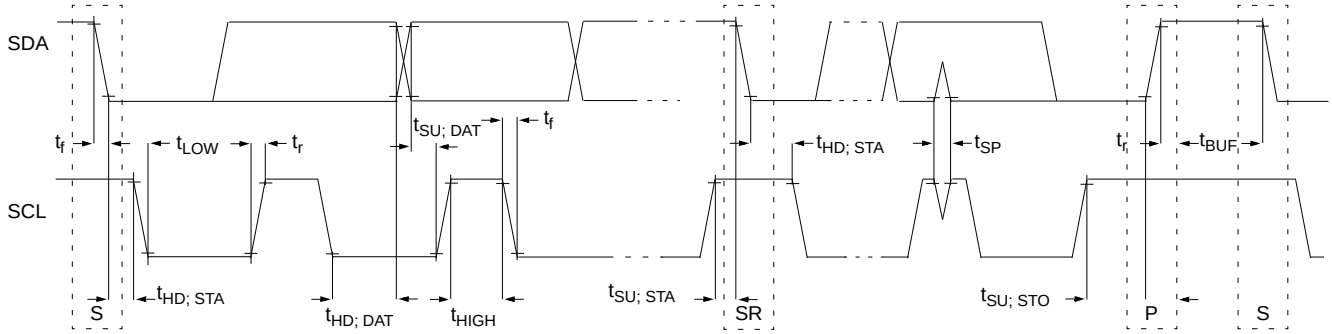



**Figure 10-14 Timing Definition for Fast and Standard Mode Devices on the $I^2C$ Bus**

## 10.13 JTAG Timing

**Table 10-18 JTAG Timing**

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|---|---|---|---|---|
| TCK frequency of operation[1] | $f_{OP}$ | DC | SYS_CLK/8 | MHz | 10-15 |
| TCK clock pulse width | $t_{PW}$ | 50 | — | ns | 10-15 |
| TMS, TDI data set-up time | $t_{DS}$ | 5 | — | ns | 10-16 |
| TMS, TDI data hold time | $t_{DH}$ | 5 | — | ns | 10-16 |
| TCK low to TDO data valid | $t_{DV}$ | — | 30 | ns | 10-16 |
| TCK low to TDO tri-state | $t_{TS}$ | — | 30 | ns | 10-16 |

1. TCK frequency of operation must be less than 1/8 the processor rate.

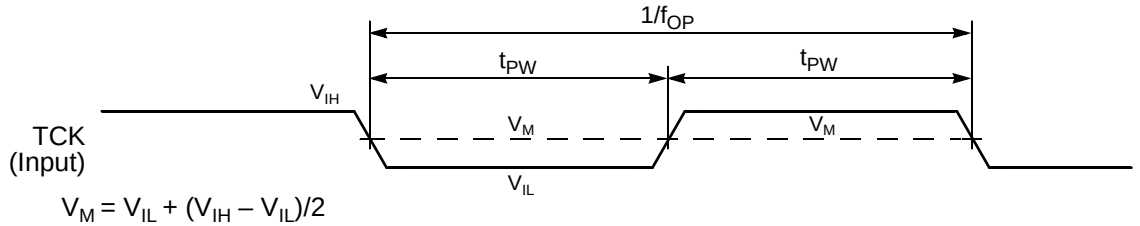



**Figure 10-15 Test Clock Input Timing Diagram**

# 10.14 Analog-to-Digital Converter (ADC) Parameters

**Table 10-19 ADC Parameters[1]**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DC Specifications** | | | | | |
| Resolution | $R_{ES}$ | 12 | — | 12 | Bits |
| ADC internal clock | $f_{ADIC}$ | 0.1 | — | 5.33 | MHz |
| Conversion range | $R_{AD}$ | $V_{REFL}$ | — | $V_{REFH}$ | V |
| ADC power-up time[2] | $t_{ADPU}$ | — | 6 | 13 | $t_{AIC}$ cycles[3] |
| Recovery from auto standby | $t_{REC}$ | — | 0 | 1 | $t_{AIC}$ cycles[3] |
| Conversion time | $t_{ADC}$ | — | 6 | — | $t_{AIC}$ cycles[3] |
| Sample time | $t_{ADS}$ | — | 1 | — | $t_{AIC}$ cycles[3] |
| **Accuracy** | | | | | |
| Integral non-linearity[4] (Full input signal range) | INL | — | +/- 3 | +/- 5 | LSB[5] |
| Differential non-linearity | DNL | — | +/- .6 | +/- 1 | LSB[5] |
| Monotonicity | GUARANTEED | | | | |
| Offset Voltage Internal Ref | $V_{OFFSET}$ | — | +/- 4 | +/- 9 | mV |
| Offset Voltage External Ref | $V_{OFFSET}$ | — | +/- 6 | +/- 12 | mV |
| Gain Error (transfer gain) | $E_{GAIN}$ | — | .998 to 1.002 | 1.01 to .99 | — |
| **ADC Inputs[6] (Pin Group 3)** | | | | | |
| Input voltage (external reference) | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V |
| Input voltage (internal reference) | $V_{ADIN}$ | $V_{SSA}$ | — | $V_{DDA}$ | V |
| Input leakage | $I_{IA}$ | — | 0 | +/- 2 | µA |
| $V_{REFH}$ current | $I_{VREFH}$ | — | 0 | — | µA |
| Input injection current[7], per pin | $I_{ADI}$ | — | — | 3 | mA |
| Input capacitance | $C_{ADI}$ | — | See **Figure 10-17** | — | pF |
| Input impedance | $X_{IN}$ | — | See **Figure 10-17** | — | Ohms |
| **AC Specifications** | | | | | |
| Signal-to-noise ratio | SNR | 60 | 65 | | dB |
| Total Harmonic Distortion | THD | 60 | 64 | | dB |
| Spurious Free Dynamic Range | SFDR | 61 | 66 | | dB |
| Signal-to-noise plus distortion | SINAD | 58 | 62 | | dB |
| Effective Number Of Bits | ENOB | — | 10.0 | | Bits |

1. All measurements were made at $V_{DD}$ = 3.3V, $V_{REFH}$ = 3.3V, and $V_{REFL}$ = ground
2. Includes power-up of ADC and $V_{REF}$
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.

- Cload is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all $V^2/R$ or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10mA into LEDs, then P = 8*.5*.01 = 40mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

# Part 11 Packaging

## 11.1 56F8033/56F8023 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8033/56F8023. This device comes in a 32-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline, **Figure 11-2** shows the mechanical parameters and **Table 11-1** lists the pin-out.

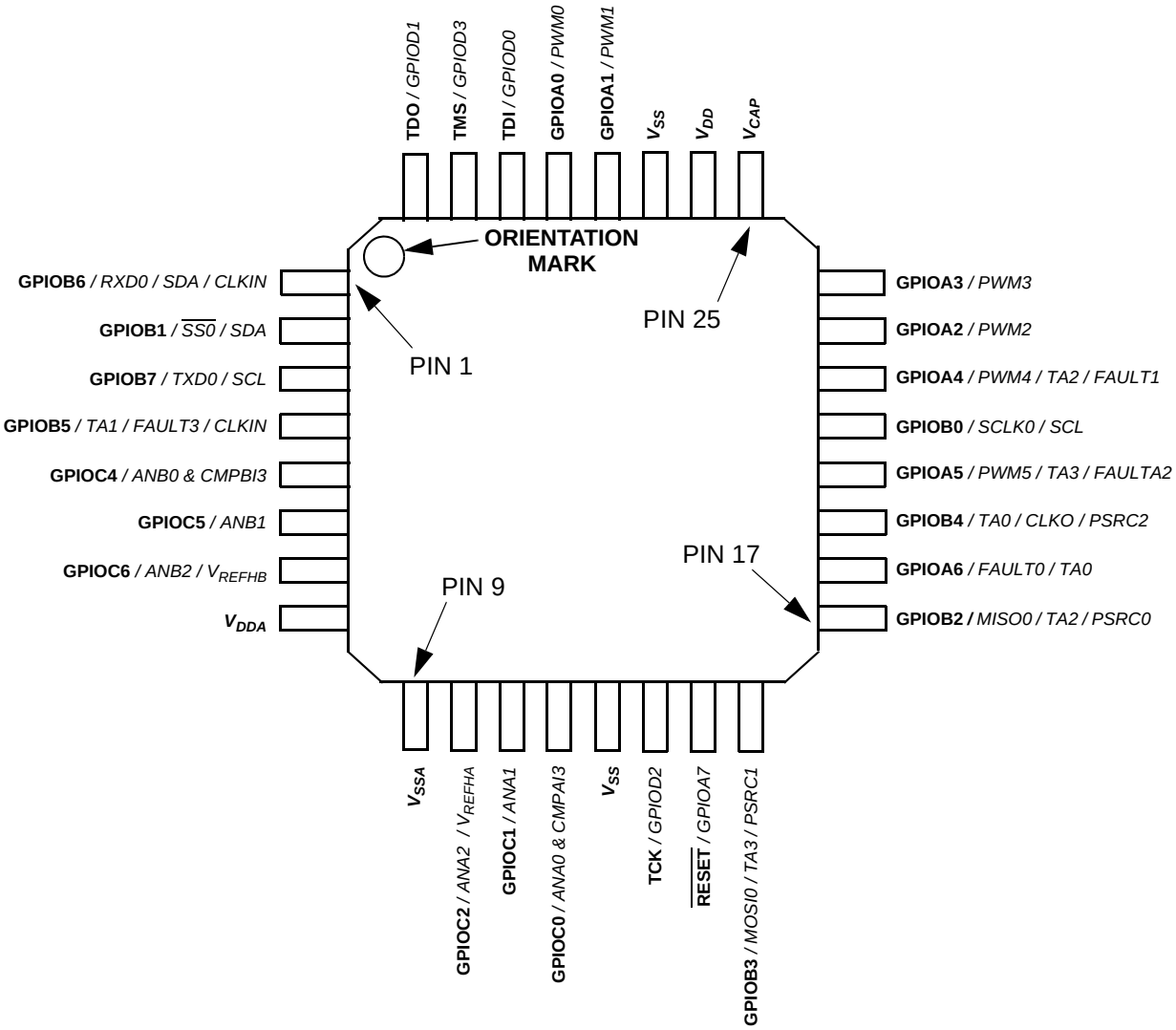



**Figure 11-1 Top View, 56F8033/56F8023 32-Pin LQFP Package**

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

## 12.2 Electrical Design Considerations

**CAUTION**

**This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.**

Use the following list of considerations to assure correct operation of the 56F8033/56F8023:

- Provide a low-impedance path from the board power supply to each $V_{DD}$ pin on the 56F8033/56F8023 and from the board ground to each $V_{SS}$ (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the $V_{DD}/V_{SS}$ pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip $V_{DD}$ and $V_{SS}$ (GND) pins are as short as possible
- Bypass the $V_{DD}$ and $V_{SS}$ with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the $V_{DD}$ and $V_{SS}$ circuits.

## Table 14-1 Legacy and Revised Acronyms (Continued)

| Register Name | Peripheral Reference Manual | | Data Sheet | | Processor Expert Acronym | Memory Address | |
|---|---|---|---|---|---|---|---|
| | New Acronym | Legacy Acronym | New Acronym | Legacy Acronym | | Start | End |
| Timeout Register | TOUT | COPTO | COP_TOUT | COPTO | COPTO | 0XF121 | |
| Counter Register | CNTR | COPCTR | COP_CNTR | COPCTR | COPCTR | 0XF122 | |