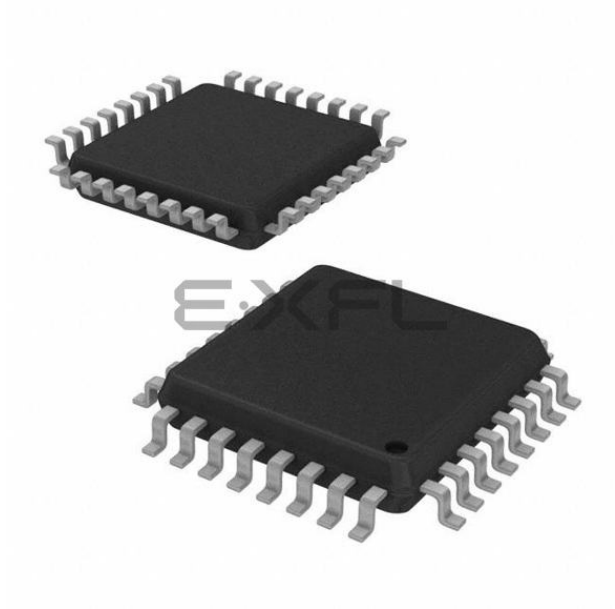


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800E |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 32KB (16K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 16 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-LQFP |
| Supplier Device Package | 32-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8023vlcr |

## 1.5 Product Documentation

The documents listed in **Table 1-2** are required for a complete description and proper design with the 56F8033/56F8023. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at:
**http://www.freescale.com**

**Table 1-2 56F8033/56F8023 Chip Documentation**

| Topic | Description | Order Number |
|---|---|---|
| DSP56800E Reference Manual | Detailed description of the 56800E family architecture, 16-bit Digital Signal Controller core processor, and the instruction set | DSP56800ERM |
| **56F802X and 56F803X Peripheral Reference Manual** | Detailed description of peripherals of the 56F802x and 56F803x family of devices | MC56F80xxRM |
| 56F802x and 56F803x Serial Bootloader User Guide | Detailed description of the Serial Bootloader in the 56F802x and 56F803x family of devices | 56F80xxBLUG |
| 56F8033/56F8023 Technical Data Sheet | Electrical and timing specifications, pin descriptions, and package descriptions (this document) | MC56F8033/56F8023 |
| 56F8033/56F8023 Errata | Details any chip issues that might be present | MC56F8033/56F8023E |

## 1.6 Data Sheet Conventions

This data sheet uses the following conventions:

| | |
|---|---|
| $\overline{\text{OVERBAR}}$ | This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low. |
| “asserted” | A high true (active high) signal is high or a low true (active low) signal is low. |
| “deasserted” | A high true (active high) signal is low or a low true (active low) signal is high. |

| Examples: | Signal/Symbol | Logic State | Signal State | Voltage[1] |
|---|---|---|---|---|
| | $\overline{\text{PIN}}$ | True | Asserted | $V_{IL}/V_{OL}$ |
| | $\overline{\text{PIN}}$ | False | Deasserted | $V_{IH}/V_{OH}$ |
| | PIN | True | Asserted | $V_{IH}/V_{OH}$ |
| | PIN | False | Deasserted | $V_{IL}/V_{OL}$ |

1. Values for $V_{IL}$, $V_{OL}$, $V_{IH}$, and $V_{OH}$ are defined by individual product specifications.

## Table 2-3 56F8033/56F8023 Signal and Package Information for the 32-Pin LQFP

| Signal Name | LQFP Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| **GPIOA1**<br><br>**(PWM1)** | 28 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM1** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA1. |
| **GPIOA2**<br><br>**(PWM2)** | 23 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM2** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA2. |
| **GPIOA3**<br><br>**(PWM3)** | 24 | Input/ Output<br><br>Output | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM3** — This is one of the six PWM output pins.<br><br>After reset, the default state is GPIOA3. |
| **GPIOA4**<br><br>**(PWM4)**<br><br>**(TA2[1])**<br><br>**(FAULT1[2])** | 22 | Input/ Output<br><br>Output<br><br>Input/ Output<br><br>Input | Input, internal pull-up enabled | **Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>**PWM4** — This is one of the six PWM output pins.<br><br>**TA2** — Timer A, Channel 2<br><br>**Fault1** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.<br><br>After reset, the default state is GPIOA4. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**. |

[1]The TA2 signal is also brought out on the GPIOB2-3 pin.
[2]The Fault1 signal is also brought out on the GPIOB4 pin.

**Return to Table 2-2**

## Table 4-2 Interrupt Vector Table Contents[1] (Continued)

| Peripheral | Vector Number | Priority Level | Vector Base Address + | Interrupt Function |
|---|---|---|---|---|
| FM | 17 | 0-2 | P:$22 | FM Access Error Interrupt |
| FM | 18 | 0-2 | P:$24 | FM Command Complete |
| FM | 19 | 0-2 | P:$26 | FM Command, Data, and Address Buffers Empty |
| | 20 - 23 | | | Reserved |
| GPIOD | 24 | 0-2 | P:$30 | GPIOD |
| GPIOC | 25 | 0-2 | P:$32 | GPIOC |
| GPIOB | 26 | 0-2 | P:$34 | GPIOB |
| GPIOA | 27 | 0-2 | P:$36 | GPIOA |
| QSPI0 | 28 | 0-2 | P:$38 | QSPI0 Receiver Full |
| QSPI0 | 29 | 0-2 | P:$3A | QSPI0 Transmitter Empty |
| | 30 - 31 | | | Reserved |
| QSCI0 | 32 | 0-2 | P:$40 | QSCI0 Transmitter Empty |
| QSCI0 | 33 | 0-2 | P:$42 | QSCI0 Transmitter Idle |
| QSCI0 | 34 | 0-2 | P:$44 | QSCI0 Receiver Error |
| QSCI0 | 35 | 0-2 | P:$46 | QSCI0 Receiver Full |
| | 36 - 39 | | | Reserved |
| I2C | 40 | 0-2 | P:$50 | $I^2C$ Error |
| I2C | 41 | 0-2 | P:$52 | $I^2C$ General |
| I2C | 42 | 0-2 | P:$54 | $I^2C$ Receive |
| I2C | 43 | 0-2 | P:$56 | $I^2C$ Transmit |
| I2C | 44 | 0-2 | P:$58 | $I^2C$ Status |
| TMRA | 45 | 0-2 | P:$5A | Timer A, Channel 0 |
| TMRA | 46 | 0-2 | P:$5C | Timer A, Channel 1 |
| TMRA | 47 | 0-2 | P:$5E | Timer A, Channel 2 |
| TMRA | 48 | 0-2 | P:$60 | Timer A, Channel 3 |
| | 49 - 52 | | | Reserved |
| CMPA | 53 | 0-2 | P:$6A | Comparator A |
| CMPB | 54 | 0-2 | P:$6C | Comparator B |
| PIT0 | 55 | 0-2 | P:$6E | Interval Timer 0 |
| | 56 - 57 | | | Reserved |
| ADC | 58 | 0-2 | P:$74 | ADC A Conversion Complete |
| ADC | 59 | 0-2 | P:$76 | ADC B Conversion Complete |
| ADC | 60 | 0-2 | P:$78 | ADC Zero Crossing or Limit Error |
| PWM | 61 | 0-2 | P:$7A | Reload PWM |
| PWM | 62 | 0-2 | P:$7C | PWM Fault |
| SWILP | 63 | -1 | P:$7E | SW Interrupt Low Priority |

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.
2. If the VBA is set to the reset value, the first two locations of the vector table will overlay the chip reset addresses since the reset address would match the base of this vector table.

## Table 4-17 GPIOA Registers Address Map (GPIOA_BASE = $00 F150)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| GPIOA_PUPEN | $0 | Pull-up Enable Register |
| GPIOA_DATA | $1 | Data Register |
| GPIOA_DDIR | $2 | Data Direction Register |
| GPIOA_PEREN | $3 | Peripheral Enable Register |
| GPIOA_IASSRT | $4 | Interrupt Assert Register |
| GPIOA_IEN | $5 | Interrupt Enable Register |
| GPIOA_IEPOL | $6 | Interrupt Edge Polarity Register |
| GPIOA_IPEND | $7 | Interrupt Pending Register |
| GPIOA_IEDGE | $8 | Interrupt Edge-Sensitive Register |
| GPIOA_PPOUTM | $9 | Push-Pull Output Mode Control Register |
| GPIOA_RDATA | $A | Raw Data Input Register |
| GPIOA_DRIVE | $B | Output Drive Strength Control Register |

## Table 4-18 GPIOB Registers Address Map (GPIOB_BASE = $00 F160)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| GPIOB_PUPEN | $0 | Pull-up Enable Register |
| GPIOB_DATA | $1 | Data Register |
| GPIOB_DDIR | $2 | Data Direction Register |
| GPIOB_PEREN | $3 | Peripheral Enable Register |
| GPIOB_IASSRT | $4 | Interrupt Assert Register |
| GPIOB_IEN | $5 | Interrupt Enable Register |
| GPIOB_IEPOL | $6 | Interrupt Edge Polarity Register |
| GPIOB_IPEND | $7 | Interrupt Pending Register |
| GPIOB_IEDGE | $8 | Interrupt Edge-Sensitive Register |
| GPIOB_PPOUTM | $9 | Push-Pull Output Mode Control Register |
| GPIOB_RDATA | $A | Raw Data Input Register |
| GPIOB_DRIVE | $B | Output Drive Strength Control Register |

## Table 4-19 GPIOC Registers Address Map (GPIOC_BASE = $00 F170)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| GPIOC_PUPEN | $0 | Pull-up Enable Register |

## 5.4 Block Diagram

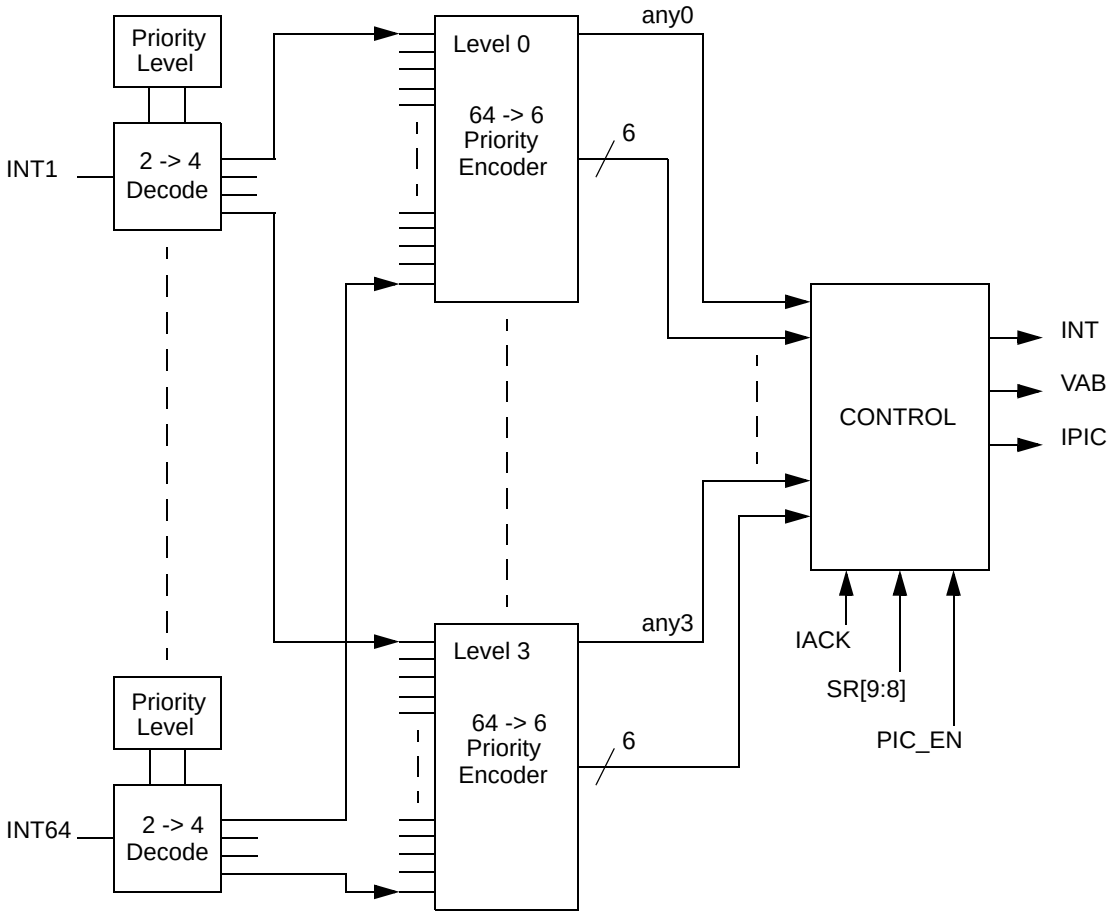



**Figure 5-1 Interrupt Controller Block Diagram**

## 5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode.

## 5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the

#### 5.6.2.5 FM Error Interrupt Priority Level (FM_ERR IPL)—Bits 1–0

This field is used to set the interrupt priority level for the FM Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

### 5.6.3 Interrupt Priority Register 2 (IPR2)

| Base + $2 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | QSCI0_XMIT IPL | | 0 | 0 | 0 | 0 | QSPI0_XMIT IPL | | QSPI0_RCV IPL | | GPIOA IPL | | GPIOB IPL | | GPIOC IPL | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 5-5 Interrupt Priority Register 2 (IPR2)**

#### 5.6.3.1 QSCI 0 Transmitter Empty Interrupt Priority Level (QSCI0_XMIT IPL)—Bits 15–14

This field is used to set the interrupt priority level for the QSCI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.3.2 Reserved—Bits 13–10

This bit field is reserved. Each bit must be set to 0.

#### 5.6.3.3 QSPI 0 Transmitter Empty Interrupt Priority Level (QSPI0_XMIT IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSPI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.4.1 $I^2C$ Error Interrupt Priority Level (I2C_ERR IPL)—Bits 15–14

This field is used to set the interrupt priority level for the $I^2C$ Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.4.2 Reserved—Bits 13–6

This bit field is reserved. Each bit must be set to 0.

#### 5.6.4.3 QSCI 0 Receiver Full Interrupt Priority Level (QSCI0_RCV IPL)—Bits 5–4

This field is used to set the interrupt priority level for the QSCI0 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.4.4 QSCI 0 Receiver Error Interrupt Priority Level (QSCI0_RERR IPL)—Bits 3–2

This field is used to set the interrupt priority level for the QSCI0 Receiver Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.4.5 QSCI 0 Transmitter Idle Interrupt Priority Level (QSCI0_TIDL IPL)—Bits 1–0

This field is used to set the interrupt priority level for the QSCI0 Transmitter Idle IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.5.4 Timer A, Channel 0 Interrupt Priority Level (TMRA_0 IPL)—Bits 9–8

This field is used to set the interrupt priority level for the Timer A, Channel 0 IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.5.5 $I^2C$ Status Interrupt Priority Level (I2C_STAT IPL)—Bits 7–6

This field is used to set the interrupt priority level for the $I^2C$ Status IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.5.6 $I^2C$ Transmit Interrupt Priority Level (I2C_TX IPL)—Bits 5–4

This field is used to set the interrupt priority level for the $I^2C$ Transmit IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.5.7 $I^2C$ Receive Interrupt Priority Level (I2C_RX IPL)— Bits 3–2

This field is used to set the interrupt priority level for the $I^2C$ Receiver IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.5.8 $I^2C$ General Call Interrupt Priority Level (I2C_GEN IPL)—Bits 1–0

This field is used to set the interrupt priority level for the $I^2C$ General Call IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1

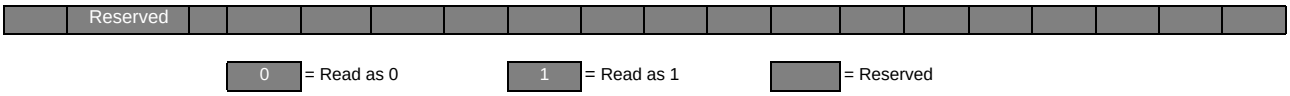



**Figure 6-1 SIM Register Map Summary**

## 6.3.1 SIM Control Register (SIM_CTRL)

| Base + $0 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ONCE EBL | SW RST | STOP_ DISABLE | | WAIT_ DISABLE | |
| Write | | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 6-2 SIM Control Register (SIM_CTRL)**

### 6.3.1.1 Reserved—Bits 15–6

This bit field is reserved. Each bit must be set to 0.

### 6.3.1.2 OnCE Enable (ONCEEBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

**Note:** Using default state “0” is recommended.

### 6.3.1.3 Software Reset (SWRST)—Bit 4

- Writing 1 to this field will cause the device to reset
- Read is zero

### 6.3.1.4 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 = Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 = The 56800E STOP instruction will not cause entry into Stop mode
- 10 = Stop mode will be entered when the 56800E core executes a STOP instruction and the STOP_DISABLE field is write-protected until the next reset
- 11 = The 56800E STOP instruction will not cause entry into Stop mode and the STOP_DISABLE field is write-protected until the next reset

### 6.3.1.5 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 = Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 = The 56800E WAIT instruction will not cause entry into Wait mode
- 10 = Wait mode will be entered when the 56800E core executes a WAIT instruction and the WAIT_DISABLE field is write-protected until the next reset
- 11 = The 56800E WAIT instruction will not cause entry into Wait mode and the WAIT_DISABLE field is write-protected until the next reset

#### 6.3.17.3 Configure GPIOB5 (GPS_B5)—Bits 12–11

This field selects the alternate function for GPIOB5.

- 00 = TA1 - Timer A1 (default)
- 01 = FAULT3 - PWM FAULT3 Input
- 10 = CLKIN - External Clock Input
- 11 = Reserved

#### 6.3.17.4 Configure GPIOB4 (GPS_B4)—Bits 10–8

This field selects the alternate function for GPIOB4.

- 000 = TA0 - Timer A0 (default)
- 001 = CLKO - Clock Output
- 010 = Reserved
- 011 = TB0 - Timer B0
- 100 = PSRC2 - PWM4 / PWM5 Pair External Source
- 11x = Reserved
- 1x1 = Reserved

#### 6.3.17.5 Configure GPIOB3 (GPS_B3)—Bits 7–6

This field selects the alternate function for GPIOB3.

- 00 = MOSI0 - QSPI0 Master Out/Slave In (default)
- 01 = TA3 - Timer A3
- 10 = PSRC1 - PWM2 / PWM3 Pair External Source
- 11 = Reserved

#### 6.3.17.6 Configure GPIOB2 (GPS_B2)—Bits 5–4

This field selects the alternate function for GPIOB2.

- 00 = MISO0 QSPI0 Master In/Slave Out (default)
- 01 = TA2 - Timer A2
- 10 = PSRC0 - PWM0 / PWM1 Pair External Source
- 11 = Reserved

#### 6.3.17.7 Reserved—Bit 3

This bit field is reserved. It must be set to 0.

#### 6.3.17.8 Configure GPIOB1 (GPS_B1)—Bit 2

This field selects the alternate function for GPIOB1.

- 0 = $\overline{SS}$0 - QSPI0 Slave Select (default)
- 1 = SDA - I2C Serial Data

## 6.5 Power-Saving Modes

The 56F8033/56F8023 operates in one of five Power-Saving modes, as shown in **Table 6-2**.

**Table 6-2 Clock Operation in Power-Saving Modes**

| Mode | Core Clocks | Peripheral Clocks | Description |
|---|---|---|---|
| Run | Core and memory clocks enabled | Peripheral clocks enabled | Device is fully functional |
| Wait | Core and memory clocks disabled | Peripheral clocks enabled | Core executes WAIT instruction to enter this mode.<br>Typically used for power-conscious applications.<br>Possible recoveries from Wait mode to Run mode are:<br>1. Any interrupt<br>2. Executing a Debug mode entry command during the 56800E core JTAG interface<br>3. Any reset (POR, external, software, COP) |
| Stop | Master clock generation in the OCCS remains operational, but the SIM disables the generation of system and peripheral clocks. | | Core executes STOP instruction to enter this mode.<br>Possible recoveries from Stop mode to Run mode are:<br>1. Interrupt from any peripheral configured in the CTRL register to operate in Stop mode (TA0-3, QSCI0, PIT0-1, CAN, CMPA-B)<br>2. Low-voltage interrupt<br>3. Executing a Debug mode entry command using the 56800E core JTAG interface<br>4. Any reset (POR, external, software, COP) |
| Standby | The OCCS generates the master clock at a reduced frequency (400kHz). The PLL is disabled and the high-speed peripheral option is not available. System and peripheral clocks operate at 200kHz. | | The user configures the OCCS and SIM to select the relaxation oscillator clock source (PRECS), shut down the PLL (PLLPD), put the relaxation oscillator in Standby mode (ROSB), and put the large regulator in Standby (LRSTDBY). The device is fully operational, but operating at a minimum frequency and power configuration. Recovery requires reversing the sequence used to enter this mode (allowing for PLL lock time). |
| Power-Down | Master clock generation in the OCCS is completely shut down. All system and peripheral clocks are disabled. | | The user configures the OCCS and SIM to enter Standby mode as shown in the previous description, followed by powering down the oscillator (ROPD). The only possible recoveries from this mode are:<br>1. External Reset<br>2. Power-On Reset |

The power-saving modes provide additional power management options by disabling the clock, reconfiguring the voltage regulator clock generation to manage power utilization, as shown in **Table 6-2**. Run, Wait, and Stop modes provide methods of enabling/disabling the peripheral and/or core clocking as a group. Stop disable controls for an individual peripheral are provided in the SD*n* registers to override the

The deassertion sequence of internal resets coordinates the device start up, including the clocking system start up. The sequence is described in the following steps:

1. As power is applied, the Relaxation Oscillator starts to operate. When a valid operating voltage is reached, the POR reset will release.
2. The release of POR reset permits operation of the POR reset extender. The POR extender generates an extended POR reset, which is released 64 OSC_CLK cycles after POR reset. This provides an additional time period for the clock source and power to stabilize.
3. A Combined reset consists of the OR of the extended POR reset, the external reset, the COP reset and Software reset. The entire device, except for the POR extender, is held reset as long as Combined reset is asserted. The release of Combined reset permits operation of the CTRL register, the Synchronous reset generator, and the CLKGEN reset extender.
4. The Synchronous reset generator generates a reset to the Software and COP reset logic. The COP and Software reset logic is released three OSC_CLK cycles after Combined reset deasserts. This provides a reasonable minimum duration to the reset for these specialized functions.
5. The CLKGEN reset extender generates the CLKGEN reset used by the clock generation logic. The CLKGEN reset is released 32 OSC_CLK cycles after Combined reset deasserts. This provides a window in which the SIM stabilizes the master clock inputs to the clock generator.
6. The release of CLKGEN reset permits operation of the clock generation logic and the Peripheral reset extender. The Peripheral reset extender generates the Peripheral reset, which is released 32 SYS_CLK cycles after CLKGEN reset. This provides a window in which peripheral and core logic remain clocked, but in reset, so that synchronous resets can be resolved.
7. The release of Peripheral reset permits operation of the peripheral logic and the Core reset extender. The Core reset extender generates the Core reset, which is released 32 SYS_CLK cycles after the Peripheral reset. This provides a window in which critical peripheral start-up functions, such as Flash Security in the Flash memory, can be implemented.
8. The release of Core reset permits execution of code by the 56800E core and marks the end of the system start-up sequence.

**Figure 6-27** illustrates clock relationships to one another and to the various resets as the device comes out of reset. $\overline{\text{RST}}$ is assumed to be the logical AND of all active-low system resets (for example, POR, external reset, COP and Software reset). In the 56F8033/56F8023, this signal will be stretched by the SIM for a period of time (up to 96 OSC_CLK clock cycles, depending upon the status of the POR) to create the clock generation reset signal (CLKGEN_$\overline{\text{RST}}$). The SIM should deassert CLKGEN_$\overline{\text{RST}}$ synchronously with the negative edge of OSC_CLK in order to avoid skew problems. CLKGEN_$\overline{\text{RST}}$ is delayed 32 SYS_CLK cycles to create the peripheral reset signal (PERIP_$\overline{\text{RST}}$). PERIP_$\overline{\text{RST}}$ is then delayed by 32 SYS_CLK cycles to create CORE_$\overline{\text{RST}}$. Both PERIP_$\overline{\text{RST}}$ and CORE_$\overline{\text{RST}}$ should be released on the negative edge of SYS_CLK_D as shown. This phased releasing of system resets is necessary to give some peripherals (for example, the Flash interface unit) set-up time prior to the 56800E core becoming active.

in order to return to normal unsecured operation. Power-on reset will also reset both.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word $0000 into program memory location $00 7FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

**Note:** Flash contents can only be programmed for 1s to 0s.

## 7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in section 7.2.4. The customer would need to supply Technical Support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

# Part 8 General-Purpose Input/Output (GPIO)

## 8.1 Introduction

This section is intended to supplement the GPIO information found in the **56F802X and 56F803X Peripheral Reference Manual** and contains only chip-specific information. This information supersedes the generic information in the **56F802X and 56F803X Peripheral Reference Manual**.

## 8.2 Configuration

There are four GPIO ports defined on the 56F8033/56F8023. The width of each port, the associated peripheral and reset functions are shown in **Table 8-1**. The specific mapping of GPIO port pins is shown in **Table 8-2**. Additional details are shown in **Tables 2-2** and **2-3**.

**Table 8-1 GPIO Ports Configuration**

| GPIO Port | Available Pins in 56F8033/56F8023 | Peripheral Function | Reset Function |
|---|---|---|---|
| A | 8 | PWM, Timer, QSPI, Comparator, Reset | GPIO, $\overline{\text{RESET}}$ |
| B | 8 | QSPI, $I^2C$, PWM, Clock, Comparator, Timer | GPIO |
| C | 6 | ADC, Comparator, QSCI | GPIO |
| D | 4 | Clock, Oscillator, JTAG | GPIO, JTAG |

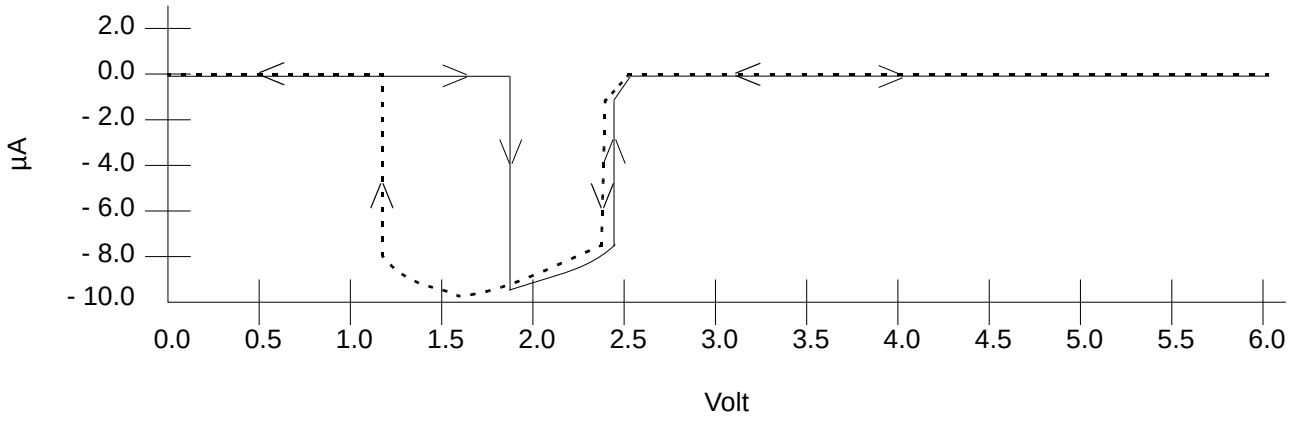



**Figure 10-1 $I_{IN}/I_{OZ}$ vs. $V_{IN}$ (Typical; Pull-Up Disabled)**

## Table 10-6 Current Consumption per Power Supply Pin

| Mode | Conditions | Typical @ 3.3V, 25°C | | Maximum@ 3.6V, 25°C | |
|---|---|---|---|---|---|
| | | $I_{DD}$[1] | $I_{DDA}$ | $I_{DD}$[1] | $I_{DDA}$ |
| RUN | 32MHz Device Clock<br>Relaxation Oscillator on<br>PLL powered on<br>Continuous MAC instructions with fetches from Program Flash<br>All peripheral modules enabled. TMR and PWM using 1X Clock<br>ADC/DAC powered on and clocked<br>Comparator powered on | 48mA | 18.8mA | — | — |
| WAIT | 32MHz Device Clock<br>Relaxation Oscillator on<br>PLL powered on<br>Processor Core in WAIT state<br>All Peripheral modules enabled. TMR and PWM using 1X Clock<br>ADC/DAC/Comparator powered off | 29mA | 0µA | — | — |
| STOP | 4MHz Device Clock<br>Relaxation Oscillator on<br>PLL powered off<br>Processor Core in STOP state<br>All peripheral module and core clocks are off<br>ADC/DAC/Comparator powered off | 5.4mA | 0µA | — | — |

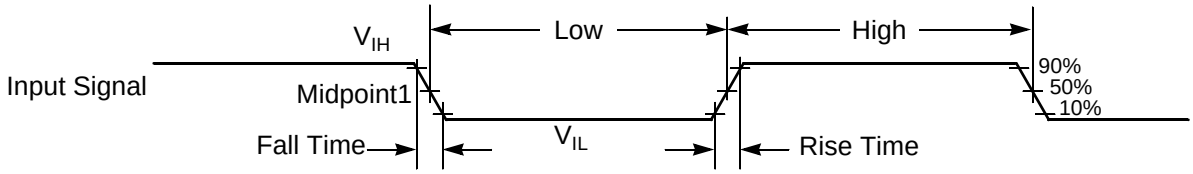
measured directly on the $V_{CAP}$ pin. The specifications for this regulator are shown in **Table 10-8**.

**Table 10-8. Regulator Parameters**

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Short Circuit Current | $I_{SS}$ | — | 450 | 650 | mA |
| Short Circuit Tolerance ($V_{CAP}$ shorted to ground) | $T_{RSC}$ | — | — | 30 | minutes |

## 10.3 AC Electrical Characteristics

Tests are conducted using the input levels specified in **Table 10-5**. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in **Figure 10-2**.




Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

**Figure 10-2 Input Signal Measurement References**

**Figure 10-3** shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached $V_{OL}$ or $V_{OH}$
- Data Invalid state, when a signal level is in transition between $V_{OL}$ and $V_{OH}$

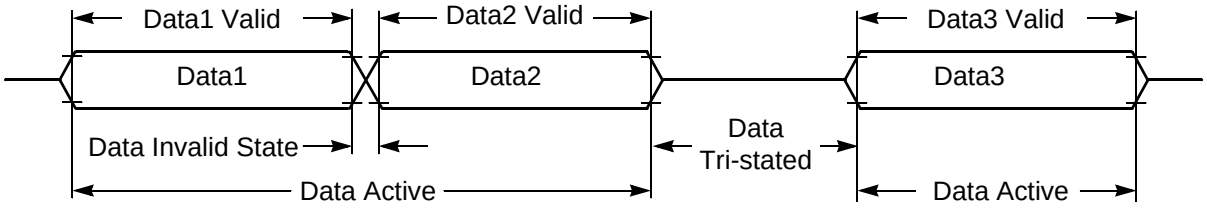



**Figure 10-3 Signal States**

## 10.6 Phase Locked Loop Timing

### Table 10-11 PLL Timing

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| External reference crystal frequency for the PLL[1] | $f_{osc}$ | 4 | 8 | — | MHz |
| Internal reference relaxation oscillator frequency for the PLL | $f_{rosc}$ | — | 8 | — | MHz |
| PLL output frequency[2] (24 x reference frequency) | $f_{op}$ | 96 | 192 | — | MHz |
| PLL lock time[3] | $t_{plls}$ | — | 40 | 100 | µs |
| Accumulated jitter using an 8MHz external crystal as the PLL source[4] | $J_A$ | — | — | 0.37 | % |
| Cycle-to-cycle jitter | $t_{jitterpll}$ | — | 350 | — | ps |

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input.
2. The core system clock will operate at 1/6 of the PLL output frequency.
3. This is the time required after the PLL is enabled to ensure reliable operation.
4. This is measured on the CLKO signal (programmed as System clock) over 264 System clocks at 32MHz System clock frequency and using an 8MHz oscillator frequency.

## 10.7 Relaxation Oscillator Timing

### Table 10-12 Relaxation Oscillator Timing

| Characteristic | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Relaxation Oscillator output frequency[1]<br>Normal Mode<br>Standby Mode | $f_{op}$ | — | <br>8.05<br>200 | — | <br>MHz<br>kHz |
| Relaxation Oscillator stabilization time[2] | $t_{roscs}$ | — | 1 | 3 | ms |
| Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3] | $t_{jitterrosc}$ | — | 400 | — | ps |
| Minimum tuning step size | | — | .08 | — | % |
| Maximum tuning step size | | — | 40 | — | % |
| Variation over temperature -40°C to 150ºC[4] | | — | +1.0 to -1.5 | +3.0 to -3.0 | % |
| Variation over temperature 0°C to 105ºC[4] | | — | 0 to +1 | +2.0 to -2.0 | % |

1. Output frequency after factory trim.
2. This is the time required from Standby to Normal mode transition.
3. $J_A$ is required to meet QSCI requirements.

# 10.11 Serial Communication Interface (SCI) Timing

**Table 10-16 SCI Timing[1]**

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|---|---|---|---|---|
| Baud Rate[2] | BR | — | ($f_{MAX}$/16) | Mbps | — |
| RXD[3] Pulse Width | $RXD_{PW}$ | 0.965/BR | 1.04/BR | ns | 10-12 |
| TXD[4] Pulse Width | $TXD_{PW}$ | 0.965/BR | 1.04/BR | ns | 10-13 |
| LIN Slave Mode | | | | | |
| Deviation of slave node clock from nominal clock rate before synchronization | $F_{TOL\_UNSYNCH}$ | -14 | 14 | % | — |
| Deviation of slave node clock relative to the master node clock after synchronization | $F_{TOL\_SYNCH}$ | -2 | 2 | % | — |
| Minimum break character length | $T_{BREAK}$ | 13 | — | Master node bit periods | — |
| | | 11 | — | Slave node bit periods | — |

1. Parameters listed are guaranteed by design.
2. $f_{MAX}$ is the frequency of operation of the system clock in MHz, which is 32MHz for the 56F8033/56F8023 device.
3. The RXD pin in QSCI0 is named RXD0 and the RXD pin in QSCI1 is named RXD1.
4. The TXD pin in QSCI0 is named TXD0 and the TXD pin in QSCI1 is named TXD1.


**Figure 10-12 RXD Pulse Width**


**Figure 10-13 TXD Pulse Width**

# 10.14 Analog-to-Digital Converter (ADC) Parameters

**Table 10-19 ADC Parameters[1]**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **DC Specifications** | | | | | |
| Resolution | $R_{ES}$ | 12 | — | 12 | Bits |
| ADC internal clock | $f_{ADIC}$ | 0.1 | — | 5.33 | MHz |
| Conversion range | $R_{AD}$ | $V_{REFL}$ | — | $V_{REFH}$ | V |
| ADC power-up time[2] | $t_{ADPU}$ | — | 6 | 13 | $t_{AIC}$ cycles[3] |
| Recovery from auto standby | $t_{REC}$ | — | 0 | 1 | $t_{AIC}$ cycles[3] |
| Conversion time | $t_{ADC}$ | — | 6 | — | $t_{AIC}$ cycles[3] |
| Sample time | $t_{ADS}$ | — | 1 | — | $t_{AIC}$ cycles[3] |
| **Accuracy** | | | | | |
| Integral non-linearity[4] (Full input signal range) | INL | — | +/- 3 | +/- 5 | LSB[5] |
| Differential non-linearity | DNL | — | +/- .6 | +/- 1 | LSB[5] |
| Monotonicity | GUARANTEED | | | | |
| Offset Voltage Internal Ref | $V_{OFFSET}$ | — | +/- 4 | +/- 9 | mV |
| Offset Voltage External Ref | $V_{OFFSET}$ | — | +/- 6 | +/- 12 | mV |
| Gain Error (transfer gain) | $E_{GAIN}$ | — | .998 to 1.002 | 1.01 to .99 | — |
| **ADC Inputs[6] (Pin Group 3)** | | | | | |
| Input voltage (external reference) | $V_{ADIN}$ | $V_{REFL}$ | — | $V_{REFH}$ | V |
| Input voltage (internal reference) | $V_{ADIN}$ | $V_{SSA}$ | — | $V_{DDA}$ | V |
| Input leakage | $I_{IA}$ | — | 0 | +/- 2 | µA |
| $V_{REFH}$ current | $I_{VREFH}$ | — | 0 | — | µA |
| Input injection current[7], per pin | $I_{ADI}$ | — | — | 3 | mA |
| Input capacitance | $C_{ADI}$ | — | See **Figure 10-17** | — | pF |
| Input impedance | $X_{IN}$ | — | See **Figure 10-17** | — | Ohms |
| **AC Specifications** | | | | | |
| Signal-to-noise ratio | SNR | 60 | 65 | | dB |
| Total Harmonic Distortion | THD | 60 | 64 | | dB |
| Spurious Free Dynamic Range | SFDR | 61 | 66 | | dB |
| Signal-to-noise plus distortion | SINAD | 58 | 62 | | dB |
| Effective Number Of Bits | ENOB | — | 10.0 | | Bits |

1. All measurements were made at $V_{DD}$ = 3.3V, $V_{REFH}$ = 3.3V, and $V_{REFL}$ = ground
2. Includes power-up of ADC and $V_{REF}$
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.

Please see **www.freescale.com** for the most current case outline.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

## 12.2 Electrical Design Considerations

**CAUTION**

**This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.**

Use the following list of considerations to assure correct operation of the 56F8033/56F8023:

- Provide a low-impedance path from the board power supply to each $V_{DD}$ pin on the 56F8033/56F8023 and from the board ground to each $V_{SS}$ (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the $V_{DD}/V_{SS}$ pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip $V_{DD}$ and $V_{SS}$ (GND) pins are as short as possible
- Bypass the $V_{DD}$ and $V_{SS}$ with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the $V_{DD}$ and $V_{SS}$ circuits.