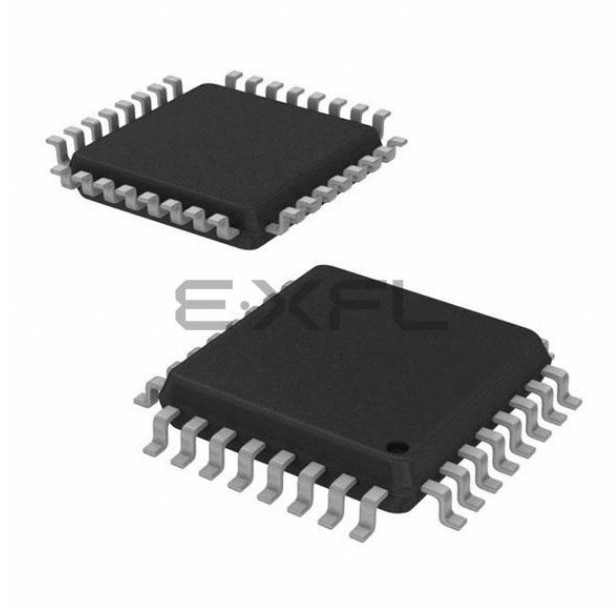

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8033vlc

In **Table 2-2**, peripheral pins in bold identify reset state.

Table 2-2 56F8033/56F8023 Pins

			Peripherals:										
Pin #	**Pin Name**	**Signal Name**	**GPIO**	**I2C**	**QSCI**	**QSPI**	**ADC**	**PWM**	**Quad Timer**	**Comp**	**Power & Ground**	**JTAG**	**Misc.**
1	**GPIOB6**	GPIOB6, RXD0, SDA, CLKIN	**B6**	SDA	RXD0								CLKIN
2	**GPIOB1**	GPIOB1, $\overline{SS0}$, SDA	**B1**	SDA		$\overline{SS0}$							
3	**GPIOB7**	GPIOB7, TXD0, SCL	**B7**	SCL	TXD0								
4	**GPIOB5**	GPIOB5, TA1, FAULT3, CLKIN	**B5**					FAULT3	TA1				CLKIN
5	**GPIOC4**	GPIOC4, ANB0 & CMPBI3	**C4**				ANB0			CMPBI3			
6	**GPIOC5**	GPIOC5, ANB1	**C5**				ANB1						
7	**GPIOC6**	GPIOC6, ANB2, V_{REFHB}	**C6**				ANB2 V_{REFHB}						
8	**VDDA**	V_{DDA}									V_{DDA}		
9	**VSSA**	V_{SSA}									V_{SSA}		
10	**GPIOC2**	GPIOC2, ANA2, V_{REFHA}	**C2**				ANA2 V_{REFHA}						
11	**GPIOC1**	GPIOC1, ANA1	**C1**				ANA1						
12	**GPIOC0**	GPIOC0, ANA0 & CMPAI3	**C0**				ANA0			CMPAI3			
13	**VSS**	V_{SS}									V_{SS}		
14	**TCK**	TCK, GPIOD2	D2									**TCK**	
15	**RESET**	$\overline{RESET}$, GPIOA7	A7										**$\overline{RESET}$**
16	**GPIOB3**	GPIOB3, MOSI0, TA3, PSRC1	**B3**			MOSI0		PSRC1	TA3				
17	**GPIOB2**	GPIOB2, MISO0, TA2, PSRC0	**B2**			MISO0		PSRC0	TA2				
18	**GPIOA6**	GPIOA6, FAULT0, TA0	**A6**					FAULT0	TA0				
19	**GPIOB4**	GPIOB4, TA0, CLKO, PSRC2	**B4**					PSRC2	TA0				CLKO
20	**GPIOA5**	GPIOA5, PWM5, TA3, FAULT2	**A5**					PWM5 FAULT2	TA3				
21	**GPIOB0**	GPIOB0, SCLK0, SCL	**B0**	SCL		SCLK0							
22	**GPIOA4**	GPIOA4, PWM4, TA2, FAULT1	**A4**					PWM4 FAULT1	TA2				
23	**GPIOA2**	GPIOA2, PWM2	**A2**					PWM2					
24	**GPIOA3**	GPIOA3, PWM3	**A3**					PWM3					
25	**VCAP**	V_{CAP}									**V_{CAP}**		
26	**VDD**	V_{DD}									**V_{DD}**		
27	**VSS**	V_{SS}									**V_{SS}**		
28	**GPIOA1**	GPIOA1, PWM1	**A1**					PWM1					

Table 2-3 56F8033/56F8023 Signal and Package Information for the 32-Pin LQFP

Signal Name	LQFP Pin No.	Type	State During Reset	Signal Description
GPIOA5	20	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)		Output		**PWM5** — This is one of the six PWM output pins.
(TA3[3])		Input/ Output		**TA3** — Timer A, Channel 3
(FAULT2[4])		Input		**Fault2** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip. After reset, the default state is GPIOA5. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[3]The TA3 signal is also brought out on the GPIOB2-3 pin. [4]The Fault2 signal is also brought out on the GPIOB4 pin.				
GPIOA6	18	Input/ Output	Input, internal pull-up enabled	**Port A GPIO** — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)		Input		**Fault0** — This fault input pin is used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TA0[5])				**TA0** — Timer A, Channel 0. After reset, the default state is GPIOA6. The peripheral functionality is controlled via the SIM. See **Section 6.3.16**.
[5]The TA0 signal is also brought out on the GPIOB4 pin.				

Return to Table 2-2

Table 4-5 Data Memory Map[1] for 56F8033 (Continued)

Begin/End Address	Memory Allocation
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 8800	RESERVED
X:$00 87FF X:$00 8000	RESERVED
X:$00 7FFF X:$00 1000	RESERVED
X:$00 0FFF X:$00 0000	On-Chip Data RAM 8KB[2]

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see **Figure 4-1**.

Table 4-6 Data Memory Map[1] for 56F8023

Begin/End Address	Memory Allocation
X:$FF FFFF X:$FF FF00	EOnCE 256 locations allocated
X:$FF FEFF X:$01 0000	RESERVED
X:$00 FFFF X:$00 F000	On-Chip Peripherals 4096 locations allocated
X:$00 EFFF X:$00 8800	RESERVED
X:$00 87FF X:$00 8000	RESERVED
X:$00 7FFF X:$00 0800	RESERVED
X:$00 07FF X:$00 0000	On-Chip Data RAM 4KB[2]

1. All addresses are 16-bit Word addresses.
2. This RAM is shared with Program space starting at P: $00 8000; see **Figure 4-2**.

Table 4-19 GPIOC Registers Address Map (GPIOC_BASE = $00 F170)

Register Acronym	Address Offset	Register Description
GPIOC_DATA	$1	Data Register
GPIOC_DDIR	$2	Data Direction Register
GPIOC_PEREN	$3	Peripheral Enable Register
GPIOC_IASSRT	$4	Interrupt Assert Register
GPIOC_IEN	$5	Interrupt Enable Register
GPIOC_IEPOL	$6	Interrupt Edge Polarity Register
GPIOC_IPEND	$7	Interrupt Pending Register
GPIOC_IEDGE	$8	Interrupt Edge-Sensitive Register
GPIOC_PPOUTM	$9	Push-Pull Output Mode Control Register
GPIOC_RDATA	$A	Raw Data Input Register
GPIOC_DRIVE	$B	Output Drive Strength Control Register

Table 4-29 Flash Module Registers Address Map (FM_BASE = $00 F400)

Register Acronym	Address Offset	Register Description
FM_CLKDIV	$0	Clock Divider Register
FM_CNFG	$1	Configuration Register
	$2	Reserved
FM_SECHI	$3	Security High Half Register
FM_SECLO	$4	Security Low Half Register
	$5 - $9	Reserved
FM_PROT	$10	Protection Register
	$11 - $12	Reserved
FM_USTAT	$13	User Status Register
FM_CMD	$14	Command Register
	$15 - $17	Reserved
FM_DATA	$18	Data Buffer Register
	$19 - $A	Reserved
FM_IFROPT_1	$1B	Information Option Register 1
	$1C	Reserved
FM_TSTSIG	$1D	Test Array Signature Register

Part 5 Interrupt Controller (ITCN)

5.1 Introduction

The Interrupt Controller (ITCN) module arbitrates between various interrupt requests (IRQs), signals to the 56800E core when an interrupt of sufficient priority exists, and to what address to jump in order to service this interrupt.

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Ability to drive initial address on the address bus after reset

For further information, see **Table 4-2**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers that allow each of the 64 interrupt sources to be set to one of four priority levels (excluding certain interrupts that are of fixed priority). Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, number 0 is the highest priority and number 63 is the lowest.

5.3.1 Normal Interrupt Handling

Once the INTC has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the Vector Base Address (VBA) and the vector number to determine the vector address, generating an offset into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The 56800E core controls the masking of interrupt priority levels it will accept by setting the I0 and I1 bits in its status register.

Table 5-1 Interrupt Mask Bit Definition

SR[9] (I1)	SR[8] (I0)	Exceptions Permitted	Exceptions Masked
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

The IPIC bits of the ICTRL register reflect the state of the priority level being presented to the 56800E core.

Table 5-2 Interrupt Priority Encoding

IPIC_VALUE[1:0]	Current Interrupt Priority Level	Required Nested Exception Priority
00	No interrupt or SWILP	Priorities 0, 1, 2, 3
01	Priority 0	Priorities 1, 2, 3
10	Priority 1	Priorities 2, 3

5.6.2 Interrupt Priority Register 1 (IPR1)

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	GPIOD IPL		0	0	0	0	0	0	0	0	FM_CBE IPL		FM_CC IPL		FM_ERR IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-4 Interrupt Priority Register 1 (IPR1)

5.6.2.1 GPIOD Interrupt Priority Level (GPIOD IPL)—Bits 15–14

This field is used to set the interrupt priority level for the GPIOD IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.2 Reserved—Bits 13–6

This bit field is reserved. Each bit must be set to 0.

5.6.2.3 FM Command, Data, Address Buffers Empty Interrupt Priority Level (FM_CBE IPL)—Bits 5–4

This field is used to set the interrupt priority level for the FM Command, Data Address Buffers Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.4 FM Command Complete Interrupt Priority Level (FM_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the FM Command Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.2.5 FM Error Interrupt Priority Level (FM_ERR IPL)—Bits 1–0

This field is used to set the interrupt priority level for the FM Error IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	QSCI0_XMIT IPL		0	0	0	0	QSPI0_XMIT IPL		QSPI0_RCV IPL		GPIOA IPL		GPIOB IPL		GPIOC IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.3.1 QSCI 0 Transmitter Empty Interrupt Priority Level (QSCI0_XMIT IPL)—Bits 15–14

This field is used to set the interrupt priority level for the QSCI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.2 Reserved—Bits 13–10

This bit field is reserved. Each bit must be set to 0.

5.6.3.3 QSPI 0 Transmitter Empty Interrupt Priority Level (QSPI0_XMIT IPL)—Bits 9–8

This field is used to set the interrupt priority level for the QSPI0 Transmitter Empty IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.4 QSPI 0 Receiver Full Interrupt Priority Level (QSPI0_RCV IPL)—Bits 7–6

This field is used to set the interrupt priority level for the QSPI0 Receiver Full IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.5 GPIOA Interrupt Priority Level (GPIOA IPL)—Bits 5–4

This field is used to set the interrupt priority level for the GPIOA IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.6 GPIOB Interrupt Priority Level (GPIOB IPL)—Bits 3–2

This field is used to set the interrupt priority level for the GPIOB IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.3.7 GPIOC Interrupt Priority Level (GPIOC IPL)—Bits 1–0

This field is used to set the interrupt priority level for the GPIOC IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.4 Interrupt Priority Register 3 (IPR3)

Base + $3	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	I2C_ERR IPL		0	0	0	0	0	0	0	0	QSCI0_RCV IPL		QSCI0_RERR IPL		QSCI0_TIDL IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-6 Interrupt Priority Register 3 (IPR3)

5.6.7.5 ADC B Conversion Complete Interrupt Priority Level (ADCB_CC IPL)—Bits 5–4

This field is used to set the interrupt priority level for the ADC B Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.6 ADC A Conversion Complete Interrupt Priority Level (ADCA_CC IPL)—Bits 3–2

This field is used to set the interrupt priority level for the ADC A Conversion Complete IRQ. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.7 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

5.6.8 Vector Base Address Register (VBA)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	VECTOR_BASE_ADDRESS													
Write																
RESET[1]	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

1. The 56F8033 resets to a value of 0 x 0000. This corresponds to reset addresses of 0 x 000000.
   The 56F8023 resets to a value of 0 x 0080. This corresponds to reset addresses of 0 x 004000.

Figure 5-10 Vector Base Address Register (VBA)

5.6.8.1 Reserved—Bits 15–14

This bit field is reserved. Each bit must be set to 0.

5.6.8.2 Vector Address Bus (VAB) Bits 13–0

The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower 7 bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the Core.

5.6.19.5 Reserved—Bits 4-2

This bit field is reserved. Each bit must be set to 1.

5.6.19.6 Reserved—Bits 1–0

This bit field is reserved. Each bit must be set to 0.

5.7 Resets

5.7.1 General

Table 5-5 Reset Summary

Reset	Priority	Source	Characteristics
Core Reset		$\overline{\text{RST}}$	Core reset from the SIM

5.7.2 Description of Reset Operation

5.7.2.1 Reset Handshake Timing

The ITCN provides the 56800E core with a reset vector address on the VAB pins whenever $\overline{\text{RESET}}$ is asserted from the SIM. The reset vector will be presented until the second rising clock edge after $\overline{\text{RESET}}$ is released. The general timing is shown in **Figure 5-22**.

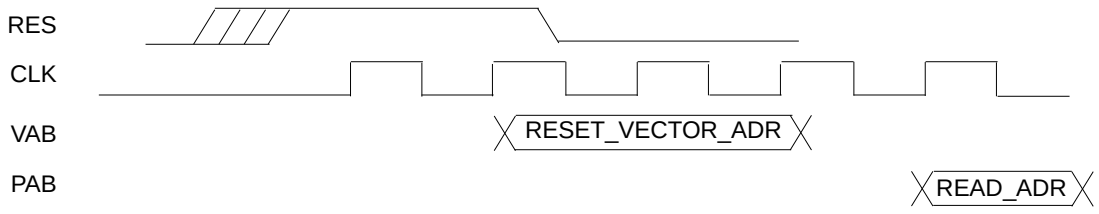

Figure 5-22 Reset Interface

5.7.3 ITCN After Reset

After reset, all of the ITCN registers are in their default states. This means all interrupts are disabled, except the core IRQs with fixed priorities:

- Illegal Instruction
- SW Interrupt 3
- HW Stack Overflow
- Misaligned Long Word Access
- SW Interrupt 2
- SW Interrupt 1
- SW Interrupt 0

6.3.6 SIM Power Control Register (SIM_PWR)

This register controls the Standby mode of the large on-chip regulator. The large on-chip regulator derives the core digital logic power supply from the IO power supply. At a system bus frequency of 200kHz, the large regulator may be put in a reduced-power standby mode without interfering with device operation to reduce device power consumption. Refer to the overview of power-down modes and the overview of clock generation for more information on the use of large regulator standby.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LRSTDBY	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-7 SIM Power Control Register (SIM_PWR)

6.3.6.1 Reserved—Bits 15–2

This bit field is reserved. Each bit must be set to 0.

6.3.6.2 Large Regulator Standby Mode[1:0] (LRSTDBY)—Bits 1–0

- 00 = Large regulator is in Normal mode
- 01 = Large regulator is in Standby (reduced-power) mode
- 10 = Large regulator is in Normal mode and the LRSTDBY field is write-protected until the next reset
- 11 = Large regulator is in Standby mode and the LRSTDBY field is write-protected until the next reset

6.3.7 Clock Output Select Register (SIM_CLKOUT)

The Clock Output Select register can be used to multiplex out selected clock sources generated inside the clock generation and SIM modules onto the muxed clock output pins. All functionality is for test purposes only. Glitches may be produced when the clock is enabled or switched. The delay from the clock source to the output is unspecified. The observability of the CLKO clock output signal at an output pad is subject to the frequency limitations of the associated IO cell.

GPIOA[3:0] can function as GPIO, PWM, or as clock output pins. If GPIOA[3:0] are programmed to operate as peripheral outputs, then the choice is between PWM and clock outputs. The default state is for the peripheral function of GPIOA[3:0] to be programmed as PWM (selected by bits [9:6] of the Clock Output Select register).

GPIOB4 can function as GPIO, or as other peripheral outputs, including clock output (CLKO). If GPIOB4 is programmed to operate as a peripheral output and CLKO is selected in the SIM_GPSB0 register, bits [4:0] decide if CLKO is enabled or disabled and which clock source is selected if CLKO is enabled. See **Figure 6-8** for details.

Add. Offset	Register Acronym		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	GPIOD_PUPEN	R													PU[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$1	GPIOD_DATA	R													D[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$2	GPIOD_DDIR	R													DD[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$3	GPIOD_PEREN	R													PE[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$4	GPIOD_IASSRT	R													IA[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$5	GPIOD_IEN	R													IEN[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$6	GPIOD_IEPOL	R													IEPOL[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$7	GPIOD_IPEND	R													IPR[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$8	GPIOD_IEDGE	R													IES[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$9	GPIOD_PPOUTM	R													OEN[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
$A	GPIOD_RDATA	R													RAW DATA[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
$B	GPIOD_DRIVE	R													DRIVE[15:0]			
		W																
		RS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R	0	Read as 0
W		Reserved
RS		Reset

Figure 8-4 GPIOD Register Map Summary

10.8 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Note: All address and data buses described here are internal.

Table 10-13 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	10-6
$\overline{\text{RESET}}$ deassertion to First Address Fetch[3]	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1. In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32MHz, T = 31.25ns. At 8MHz (used during Reset and Stop modes), T = 125ns.
2. Parameters listed are guaranteed by design.
3. During Power-On Reset, it is possible to use the 56F8033/56F8023 internal reset stretching circuitry to extend this period to 2^21T.

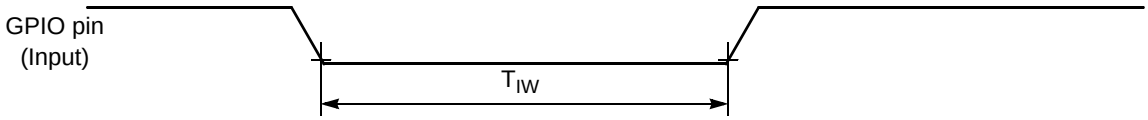

Figure 10-6 GPIO Interrupt Timing (Negative Edge-Sensitive)

10.12 Inter-Integrated Circuit Interface (I^2C) Timing

Table 10-17 I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	100[3, 4]	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	20 +0.1C_b[5]	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
4. A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;\ DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
5. C_b = total capacitance of the one bus line in pF.

10.14 Analog-to-Digital Converter (ADC) Parameters

Table 10-19 ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	5.33	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC power-up time[2]	t_{ADPU}	—	6	13	t_{AIC} cycles[3]
Recovery from auto standby	t_{REC}	—	0	1	t_{AIC} cycles[3]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy					
Integral non-linearity[4] (Full input signal range)	INL	—	+/- 3	+/- 5	LSB[5]
Differential non-linearity	DNL	—	+/- .6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 4	+/- 9	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 6	+/- 12	mV
Gain Error (transfer gain)	E_{GAIN}	—	.998 to 1.002	1.01 to .99	—
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[7], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-17**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-17**	—	Ohms
AC Specifications					
Signal-to-noise ratio	SNR	60	65		dB
Total Harmonic Distortion	THD	60	64		dB
Spurious Free Dynamic Range	SFDR	61	66		dB
Signal-to-noise plus distortion	SINAD	58	62		dB
Effective Number Of Bits	ENOB	—	10.0		Bits

1. All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2. Includes power-up of ADC and V_{REF}
3. ADC clock cycles
4. INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
5. LSB = Least Significant Bit = 0.806mV
6. Pin groups are detailed following **Table 10-1**.

Part 11 Packaging

11.1 56F8033/56F8023 Package and Pin-Out Information

This section contains package and pin-out information for the 56F8033/56F8023. This device comes in a 32-pin Low-profile Quad Flat Pack (LQFP). **Figure 11-1** shows the package outline, **Figure 11-2** shows the mechanical parameters and **Table 11-1** lists the pin-out.

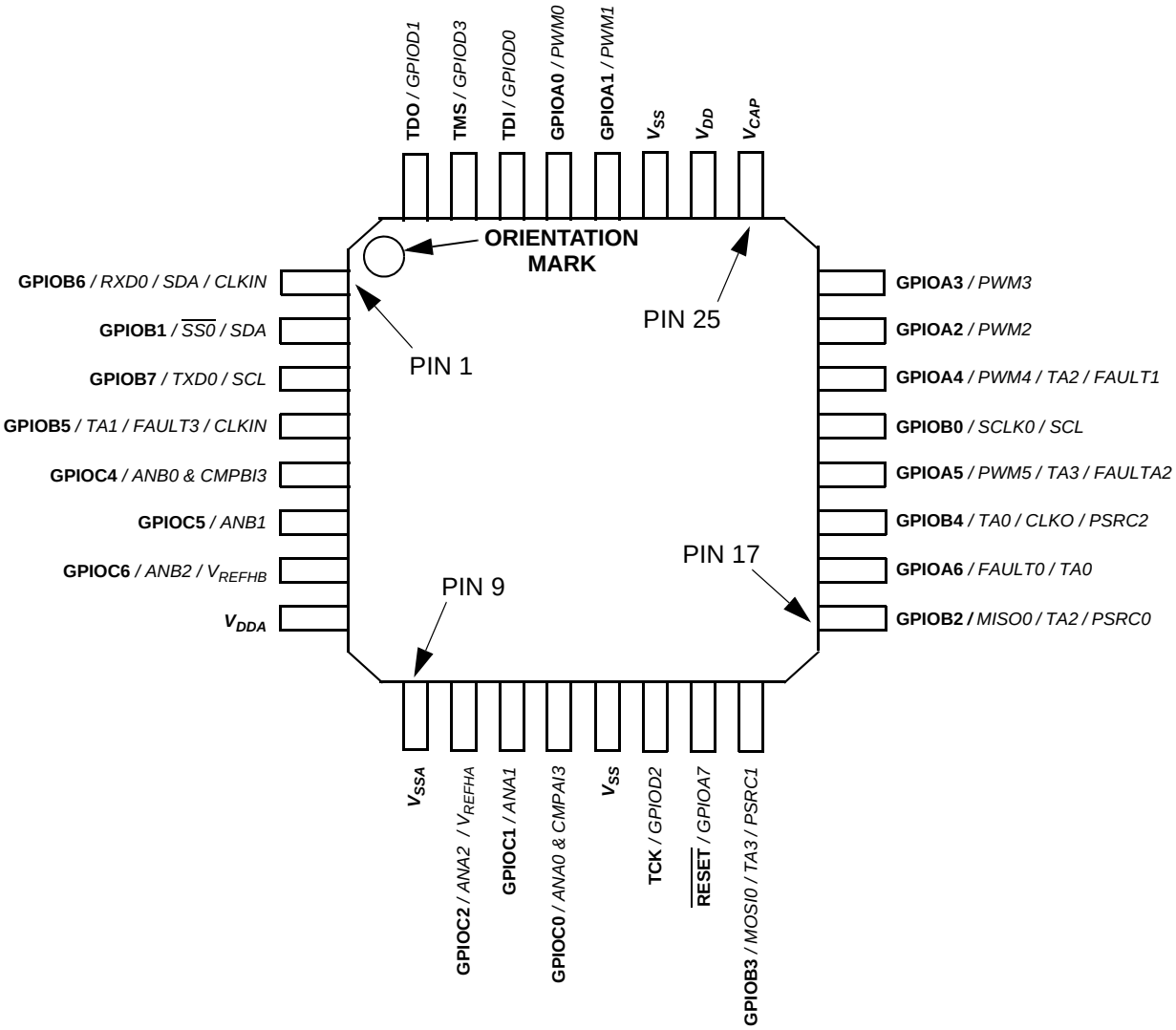

Figure 11-1 Top View, 56F8033/56F8023 32-Pin LQFP Package

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8033/56F8023:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8033/56F8023 and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible
- Bypass the V_{DD} and V_{SS} with approximately 100µF, plus the number of 0.1µF ceramic capacitors
- PCB trace lengths should be minimal for high-frequency signals
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.

Part 14 Appendix

Register acronyms are revised from previous device data sheets to provide a cleaner register description. A cross reference to legacy and revised acronyms are provided in the following table.

Note: This table comprises all peripherals used in the 56F803x and 56F802x family; some of the peripherals described here may not be present on this device.

Table 14-1 Legacy and Revised Acronyms

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Analog-to-Digital Converter (ADC) Module							
Control 1 Register	CTRL1	ADCR1	ADC_CTRL1	ADC_ADCR1	ADC_ADCR1	0xF080	
Control 2 Register	CTRL2	ADCR2	ADC_CTRL2	ADC_ADCR2	ADC_ADCR2	0xF081	
Zero Crossing Control Register	ZXCTRL	ADZCC	ADC_ZXCTRL	ADC_ADZCC	ADC_ADZCC	0xF082	
Channel List 1 Register	CLIST1	ADLST1	ADC_CLIST1	ADC_ADLST1	ADC_ADLST1	0xF083	
Channel List 2 Register	CLIST2	ADLST2	ADC_CLIST2	ADC_ADLST2	ADC_ADLST2	0xF084	
Channel List 3 Register	CLIST3		ADC_CLIST3	ADC_ADCLST3	ADC_ADCLST3	0xF085	
Channel List 4 Register	CLIST4		ADC_CLIST4	ADC_ADCLST4	ADC_ADCLST4	0xF086	
Sample Disable Register	SDIS	ADSDIS	ADC_SDIS	ADC_ADSDIS	ADC_ADSDIS	0xF087	
Status Register	STAT	ADSTAT	ADC_STAT	ADC_ADSTAT	ADC_ADSTAT	0xF088	
Conversion Ready Register	RDY		ADC_CNRDY	ADC_ADCNRDY	ADC_ADCNRDY	0xF089	
Limit Status Register	LIMSTAT	ADLSTAT	ADC_LIMSTAT	ADC_ADLSTAT	ADC_ADLSTAT	0xF08A	
Zero Crossing Status Register	ZXSTAT	ADZCSTAT	ADC_ZXSTAT	ADC_ADZCSTAT	ADC_ADZCSTAT	0xF08B	
Result 0-7 Registers	RSLT0-7	ADRSLT0-7	ADC_RSLT0-7	ADC_ADRSLT0-7	ADC_ADRSLT0-7	0xF08C	0XF093
Result 8-15 Registers	RSLT8-15		ADC_RSLT8-15	ADC_ADRSLT8-15	ADC_ADRSLT8-15	0xF094	0XF09B
Low Limit 0-7 Registers	LOLIM0-7	ADLLMT0-7	ADC_LOLIM0-7	ADC_ADLLMT0-7	ADC_ADLLMT0-7	0XF09C	0XF0A3
High Limit 0-7 Registers	HILIM0-7	ADHLMT0-7	ADC_HILIM0-7	ADC_ADHLMT0-7	ADC_ADHLMT0-7	0XF0A4	0XF0AB
Offset 0-7 Registers	OFFST0-7	ADOFS0-7	ADC_OFFST0-7	ADC_ADOFS0-7	ADC_ADOFS0-7	0XF0AC	0XF0B3
Power Control Register	PWR	ADPOWER	ADC_PWR	ADC_ADPOWER	ADC_ADPOWER	0XF0B4	
Calibration Register	CAL		ADC_CAL	ADC_ADCAL	ADC_ADCAL	0XF0B5	
Computer Operating Properly (COP) Module							
Control Register	CTRL	COPCTL	COP_CTRL	COPCTL	COPCTL	0XF120	

Table 14-1 Legacy and Revised Acronyms (Continued)

Register Name	Peripheral Reference Manual		Data Sheet		Processor Expert Acronym	Memory Address	
	New Acronym	Legacy Acronym	New Acronym	Legacy Acronym		Start	End
Pulse Width Modulator (PWM) Module							
Control Register	CTRL	PMCTL	PWM_CTRL	PWM_PMCTL	PWM_PMCTL	0xF0C0	
Fault Control Register	FCTRL	PMFCTL	PWM_FCTRL	PWM_PMFCTL	PWM_PMFCTL	0xF0C1	
Fault Status/Acknowledge Regis.	FLTACK	PMFSA	PWM_FLTACK	PWM_PMFSA	PWM_PMFSA	0xF0C2	
Output Control Register	OUT	PMOUT	PWM_OUT	PWM_PMOUT	PWM_PMOUT	0xF0C3	
Counter Register	CNTR	PMCNT	PWM_CNTR	PWM_PMCNT	PWM_PMCNT	0xF0C4	
Counter Modulo Register	CMOD	MCM	PWM_CMOD	PWM_MCM	PWM_MCM	0xF0C5	
Value 0-5 Registers	VAL0-5	PMVAL0-5	PWM_VAL0-5	PWM_PMVAL0-5	PWM_PMVAL0-5	0xF0C6	0xF0CB
Deadtime 0-1 Registers	DTIM0-1	PMDEADTM0-1	PWM_DTIM0-1	PWM_PMDEADTM0-1	PWM_PMDEADTM0-1	0xF0CC	0xF0CD
Disable Mapping 1-2 Registers	DMAP1-2	PMDISMAP1-2	PWM_DMAP1-2	PWM_PMDISMAP1-2	PWM_PMDISMAP1-2	0xF0CE	0xF0CF
Configure Register	CNFG	PMCFG	PWM_CNFG	PWM_PMCFG	PWM_PMCFG	0xF0D0	
Channel Control Register	CCTRL	PMCCR	PWM_CCTRL	PWM_PMCCR	PWM_PMCCR	0xF0D1	
Port Register	PORT	PMPORT	PWM_PORT	PWM_PMPORT	PWM_PMPORT	0xF0D2	
Internal Correction Control Register	ICCTRL	PMICCR	PWM_ICCTRL	PWM_PMICCR	PWM_PMICCR	0xF0D3	
Source Control Register	SCTRL	PMSRC	PWM_SCTRL	PWM_PMSRC	PWM_PMSRC	0xF0D4	
Synchronization Window Register	SYNC		PWM_SYNC	PWM_SYNC	PWM_SYNC	0xF0D5	
Fault Filter 0-3 Register	FFILT0-3		PWM_FFILT0-3	PWM_FFILT0-3	PWM_FFILT0-3	0xF0D6	0xF0D9
Multi-Scalable Controller Area Network (MSCAN) Module							
Control 0 Register	CTRL0		CAN_CTRL0		CANCTRL0	0XF800	
Control 1 Register	CTRL1		CAN_CTRL1		CANCTRL1	0XF801	
Bus Timing 0 Register	BTR0		CAN_BTR0		CANBTR0	0XF802	
Bus Timing 1 Register	BTR1		CAN_BTR1		CANBTR1	0XF803	
Receive Flag Register	RFLG		CAN_RFLG		CANRFLG	0XF804	
Receiver Interrupt Enable Register	RIER		CAN_RIER		CANRIER	0XF805	
Transmitter Flag Register	TFLG		CAN_TFLG		CANTFLG	0XF806	
Transmitter Interrupt Enable Register.	TIER		CAN_TIER		CANTIER	0XF807	
Transmitter Msg Abort Request Register	TARQ		CAN_TARQ		CANTARQ	0XF808	