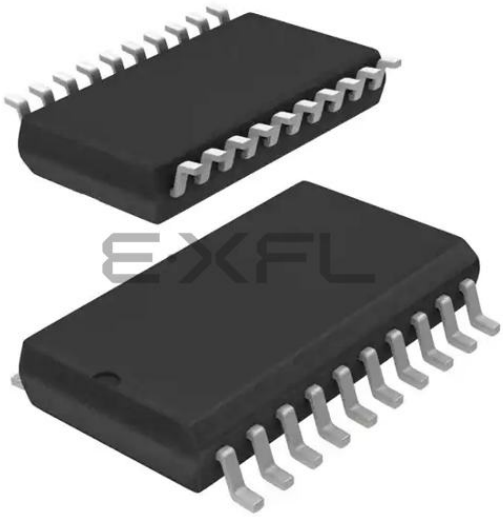

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe4cwj

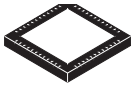
Freescale Semiconductor
Data Sheet: Technical Data
An Energy Efficient Solution by Freescale

Document Number: MC9S08QE8
Rev. 8, 4/2011

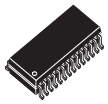
MC9S08QE8 Series

Covers: MC9S08QE8 and MC9S08QE4

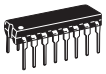
MC9S08QE8

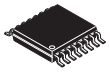

32-Pin QFN
Case 2078-01


32-Pin LQFP
Case 873A


28-Pin SOIC
751F-05


20-Pin SOIC
751D-07


16-Pin PDIP
648


16-Pin TSSOP
948F

Features

- 8-Bit HCS08 Central Processor Unit (CPU)
  - Up to 20 MHz CPU at 3.6 V to 1.8 V across temperature range of –40 °C to 85 °C
  - HC08 instruction set with added BGND instruction
  - Support for up to 32 interrupt/reset sources
- On-Chip Memory
  - Flash read/program/erase over full operating voltage and temperature
  - Random-access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Two low power stop modes
  - Reduced power wait mode
  - Low power run and wait modes allow peripherals to run while voltage regulator is in standby
  - Peripheral clock gating register can disable clocks to unused modules, thereby reducing currents
  - Very low power external oscillator that can be used in stop2 or stop3 modes to provide accurate clock source to real time counter
  - 6 µs typical wake-up time from stop3 mode
- Clock Source Options
  - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation over temperature and voltage; supporting bus frequencies from 1 MHz to 10 MHz
- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low-voltage warning with interrupt
  - Low-voltage detection with reset or interrupt
  - Illegal opcode detection with reset
  - Illegal address detection with reset
  - Flash block protection
- Development Support
  - Single-wire background debug interface
  - Breakpoint capability to allow single breakpoint setting during in-circuit debugging (plus two more breakpoints in on-chip debug module)
  - On-chip in-circuit emulator (ICE) debug module containing two comparators and nine trigger modes; eight deep FIFO for storing change-of-flow addresses and event-only data; debug module supports both tag and force breakpoints
- Peripherals
  - **ADC** — 10-channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
  - **ACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
  - **SCI** — Full-duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake-up on active edge
  - **SPI** — Full-duplex or single-wire bidirectional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - **IIC** — Up to 100 kbps with maximum bus loading; multi-master operation; programmable slave address; interrupt driven byte-by-byte data transfer; supporting broadcast mode and 10-bit addressing
  - **TPMx** — Two 3-channel (TPM1 and TPM2); selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - **RTC** — (Real-time counter) 8-bit modulus counter with binary or decimal based prescaler; external clock source for precise time base, time-of-day, calendar or task scheduling functions; free running on-chip low power oscillator (1 kHz) for cyclic wakeup without external components; runs in all MCU modes
- Input/Output
  - 26 GPIOs, one output-only pin and one input-only pin
  - Eight KBI interrupts with selectable polarity
  - Hysteresis and configurable pullup device on all input pins; configurable slew rate and drive strength on all output pins.
- Package Options
  - 32-pin LQFP, 32-pin QFN, 28-pin SOIC, 20-pin SOIC, 16-pin PDIP, 16-pin TSSOP

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

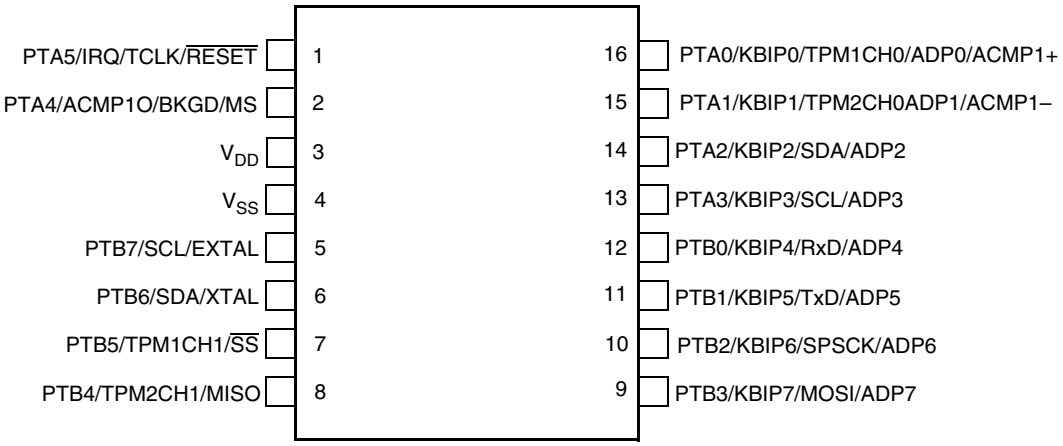


Figure 5. MC9S08QE8 Series in 16-pin PDIP and TSSOP Packages

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	—	—	—	PTD1				
2	—	—	—	PTD0				
3	5	3	3					V_{DD}
4	6	—	—					V_{DDA}/V_{REFH}
5	7	—	—					V_{SSA}/V_{REFL}
6	8	4	4					V_{SS}
7	9	5	5	PTB7	SCL[1]			EXTAL
8	10	6	6	PTB6	SDA[1]			XTAL
9	11	7	7	PTB5	TPM1CH1	$\overline{SS}$		
10	12	8	8	PTB4	TPM2CH1	MISO		
11	13	9	—	PTC3				
12	14	10	—	PTC2				
13	15	11	—	PTC1	TPM2CH2[2]			
14	16	12	—	PTC0	TPM1CH2[3]			
15	17	13	9	PTB3	KBIP7	MOSI	ADP7	
16	18	14	10	PTB2	KBIP6	SPSCK	ADP6	
17	19	15	11	PTB1	KBIP5	TxD	ADP5	
18	20	16	12	PTB0	KBIP4	RxD	ADP4	
19	21	—	—	PTA7	TPM2CH2[2]		ADP9	
20	22	—	—	PTA6	TPM1CH2[3]		ADP8	
21	—	—	—	PTD3				
22	—	—	—	PTD2				
23	23	17	13	PTA3	KBIP3	SCL[1]	ADP3	
24	24	18	14	PTA2	KBIP2	SDA[1]	ADP2	
25	25	19	15	PTA1	KBIP1	TPM2CH0	ADP1[4]	ACMP1–[4]

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
26	26	20	16	PTA0	KBIP0	TPM1CH0	ADP0[4]	ACMP1+[4]
27	27	—	—	PTC7				ACMP2–
28	28	—	—	PTC6				ACMP2+
29	1	—	—	PTC5				ACMP2O
30	2	—	—	PTC4				
31	3	1	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$	
32	4	2	2	PTA4	ACMP1O	BKGD	MS	

1 IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2, default reset locations are PTA3 and PTA2.

2 TPM2CH2 pin can be repositioned using TPM2CH2PS in SOPT2, default reset location is PTA7.

3 TPM1CH2 pin can be repositioned using TPM1CH2PS in SOPT2, default reset location is PTA6.

4 If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
1		Operating voltage V_{DD} rising V_{DD} falling				2.0[2] 1.8		3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	V_{DD} > 1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	C				V_{DD} > 1.8V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	V_{DD} > 1.8 V, I_{Load} = 0.6 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		V_{DD} > 2.7 V, I_{Load} = 10 mA	—	—	0.5	
	C				V_{DD} > 1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	All digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 × V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 × V_{DD}	—	—	
7	P	Input low voltage	All digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 × V_{DD}	
	C				V_{DD} > 1.8 V	—	—	0.30 × V_{DD}	
8	C	Input hysteresis	All digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	All input only pins (per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	1	µA
10	P	Hi-Z (off-state) leakage current	All input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	1	µA
11	P	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	$\lvert I_{OZTOT} \rvert$	V_{In} = V_{DD} or V_{SS}	—	—	2	µA
12a	P	Pullup, pulldown resistors	All digital inputs, when enabled (all I/O pins other than PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD}	—	17.5	—	52.5	kΩ

Table 7. DC Characteristics (continued)

Num	C	Characteristic		Symbol	Condition	Min.	Typical[1]	Max.	Unit
12b	C	Pullup, pulldown resistors	(PTA5/IRQ/TCLK/$\overline{\text{RESET}}$)	R_{PU}, R_{PD} (Note[3])	—	17.5	—	52.5	kΩ
13	C	DC injection current [4, 5, 6]	Single pin limit	I_{IC}	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
14	C	Input capacitance, all pins		C_{In}	—	—	—	8	pF
15	C	RAM retention voltage		V_{RAM}	—	—	0.6	1.0	V
16	C	POR re-arm voltage[7]		V_{POR}	—	0.9	1.4	2.0	V
17	D	POR re-arm time		t_{POR}	—	10	—	—	µs
18	P	Low-voltage detection threshold		V_{LVD}	V_{DD} falling V_{DD} rising	1.80 1.88	1.84 1.92	1.88 1.96	V
19	P	Low-voltage warning threshold		V_{LVW}	V_{DD} falling V_{DD} rising	2.08	2.14	2.24	V
20	P	Low-voltage inhibit reset/recover hysteresis		V_{hys}	—	—	80	—	mV
21	P	Bandgap voltage reference[8]		V_{BG}	—	1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 The specified resistor value is the actual value internal to the device. The pullup or pulldown value may appear higher when measured externally on the pin.

4 All functional non-supply pins, except for PTA5 are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 Maximum is highest voltage that POR is guaranteed.

8 Factory trimmed at V_{DD} = 3.0 V, Temp = 25 °C

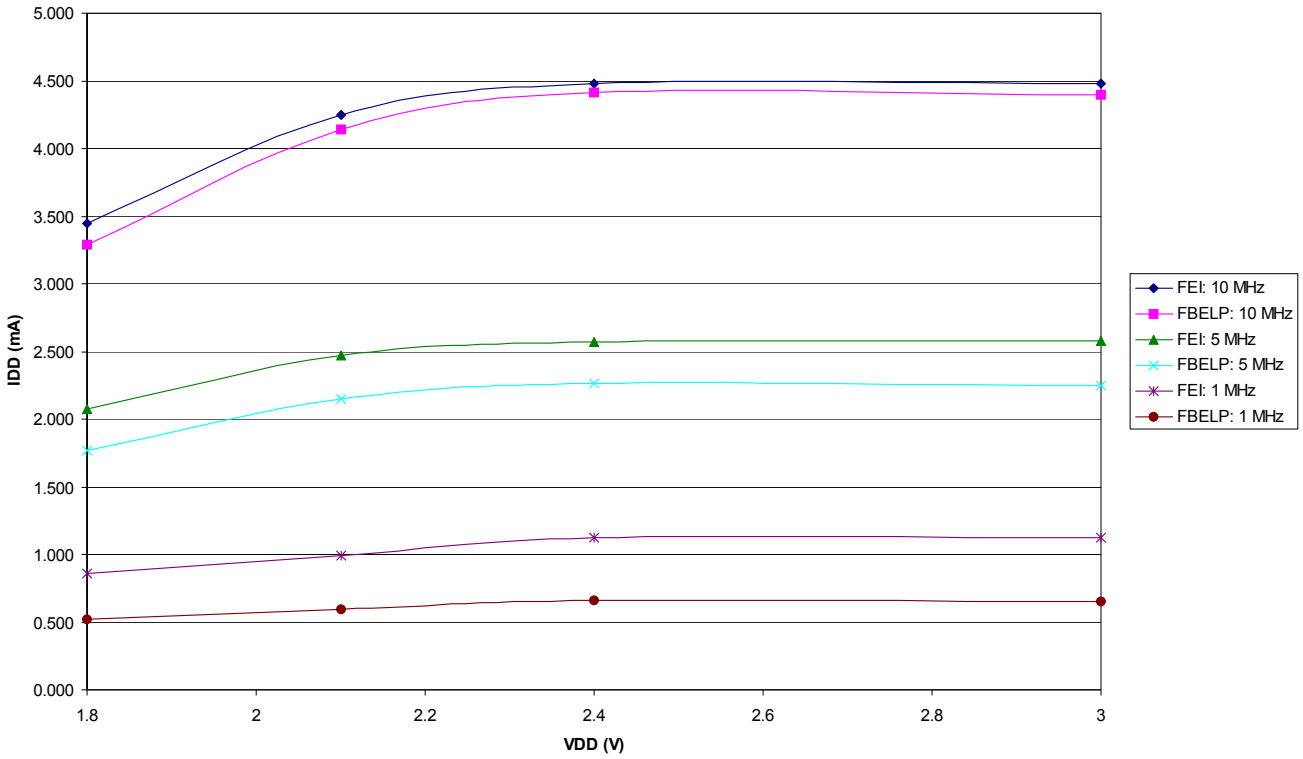


Figure 11. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ADC off, All Other Modules Enabled)

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

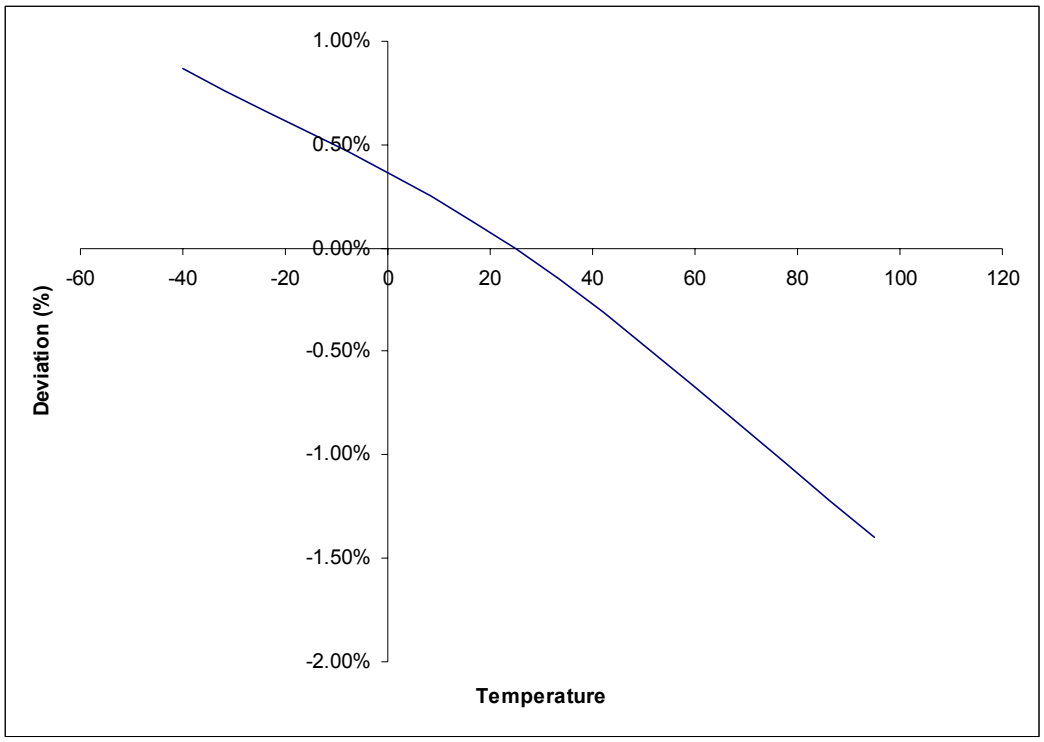


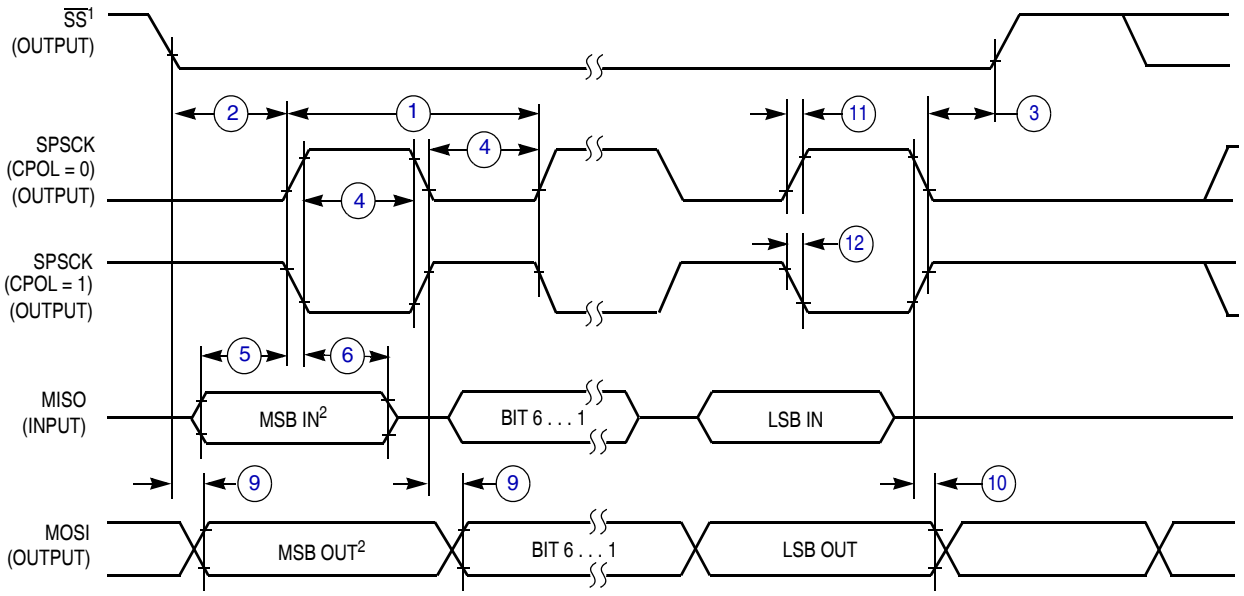
Figure 14. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10.3 SPI Timing

Table 14 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

Table 14. SPI Timing

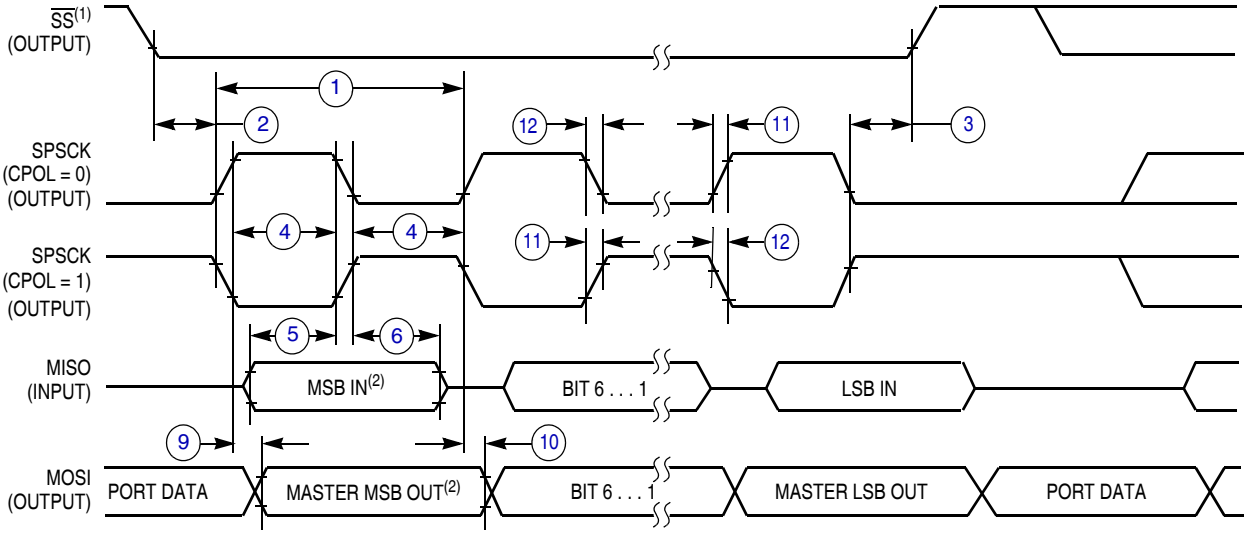
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	15 15	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	0 25	— —	ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	— —	25 25	ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	0 0	— —	ns ns
11	D	Rise time Input Output	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns ns
12	D	Fall time Input Output	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. SPI Master Timing (CPHA =1)

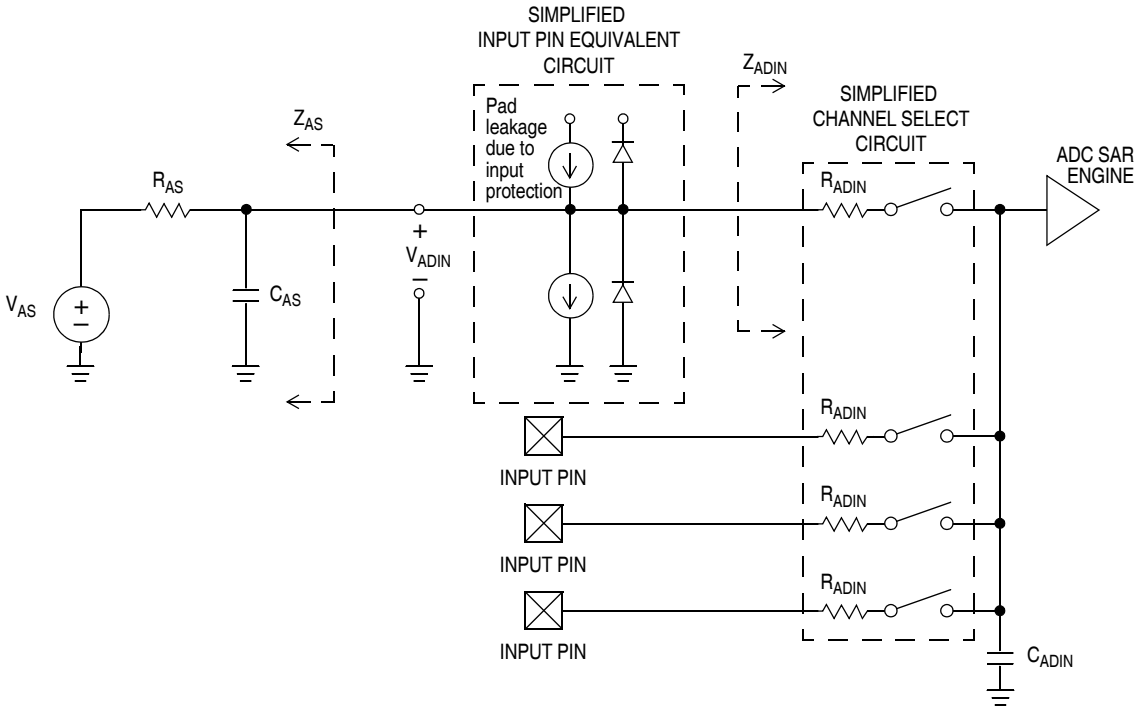


Figure 23. ADC Input Impedance Equivalency Diagram

Table 17. ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
T	Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		I_{DDA}	—	120	—	μA	
T	Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		I_{DDA}	—	202	—	μA	
T	Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		I_{DDA}	—	288	—	μA	
P	Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		I_{DDA}	—	0.532	1	mA	
P	ADC asynchronous clock source	High speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
		Low power (ADLPC = 1)		1.25	2	3.3		

3.14.1 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 19.

Table 19. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Result	Amplitude[1] (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 3.3 V T_A = 25 °C package type 32-pin LQFP	8 MHz crystal 8 MHz bus	A	2.3	kV
				B	4.0	
				C	>4.0	
				D	>4.0	

1 Data based on qualification test results. Not tested in production.

The susceptibility performance classification is described in Table 20.

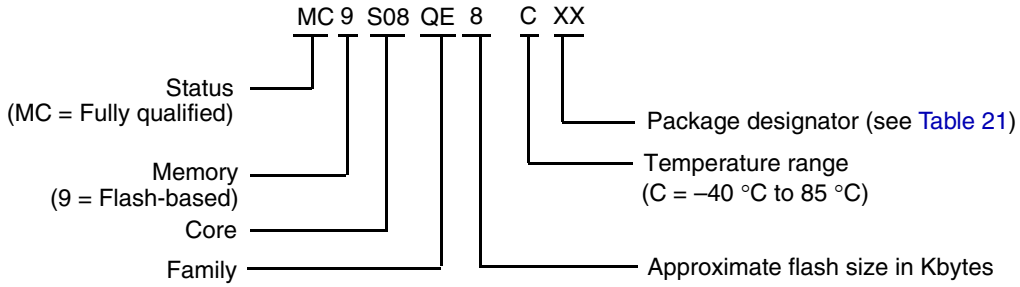
Table 20. Susceptibility Performance Classification

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the $\overline{\text{RESET}}$ pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



5 Package Information

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
32	Quad Flat No-Leads	QFN	FM	2078	98ASA00071D
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
20	Small Outline Integrated Circuit	SOIC	WJ	751D	98ASB42343B
16	Plastic Dual In-line Package	PDIP	PG	648	98ASB42431B
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

5.1 Mechanical Drawings

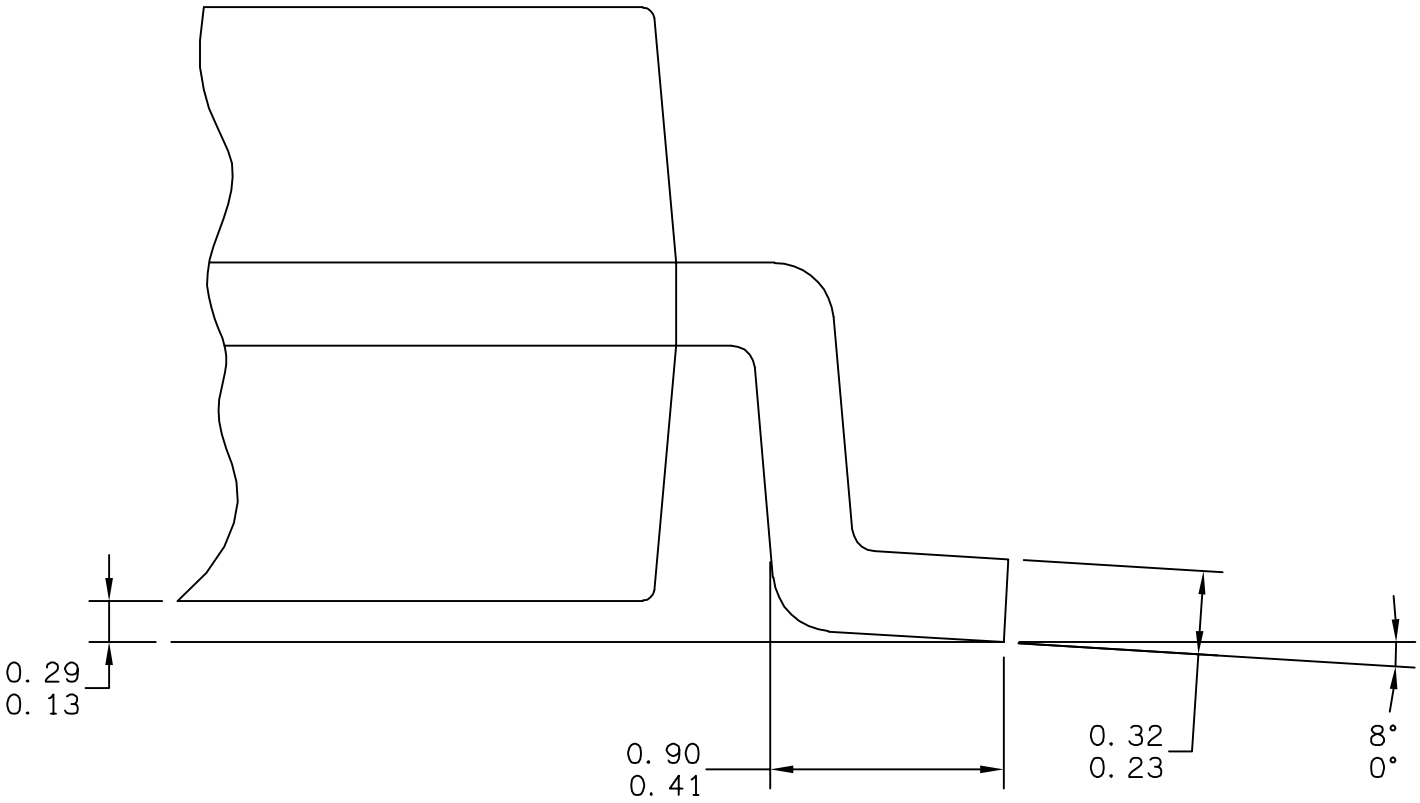
The following pages are mechanical drawings for the packages described in Table 21.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.2MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.4 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ASA00071D	REV: O
	CASE NUMBER: 2078–01	14 APR 2009
	STANDARD: NON–JEDEC	



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F-05	10 MAR 2005
	STANDARD: MS-013AE	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

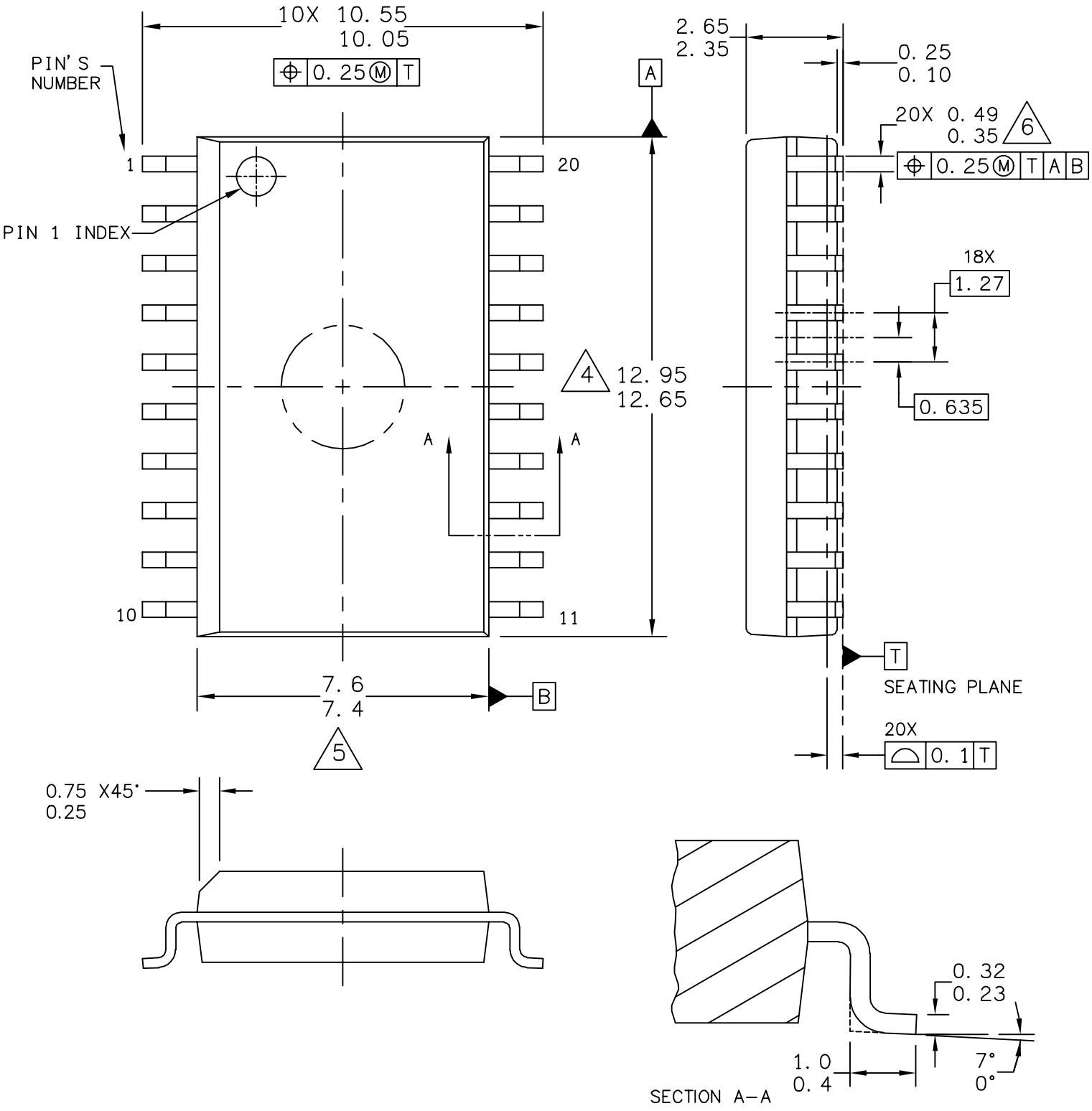
3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05

5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	



MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42343B	REV: J
20LD SOIC W/B, 1.27 PITCH, CASE OUTLINE	CASE NUMBER: 751D–07	23 MAR 2005
	STANDARD: JEDEC MS–013AC	