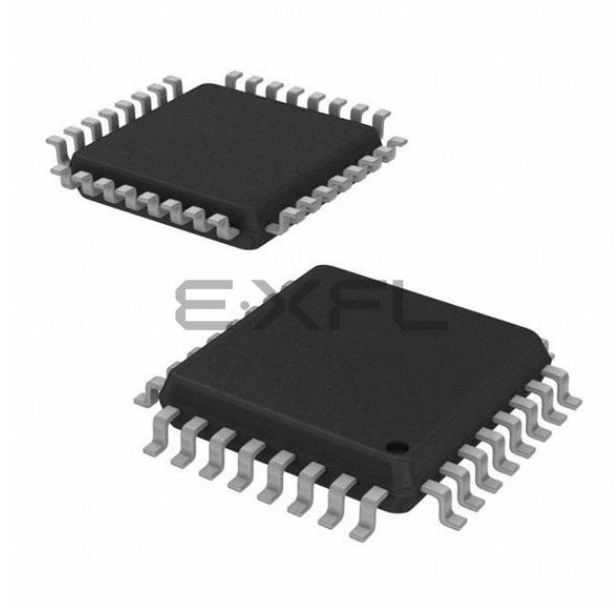

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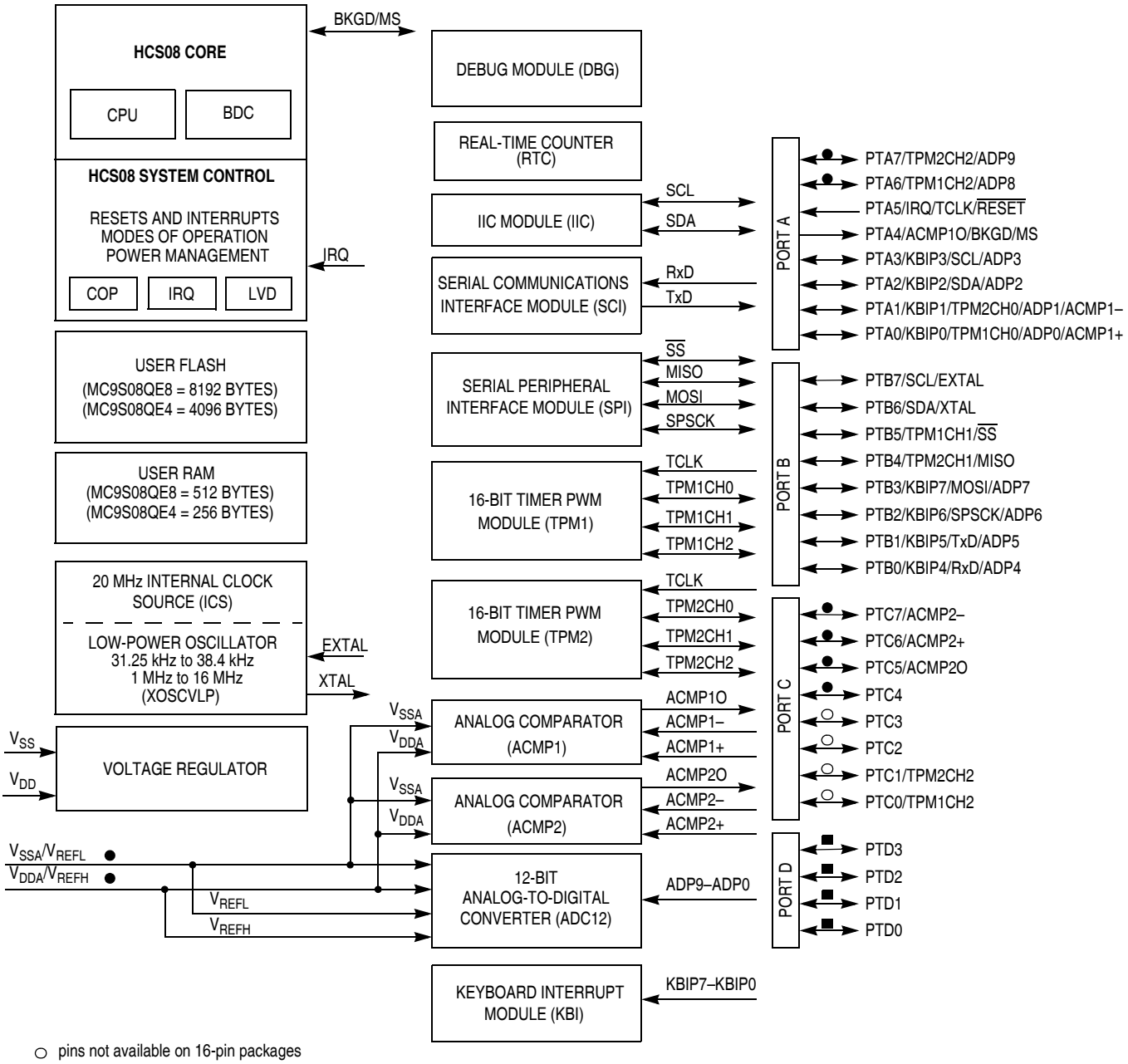
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08qe8clc

1 MCU Block Diagram

The block diagram, Figure 1, shows the structure of MC9S08QE8 series MCU.



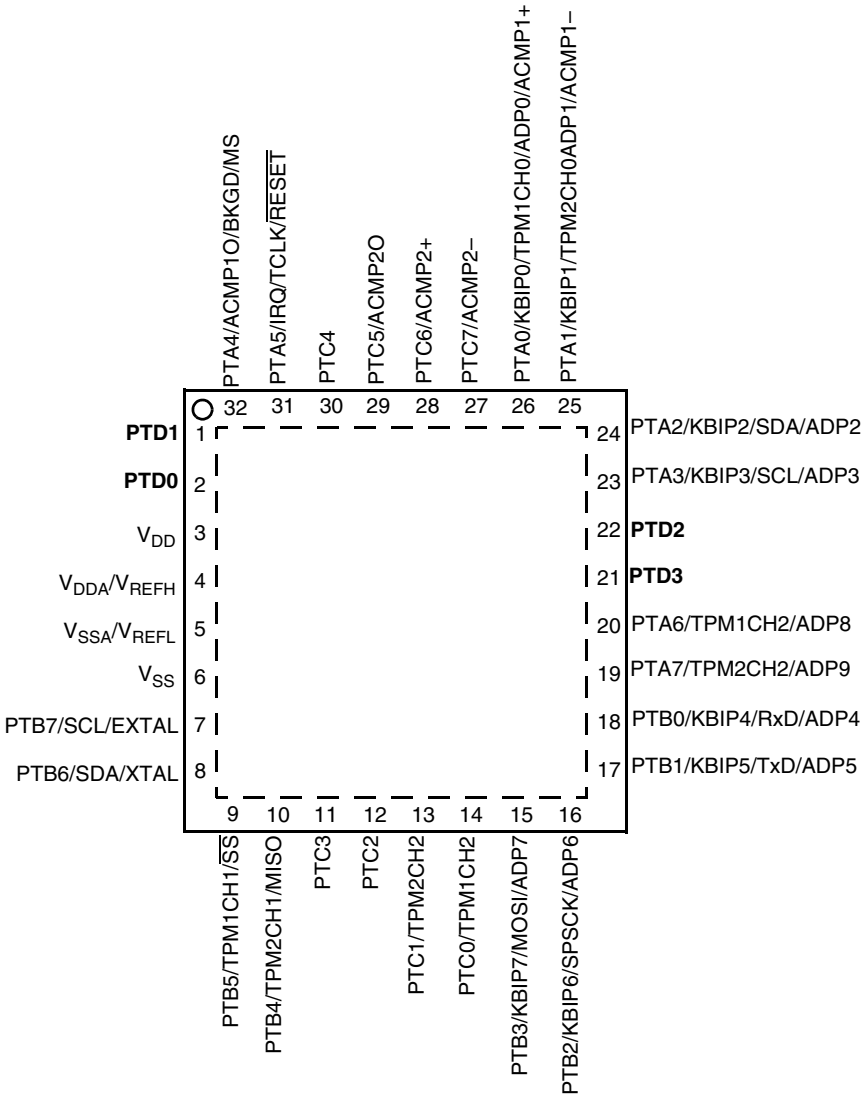
○ pins not available on 16-pin packages
● pins not available on 16-pin or 20-pin packages
■ pins not available on 16-pin, 20-pin or 28-pin packages

Notes: When PTA5 is configured as $\overline{\text{RESET}}$, pin becomes bi-directional with output being open-drain drive containing an internal pullup device.
When PTA4 is configured as BKGD, pin becomes bi-directional.
For the 16-pin and 20-pin packages, V_{SSA}/V_{REFL} and V_{DDA}/V_{REFH} are double bonded to V_{SS} and V_{DD} respectively.

Figure 1. MC9S08QE8 Series Block Diagram

2 Pin Assignments

This section shows the pin assignments for the MC9S08QE8 series devices.



Pins shown in bold type are lost in the next lower pin count package.

Figure 2. MC9S08QE8 Series in 32-Pin LQFP/QFN Package

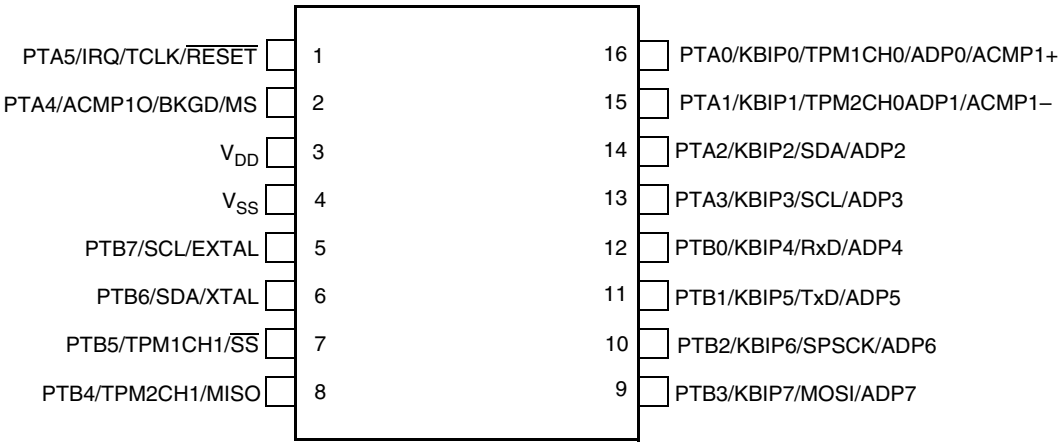


Figure 5. MC9S08QE8 Series in 16-pin PDIP and TSSOP Packages

Table 1. Pin Availability by Package Pin-Count

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	—	—	—	PTD1				
2	—	—	—	PTD0				
3	5	3	3					V_{DD}
4	6	—	—					V_{DDA}/V_{REFH}
5	7	—	—					V_{SSA}/V_{REFL}
6	8	4	4					V_{SS}
7	9	5	5	PTB7	SCL[1]			EXTAL
8	10	6	6	PTB6	SDA[1]			XTAL
9	11	7	7	PTB5	TPM1CH1	$\overline{SS}$		
10	12	8	8	PTB4	TPM2CH1	MISO		
11	13	9	—	PTC3				
12	14	10	—	PTC2				
13	15	11	—	PTC1	TPM2CH2[2]			
14	16	12	—	PTC0	TPM1CH2[3]			
15	17	13	9	PTB3	KBIP7	MOSI	ADP7	
16	18	14	10	PTB2	KBIP6	SPSCK	ADP6	
17	19	15	11	PTB1	KBIP5	TxD	ADP5	
18	20	16	12	PTB0	KBIP4	RxD	ADP4	
19	21	—	—	PTA7	TPM2CH2[2]		ADP9	
20	22	—	—	PTA6	TPM1CH2[3]		ADP8	
21	—	—	—	PTD3				
22	—	—	—	PTD2				
23	23	17	13	PTA3	KBIP3	SCL[1]	ADP3	
24	24	18	14	PTA2	KBIP2	SDA[1]	ADP2	
25	25	19	15	PTA1	KBIP1	TPM2CH0	ADP1[4]	ACMP1–[4]

Table 1. Pin Availability by Package Pin-Count (continued)

Pin Number				<-- Lowest **Priority** --> Highest				
32	**28**	**20**	**16**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
26	26	20	16	PTA0	KBIP0	TPM1CH0	ADP0[4]	ACMP1+[4]
27	27	—	—	PTC7				ACMP2–
28	28	—	—	PTC6				ACMP2+
29	1	—	—	PTC5				ACMP2O
30	2	—	—	PTC4				
31	3	1	1	PTA5	IRQ	TCLK	$\overline{\text{RESET}}$	
32	4	2	2	PTA4	ACMP1O	BKGD	MS	

1 IIC pins, SCL and SDA can be repositioned using IICPS in SOPT2, default reset locations are PTA3 and PTA2.

2 TPM2CH2 pin can be repositioned using TPM2CH2PS in SOPT2, default reset location is PTA7.

3 TPM1CH2 pin can be repositioned using TPM1CH2PS in SOPT2, default reset location is PTA6.

4 If ADC and ACMP1 are enabled, both modules will have access to the pin.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08QE8 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions must be taken to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification, ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless instructed otherwise in the device specification.

Table 5. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 6. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	±2000	—	V
2	Machine model (MM)	V_{MM}	±200	—	V
3	Charge device model (CDM)	V_{CDM}	±500	—	V
4	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

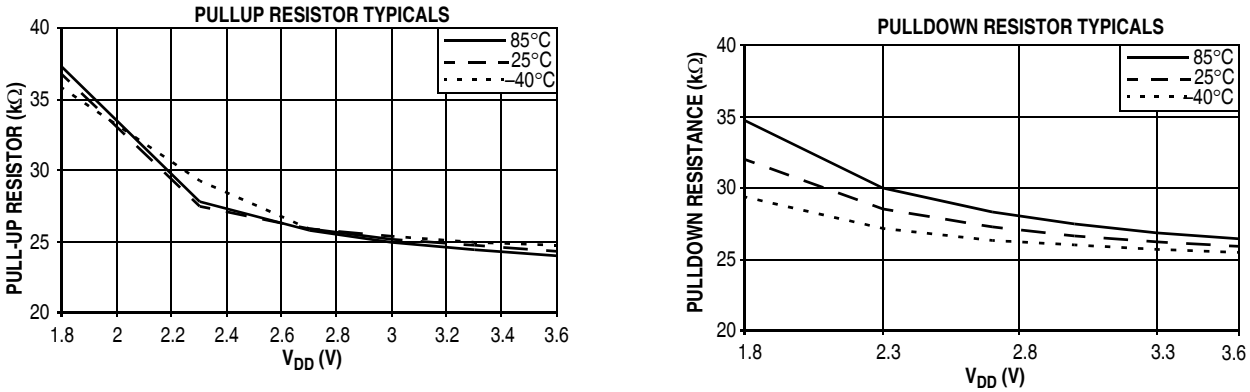


Figure 6. Pullup and Pulldown Typical Resistor Values (V_{DD} = 3.0 V)

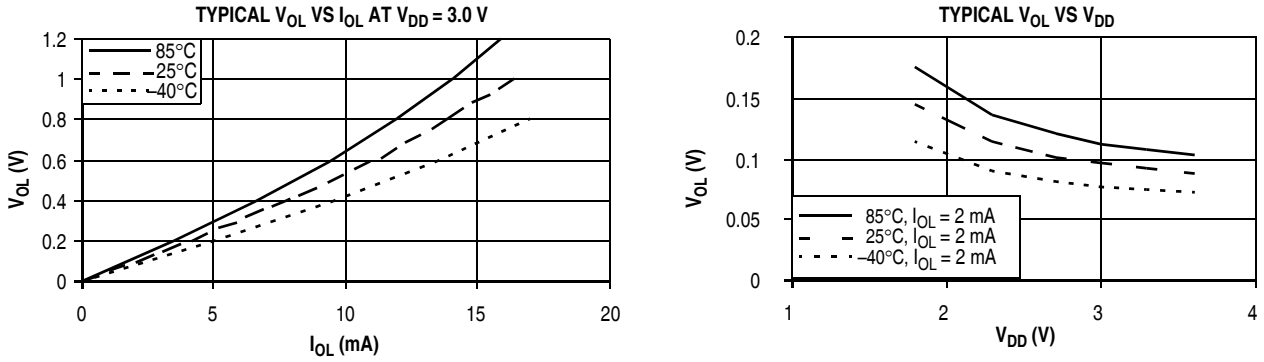


Figure 7. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

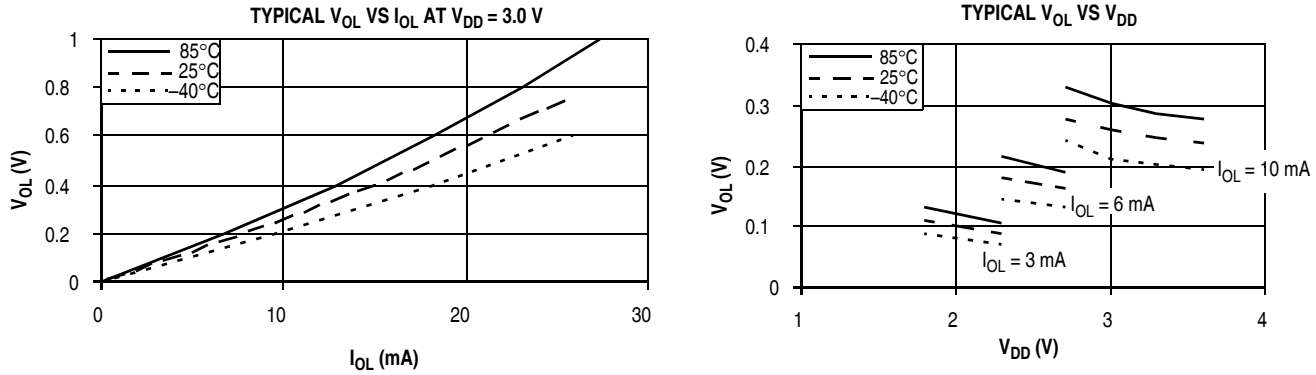


Figure 8. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

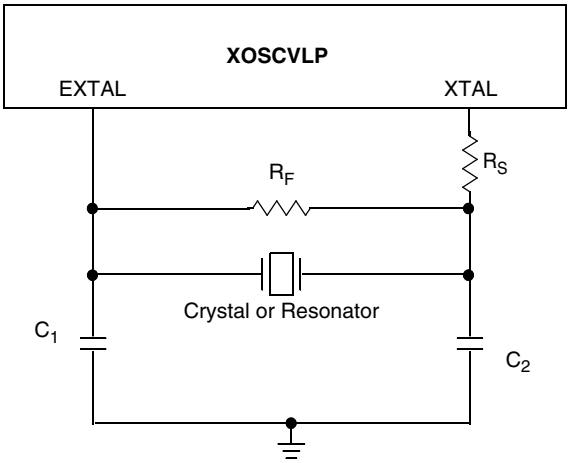


Figure 12. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

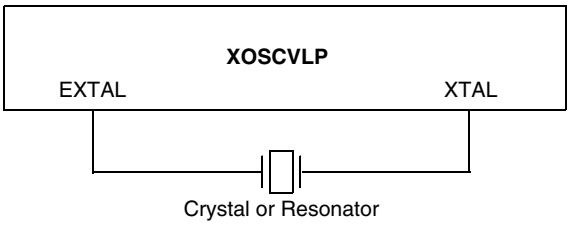


Figure 13. Typical Crystal or Resonator Circuit: Low Range/Low Power

3.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C	f_{int_t}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed	f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time	t_{IRST}	—	5	10	µs
4	P	DCO output frequency range — trimmed[2] Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	f_{dco_DMX32}	—	19.92	—	MHz
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$

Table 11. ICS Frequency Specifications (Temperature Range = –40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min.	Typical[1]	Max.	Unit
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
8	C	Total deviation of DCO output from trimmed frequency[3] Over full voltage and temperature range Over fixed voltage and temperature range of 0 to 70 °C	Δf_{dco_t}	—	–1.0 to 0.5 ±0.5	± 2 ± 1	$\%f_{dco}$
10	C	FLL acquisition time[4]	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval)[5]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

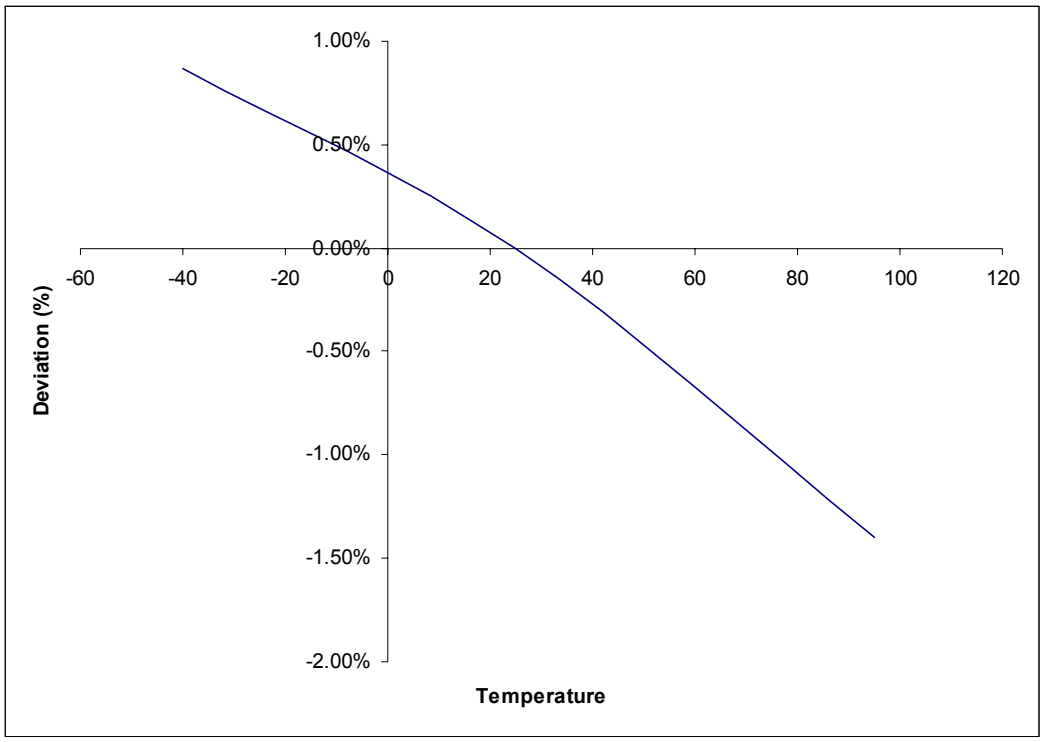


Figure 14. Deviation of DCO Output from Trimmed Frequency (20 MHz, 3.0 V)

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 12. Control Timing

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	10	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 × t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 1.5 × t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 16 23	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 5 9	 — —	ns
10	C	Voltage regulator recovery time	t_{VRR}	—	4	—	µs

1 Typical values are based on characterization data at V_{DD} = 3.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

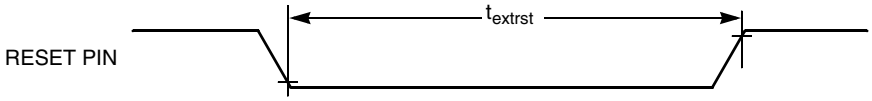


Figure 15. Reset Timing

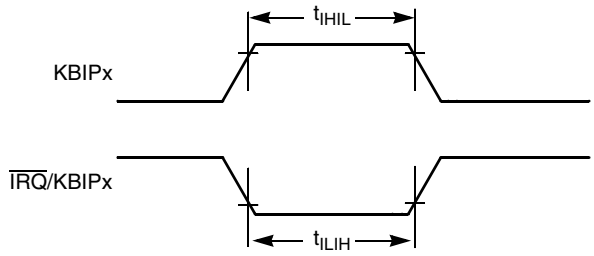


Figure 16. IRQ/KBIPx Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 13. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

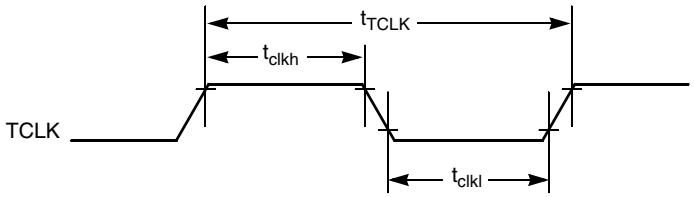


Figure 17. Timer External Clock

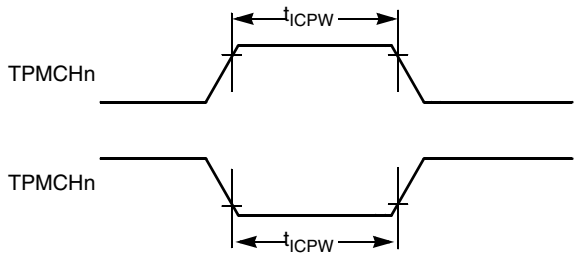
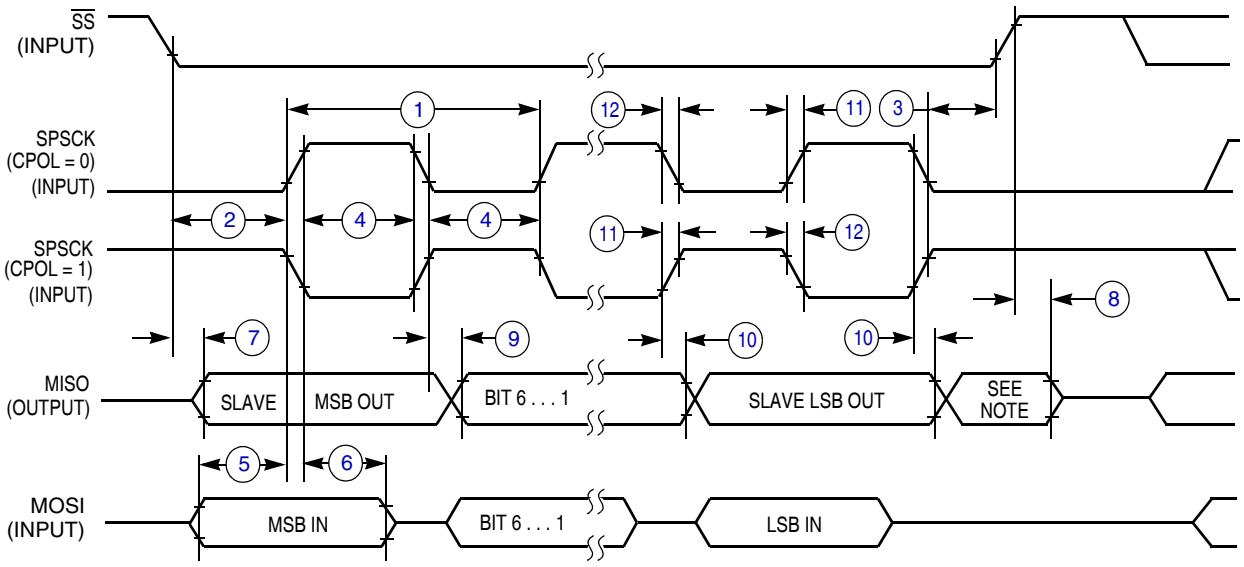


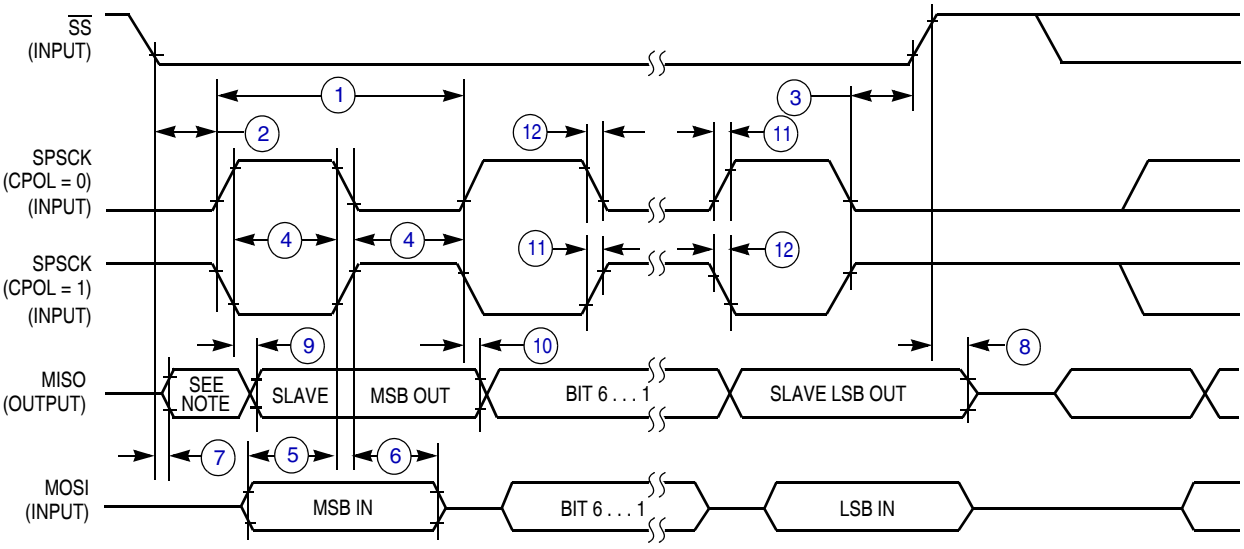
Figure 18. Timer Input Capture Pulse



NOTE:

1. Not defined but normally MSB of character just received

Figure 21. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 22. SPI Slave Timing (CPHA = 1)

3.11 Analog Comparator (ACMP) Electricals

Table 15. Analog Comparator Electrical Specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DD}	1.8	—	3.6	V
P	Supply current (active)	I_{DDAC}	—	20	35	µA

Table 17. ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
P	Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See QE8 reference manual for conversion time variances
		Long sample (ADLSMP = 1)		—	40	—		
P	Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
		Long sample (ADLSMP = 1)		—	23.5	—		
D	Temp sensor slope	–40 °C– 25 °C	m	—	1.646	—	mV/°C	
		25 °C– 85 °C		—	1.769	—		
D	Temp sensor voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	
Characteristics for devices with dedicated analog supply (28- and 32-pin packages only)								
T	Total unadjusted error	12-bit mode, 3.6> V_{DDA} > 2.7	E_{TUE}	—	–1 to 3	–2.5 to 5.5	LSB[2]	Includes quantization
T		12-bit mode, 2.7> V_{DDA} > 1.8V		—	–1 to 3	–3.0 to 6.5		
P		10-bit mode		—	±1	±2.5		
P		8-bit mode		—	±0.5	±1.0		
T	Differential non-linearity	12-bit mode	DNL	—	±1.0	–1.5 to 2.0	LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	—	±1.5	–2.5 to 2.75	LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	—	±1.5	±2.5	LSB[2]	V_{ADIN} = V_{SSA}
P		10-bit mode		—	±0.5	±1.5		
P		8-bit mode		—	±0.5	±0.5		
T	Full-scale error	12-bit mode	E_{FS}	—	±1.0	–3.5 to 1.0	LSB[2]	V_{ADIN} = V_{DDA}
P		10-bit mode		—	±0.5	±1		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		

Table 17. ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

C	Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
D	Input leakage error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		
Characteristics for devices with shared supply (16- and 20-pin packages only)								
T	Total unadjusted error	12-bit mode	E_{TUE}	Not recommended usage			LSB[2]	Includes quantization
P		10-bit mode		—	±1.5	±3.5		
P		8-bit mode		—	±0.7	±1.5		
T	Differential non-linearity	12-bit mode	DNL	Not recommended usage			LSB[2]	
P		10-bit mode[3]		—	±0.5	±1.0		
P		8-bit mode[3]		—	±0.3	±0.5		
T	Integral non-linearity	12-bit mode	INL	Not recommended usage			LSB[2]	
T		10-bit mode		—	±0.5	±1.0		
T		8-bit mode		—	±0.3	±0.5		
T	Zero-scale error	12-bit mode	E_{ZS}	Not recommended usage			LSB[2]	V_{ADIN} = V_{SSA}
P		10-bit mode		—	±1.5	±2.1		
P		8-bit mode		—	±0.5	±0.7		
T	Full-scale error	12-bit mode	E_{FS}	Not recommended usage			LSB[2]	V_{ADIN} = V_{DDA}
P		10-bit mode		—	±1	±1.5		
P		8-bit mode		—	±0.5	±0.5		
D	Quantization error	12-bit mode	E_Q	Not recommended usage			LSB[2]	
		10-bit mode		—	—	±0.5		
		8-bit mode		—	—	±0.5		
D	Input leakage error	12-bit mode	E_{IL}	Not recommended usage			LSB[2]	Pad leakage[4] * R_{AS}
		10-bit mode		—	±0.2	±4		
		8-bit mode		—	±0.1	±1.2		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
P	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
P	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
	Byte program current[3]	RI_{DDBP}	—	4	—	mA
	Page erase current[3]	RI_{DDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.14.1 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 19.

Table 19. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Result	Amplitude[1] (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 3.3 V T_A = 25 °C package type 32-pin LQFP	8 MHz crystal 8 MHz bus	A	2.3	kV
				B	4.0	
				C	>4.0	
				D	>4.0	

1 Data based on qualification test results. Not tested in production.

The susceptibility performance classification is described in Table 20.

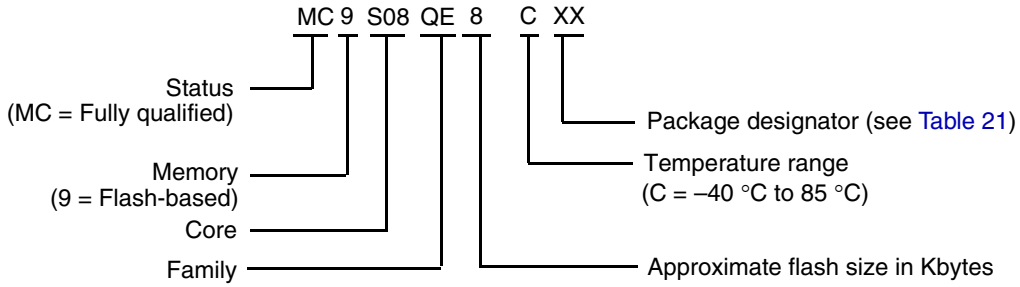
Table 20. Susceptibility Performance Classification

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the $\overline{\text{RESET}}$ pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

4 Ordering Information

This section contains ordering information for the device numbering system.

Example of the device numbering system:



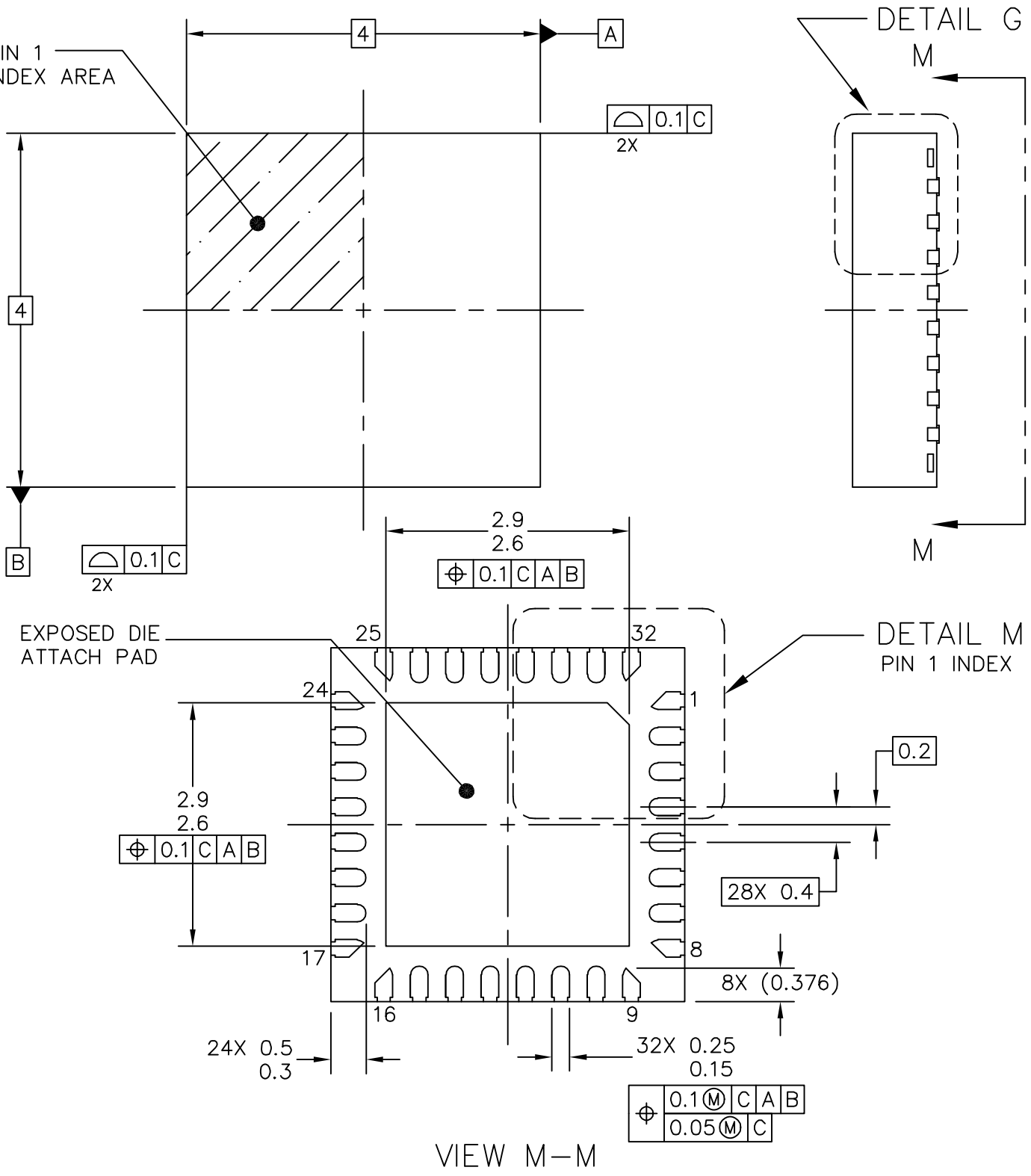
5 Package Information

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
32	Quad Flat No-Leads	QFN	FM	2078	98ASA00071D
32	Low Quad Flat Package	LQFP	LC	873A	98ASH70029A
28	Small Outline Integrated Circuit	SOIC	WL	751F	98ASB42345B
20	Small Outline Integrated Circuit	SOIC	WJ	751D	98ASB42343B
16	Plastic Dual In-line Package	PDIP	PG	648	98ASB42431B
16	Thin Shrink Small Outline Package	TSSOP	TG	948F	98ASH70247A

5.1 Mechanical Drawings

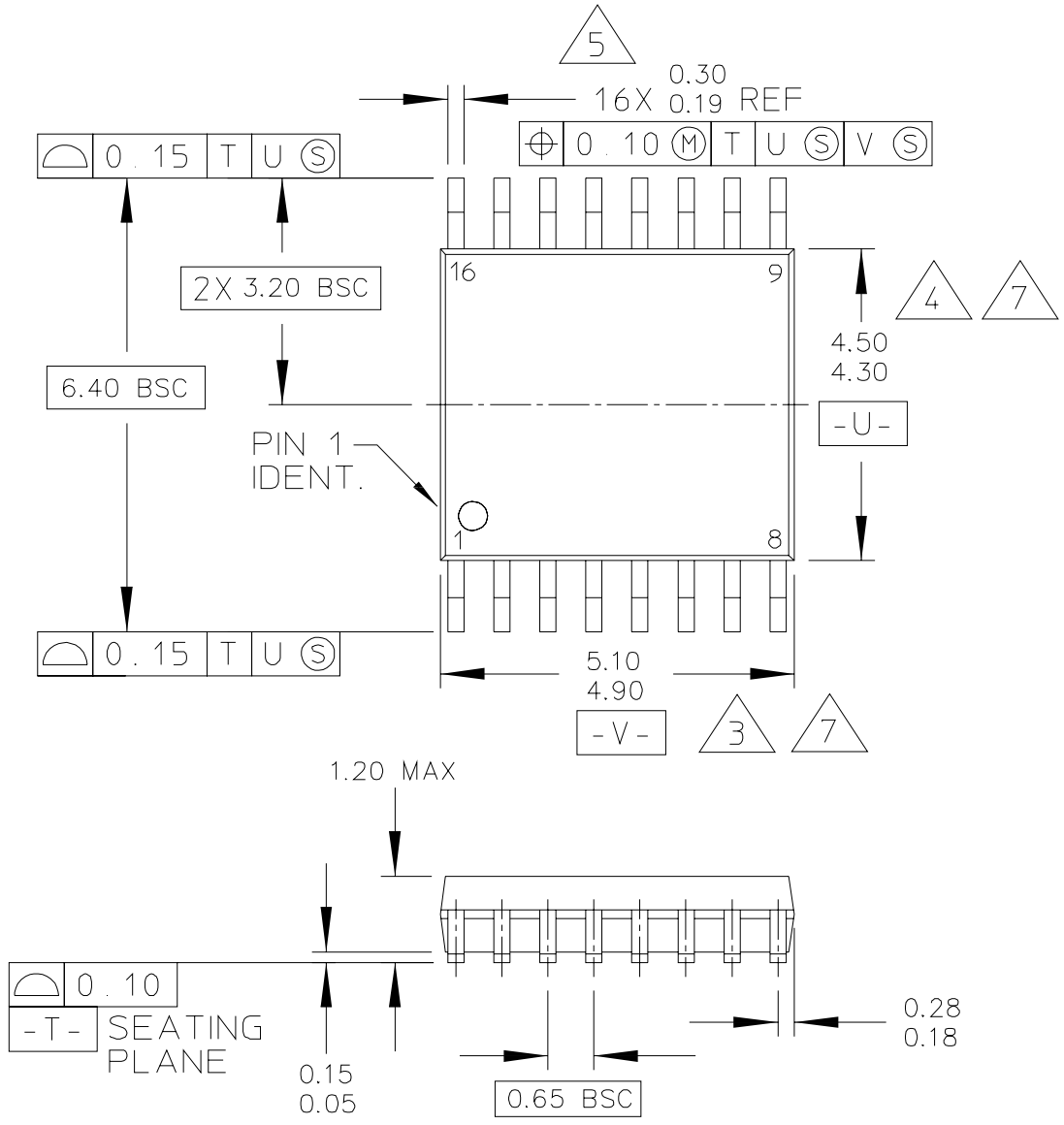
The following pages are mechanical drawings for the packages described in Table 21.



VIEW M–M

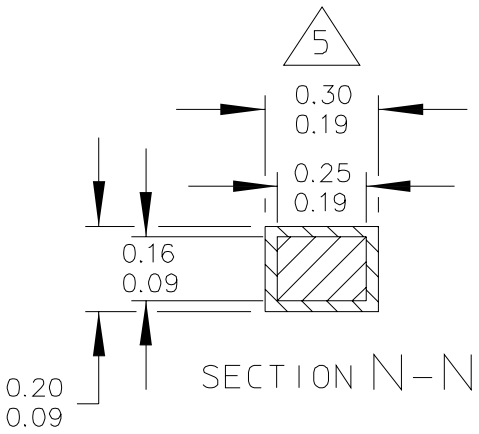
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

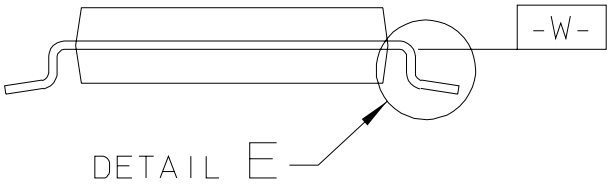
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.4 PITCH (4 X 4 X 1)	DOCUMENT NO: 98ASA00071D	REV: O
	CASE NUMBER: 2078–01	14 APR 2009
	STANDARD: NON–JEDEC	

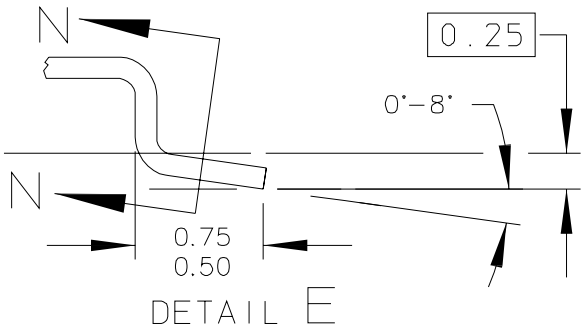


MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	







MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	