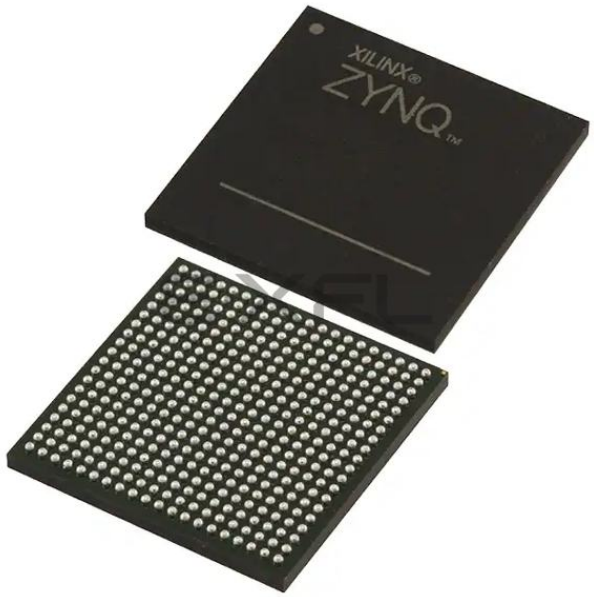

Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Artix™-7 FPGA, 85K Logic Cells
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa7z020-1clg400q

- Static memory interfaces
  - 8-bit SRAM data bus with up to 64 MB support
  - Parallel NOR flash support
  - ONFI1.0 NAND flash support (1-bit ECC)
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

I/O Peripherals and Interfaces

- Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - GMII and RGMII interfaces
- Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
  - USB 2.0 compliant device IP core
  - On-the-go, high-speed, full-speed, and low-speed modes support
  - Intel EHCI compliant USB host
  - 8-bit ULPI external PHY interface
- Two full CAN 2.0B compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
  - External PHY interface
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the programmable logic (PL)
- Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA AXI based
- QoS support on critical masters for latency and bandwidth control

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadeable adders

36 Kb Block RAM

- True Dual-Port
- Up to 72 bits wide
- Configurable as dual 18 Kb

DSP Blocks

- 18 x 25 signed multiply
- 48-bit adder/accumulator
- 25-bit pre-adder

Programmable I/O Blocks

- Supports LVCMOS, LVDS, and SSTL
- 1.2V to 3.3V I/O
- Programmable I/O delay and SerDes

JTAG Boundary-Scan

- IEEE Std 1149.1 Compatible Test Interface

Two 12-Bit Analog-to-Digital Converters

- On-chip voltage and temperature sensing
- Up to 17 external differential input channels
- One million samples per second maximum conversion rate

Automotive Temperature Range

- I-Grade: Tj = –40°C to +100°C
- Q-Grade: Tj = –40°C to +125°C

Automotive Standards

- AEC-Q100 qualification
  (Beyond AEC-Q100 Qualification is available upon request)
- Production Part Approval Process (PPAP) Documentation

Serial Transceivers

- Up to 4 receivers and transmitters
- Supports up to 6.6 Gb/s data rates

PCI Express® Block

- Root Complex and Endpoint configurations
- Supports up to Gen2 speeds
- Supports up to 4 lanes

Feature Summary

Table 1: **XA Zynq-7000 All Programmable SoC**

	Device Name	Z-7010	Z-7020	Z-7030
	Part Number	**XA7Z010**	**XA7Z020**	**XA7Z030**
Processing System	Processor Core	Dual ARM Cortex-A9 MPCore with CoreSight technology		
	Processor Extensions	NEON & Single/Double Precision Floating Point for each processor		
	Maximum Frequency	667 MHz (-1)		
	L1 Cache	32 KB Instruction, 32 KB Data per processor		
	L2 Cache	512 KB		
	On-Chip Memory	256 KB		
	External Memory Support(1)	DDR3L, DDR3, DDR2, LPDDR2		
	External Static Memory Support(1)	2x Quad-SPI, NAND, NOR		
	DMA Channels	8 (4 dedicated to Programmable Logic)		
	Peripherals(1)	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO		
	Security(2)	AES and SHA 256b for device security		
Processing System to Programmable Logic Interface Ports (Primary Interfaces and Interrupts Only)		2x AXI 32b Master 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts		
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Kintex® FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600
	Flip-Flops	35,200	106,400	157,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)
	Programmable DSP Slices (18x25 MACCs)	80	220	400
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs
	PCI Express (Root Complex and Endpoint)	–	–	Gen2 x4
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs		
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication		

Notes:

1. Restrictions apply for CLG225 package. Refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* (TRM) for details.
2. Security is shared by the processing system and the programmable logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Device-Package Combinations

XA Zynq-7000 All Programmable SoCs device-package combinations are listed in Table 1.

Table 2: **Device-Package Combinations**

Package[1]	CLG225		CLG400		CLG484		FBG484 / FBV484			
Size	13 x 13 mm		17 x 17 mm		19 x 19 mm		23 x 23 mm			
Ball Pitch	0.8 mm		0.8 mm		0.8 mm		1.0 mm			
Device	PS I/O[2]	SelectIO™ HR	PS I/O[2]	SelectIO HR[3]	PS I/O[2]	SelectIO HR[3]	PS I/O[2]	GTX	SelectIO HR	SelectIO HP[4]
XA7Z010	86	54	130	100						
XA7Z020			130	125	130	200				
XA7Z030							130	4	100	63

Notes:
1. All packages listed are Pb-free.
2. PS I/O includes user I/O and DDR I/O.
3. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
4. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

XA Zynq-7000 Family Description

The XA Zynq-7000 family offers the flexibility and scalability of an FPGA, while providing the performance, power, and ease of use typically associated with ASICs and ASSPs. The range of devices in the XA Zynq-7000 All Programmable SoC family allows designers to target cost-sensitive as well as high-performance applications from a single platform using industry-standard tools. While each device in the XA Zynq-7000 family contains the same PS, the PL and I/O resources vary between the devices.

The XA Zynq-7000 architecture enables implementation of custom logic in the PL and custom software in the PS. It allows for the realization of unique and differentiated system functions. The integration of the PS with the PL allows levels of performance that two-chip solutions (e.g., an ASSP with an FPGA) cannot match due to their limited I/O bandwidth, latency, and power budgets.

Xilinx offers a large number of soft IP for the XA Zynq-7000 family. Stand-alone and Linux device drivers are available for the peripherals in the PS and the PL. The award-winning ISE® Design Suite: System Edition development environment enables a rapid product development for software, hardware, and systems engineers. Adoption of the ARM-based PS also brings a broad range of third-party tools and IP providers in combination with Xilinx's existing PL ecosystem.

The inclusion of an application processor enables high-level operating system support, e.g., Linux. Other standard operating systems used with the Cortex-A9 processor are also available for the XA Zynq-7000 family.

The PS and the PL are on separate power domains, enabling the user of these devices to power down the PL for power management if required. The processors in the PS always boot first, allowing a software centric approach for PL configuration. PL configuration is managed by software running on the CPU, so it boots similar to an ASSP.