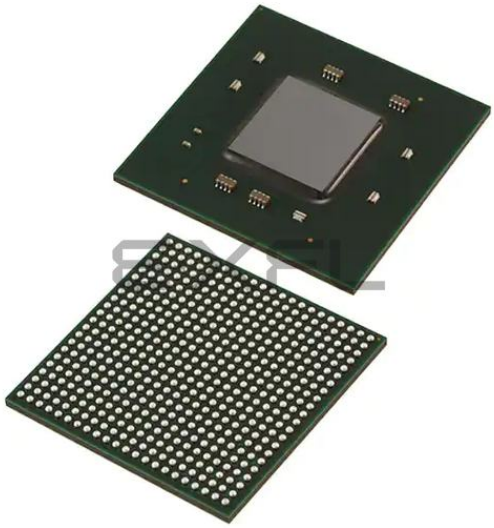

Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	667MHz
Primary Attributes	Kintex™-7 FPGA, 125K Logic Cells
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa7z030-1fbv484q

- Static memory interfaces
  - 8-bit SRAM data bus with up to 64 MB support
  - Parallel NOR flash support
  - ONFI1.0 NAND flash support (1-bit ECC)
  - 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash

8-Channel DMA Controller

- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

I/O Peripherals and Interfaces

- Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
  - Scatter-gather DMA capability
  - Recognition of 1588 rev. 2 PTP frames
  - GMII and RGMII interfaces
- Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
  - USB 2.0 compliant device IP core
  - On-the-go, high-speed, full-speed, and low-speed modes support
  - Intel EHCI compliant USB host
  - 8-bit ULPI external PHY interface
- Two full CAN 2.0B compliant CAN bus interfaces
  - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
  - External PHY interface
- Two SD/SDIO 2.0/MMC3.31 compliant controllers
- Two full-duplex SPI ports with three peripheral chip selects
- Two high-speed UARTs (up to 1 Mb/s)
- Two master and slave I2C interfaces
- GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the programmable logic (PL)
- Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments

Interconnect

- High-bandwidth connectivity within PS and between PS and PL
- ARM AMBA AXI based
- QoS support on critical masters for latency and bandwidth control

Programmable Logic (PL)

Configurable Logic Blocks (CLB)

- Look-up tables (LUT)
- Flip-flops
- Cascadeable adders

36 Kb Block RAM

- True Dual-Port
- Up to 72 bits wide
- Configurable as dual 18 Kb

DSP Blocks

- 18 x 25 signed multiply
- 48-bit adder/accumulator
- 25-bit pre-adder

Programmable I/O Blocks

- Supports LVCMOS, LVDS, and SSTL
- 1.2V to 3.3V I/O
- Programmable I/O delay and SerDes

JTAG Boundary-Scan

- IEEE Std 1149.1 Compatible Test Interface

Two 12-Bit Analog-to-Digital Converters

- On-chip voltage and temperature sensing
- Up to 17 external differential input channels
- One million samples per second maximum conversion rate

Automotive Temperature Range

- I-Grade: Tj = –40°C to +100°C
- Q-Grade: Tj = –40°C to +125°C

Automotive Standards

- AEC-Q100 qualification
  (Beyond AEC-Q100 Qualification is available upon request)
- Production Part Approval Process (PPAP) Documentation

Serial Transceivers

- Up to 4 receivers and transmitters
- Supports up to 6.6 Gb/s data rates

PCI Express® Block

- Root Complex and Endpoint configurations
- Supports up to Gen2 speeds
- Supports up to 4 lanes

Feature Summary

Table 1: **XA Zynq-7000 All Programmable SoC**

	Device Name	Z-7010	Z-7020	Z-7030
	Part Number	**XA7Z010**	**XA7Z020**	**XA7Z030**
Processing System	Processor Core	Dual ARM Cortex-A9 MPCore with CoreSight technology		
	Processor Extensions	NEON & Single/Double Precision Floating Point for each processor		
	Maximum Frequency	667 MHz (-1)		
	L1 Cache	32 KB Instruction, 32 KB Data per processor		
	L2 Cache	512 KB		
	On-Chip Memory	256 KB		
	External Memory Support(1)	DDR3L, DDR3, DDR2, LPDDR2		
	External Static Memory Support(1)	2x Quad-SPI, NAND, NOR		
	DMA Channels	8 (4 dedicated to Programmable Logic)		
	Peripherals(1)	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Peripherals w/ built-in DMA(1)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO		
	Security(2)	AES and SHA 256b for device security		
Processing System to Programmable Logic Interface Ports (Primary Interfaces and Interrupts Only)		2x AXI 32b Master 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts		
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Kintex® FPGA
	Programmable Logic Cells (Approximate ASIC Gates)(3)	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)
	Look-Up Tables (LUTs)	17,600	53,200	78,600
	Flip-Flops	35,200	106,400	157,200
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	560 KB (140)	1,060 KB (265)
	Programmable DSP Slices (18x25 MACCs)	80	220	400
	Peak DSP Performance (Symmetric FIR)	100 GMACs	276 GMACs	593 GMACs
	PCI Express (Root Complex and Endpoint)	–	–	Gen2 x4
	Analog Mixed Signal (AMS) / XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs		
	Security(2)	AES and SHA 256b for Boot Code and Programmable Logic Configuration, Decryption, and Authentication		

Notes:

1. Restrictions apply for CLG225 package. Refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual* (TRM) for details.
2. Security is shared by the processing system and the programmable logic.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Power Examples

Power for the XA Zynq-7000 All Programmable SoCs varies depending on the utilization of the PL resources, and the frequency of the PS and PL. To estimate power, use Xilinx Power Estimator (XPE) at http://www.xilinx.com/products/design_tools/logic_design/xpe.htm.

Memory Map

XA Zynq-7000 All Programmable SoCs support a 4 GB address space, organized as described in Table 5.

Table 5: **Memory Map**

Start Address	Size (MB)	Description
0x0000_0000	1,024	DDR DRAM and on-chip memory (OCM)
0x4000_0000	1,024	PL AXI slave port #0
0x8000_0000	1,024	PL AXI slave port #1
0xE000_0000	256	IOP devices
0xF000_0000	128	Reserved
0xF800_0000	32	Programmable registers access via AMBA APB bus
0xFA00_0000	32	Reserved
0xFC00_0000	64 MB - 256 KB	Quad-SPI linear address base address (except top 256 KB which is in OCM), 64 MB reserved, only 32 MB is currently supported
0xFFFC_0000	256 KB	OCM when mapped to high address space

Ordering Information

Table 6 shows the speed and temperature grades available in the different device families. Some devices might not be available in every speed and temperature grade.

Table 6: **Speed Grade and Junction Temperature Ranges**

Device	Speed Grade and Junction Temperature Range	
	Industrial (I) –40°C to +100°C	Automotive (Q) –40°C to +125°C
XA Zynq-7000	-1	-1

The ordering information, shown in Figure 4, applies to all packages including Pb-Free.

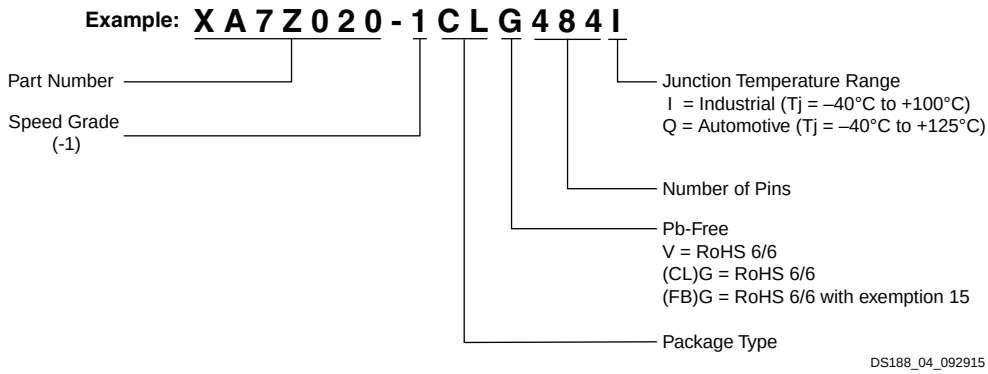

Figure 4: **Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/08/2016	1.3.1	Typographical updates.
10/15/2015	1.3	Changed document classification to Product Specification from Advance Product Specification. Updated Table 2. Updated Ordering Information.
10/10/2014	1.2	Added DDR3L to: External Memory Interfaces; Table 1; Memory Interfaces; Dynamic Memory Interfaces; and PS External Interfaces. Updated I/O Peripherals (IOP) and Clock Management.
06/04/2014	1.1	Added Z-7030 device; Serial Transceivers; PCI Express® Block; Table 4; Low-Power Serial Transceivers; Integrated Block for PCI Express Designs Updated Table 1; Table 2; Application Processor Unit (APU); Programmable Logic (PL) Description; Clock Management; Block RAM; Input/Output; Power Examples (including the removal of Table 4), and XADC (Analog-to-Digital Converter).
10/15/2012	1.0	Initial Xilinx release.

Notice of Disclaimer

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/ legal.htm#tos.

Automotive Applications Disclaimer

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.