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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8SX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	82
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds61651n50fpv

3. De c i i n f Regi e

Each egi e de c i i n incl de a bi cha , ill a ing he a angemen f bi , and a able f bi , de c ibing he meaning f he bi e ing . The anda d f ma and n a i n f bi cha and able a e de c ibed bel .

[Bit Chart]

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ASID2	ASID1	ASID0	—	—	—	—	—	—	Q	ACMP2	ACMP1	ACMP0	IFE
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Table of Bits]

Bit	Bit Name	Initial Value	R/W	Description
15	–	0	R	
14	–	0		
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	–	0	R	Reserved This bit is always read as 0.
9	–	1	R	Reserved This bit is always read as 1.
	–	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

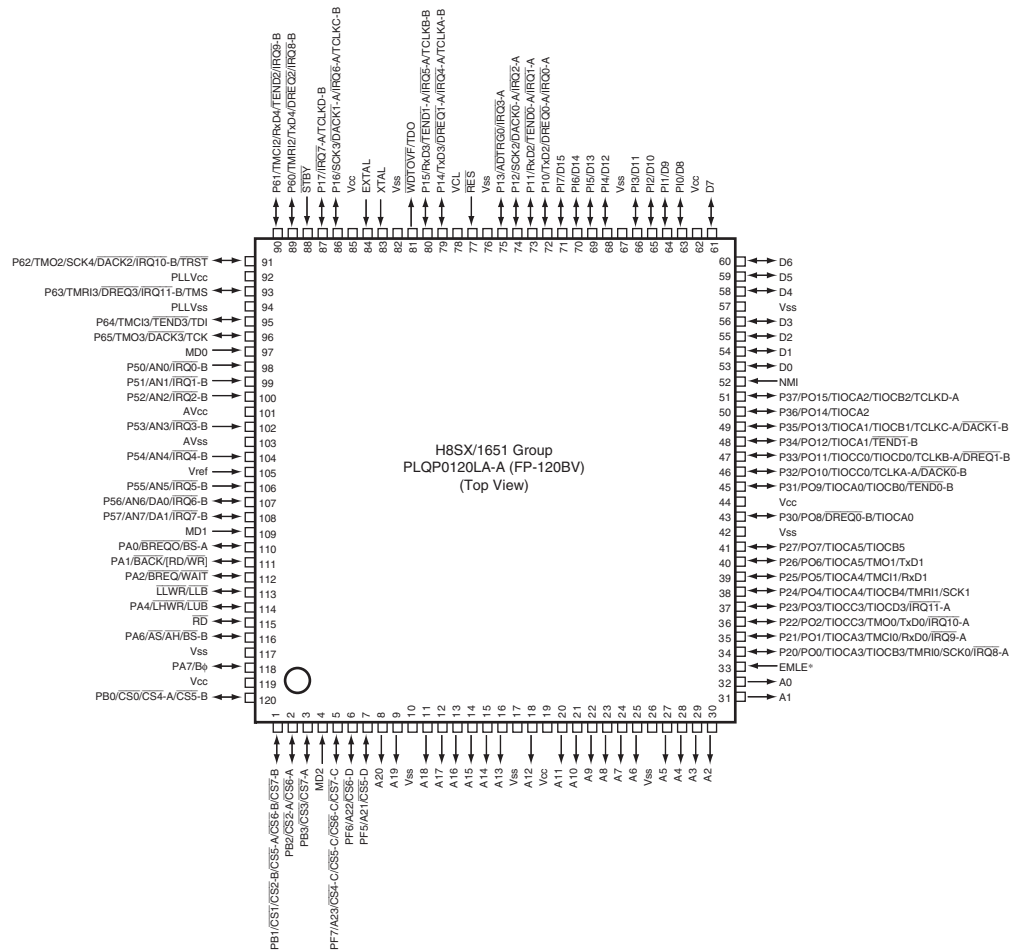
(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0
1: The initial value is 1
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

1.4 Pin Assignments



Note: * This is an on-chip emulator enable pin. Drive this pin low for the connection in normal operating mode. When this pin is driven high, the on-chip emulation function is enabled and pins P62, P63, P64, P65, and WDTOVF are dedicated for the on-chip emulator. For details on a connection example with the E10A, refer to the E10A Emulator User's Manual.

Figure 1.3 Pin Assignments

2.6.2 Memory Data Formats

Fig e 2.13 h he da a f ma in mem .

The H8SX CPU can acce d da a and l ng d da a hich a e ed a an add e e in mem . When d da a begin a an dd add e l ng d da a begin a an add e he han a m l i le f 4, a b c cle i di ided in m e acce e . F e am le, hen l ng d da a begin a an dd add e , he b c cle i di ided in b e, d, and b e acce e . In hi ca e, he e acce e a e a med be indi id al b c cle .

H e e , in c i n be fe ched, d and l ng d da a be acce ed d ing e ec i n f he ack mani la i n, bl ck an fe in c i n , and MAC in c i n h ld be l ca ed e en add e e .

When he ack in e (ER7) i ed a an add e egi e acce he ack, he e and i e h ld be d i e l ng d i e.

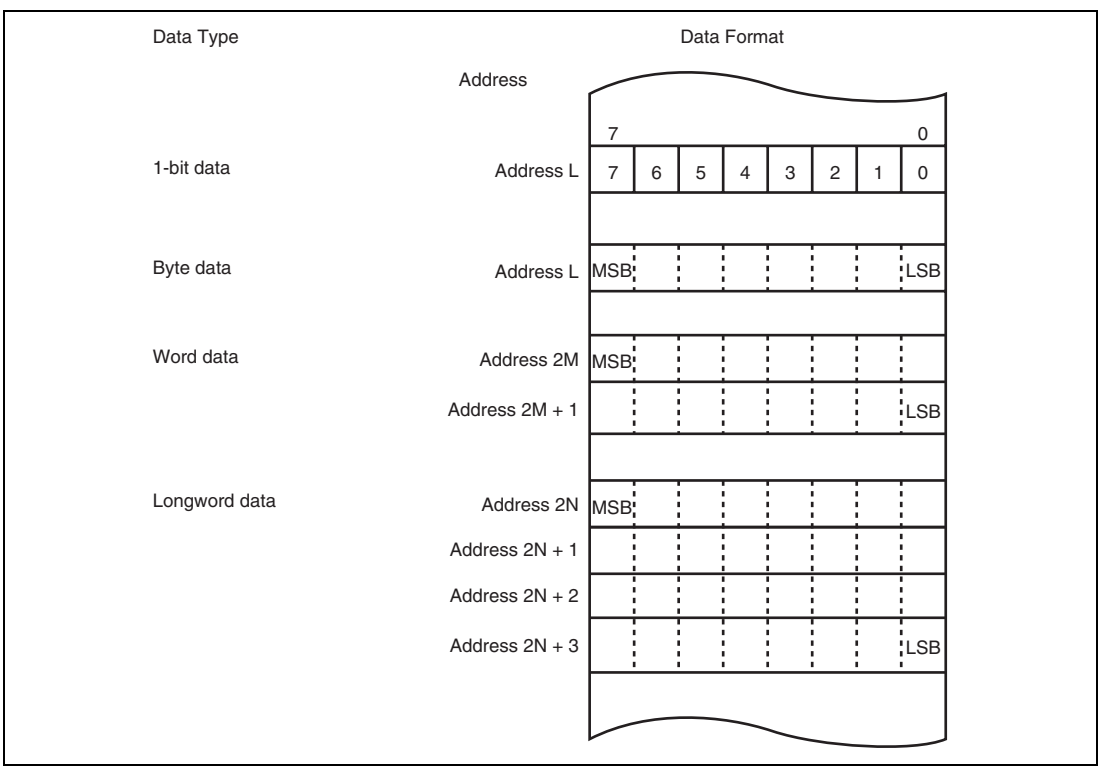
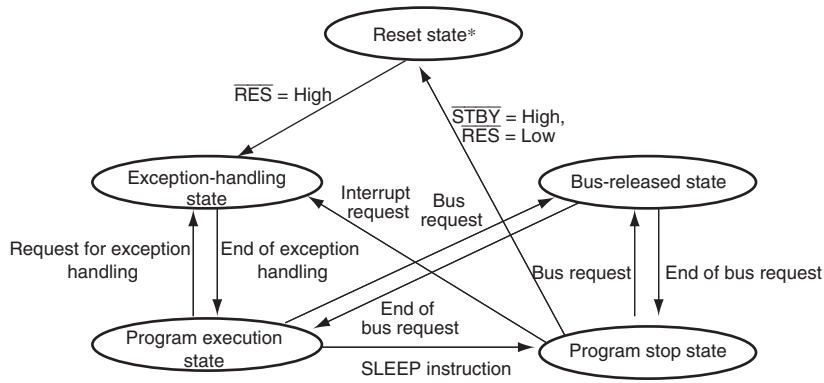


Figure 2.13 Memory Data Formats

Table 2.10 Branch Instructions

Instruction	Size	Function
BRA/BS BRA/BC	B	Tests a specified bit in memory location contents. If the specified condition is satisfied, execution branches to a specified address.
BSR/BS BSR/BC	B	Tests a specified bit in memory location contents. If the specified condition is satisfied, execution branches to a subroutine at a specified address.
Bcc	—	Branches to a specified address if the specified condition is satisfied.
BRA/S	—	Branches unconditionally to a specified address after executing the next instruction. The next instruction should be a 1-word instruction except for the block transfer and branch instructions.
JMP	—	Branches unconditionally to a specified address.
BSR	—	Branches to a subroutine at a specified address.
JSR	—	Branches to a subroutine at a specified address.
RTS	—	Returns from a subroutine
RTS/L	—	Returns from a subroutine, restoring data from the stack to general registers.



Notes: In any state, when the $\overline{\text{STBY}}$ signal goes low, the hardware standby mode is entered.

* From any state except hardware standby mode, a transition to the reset state occurs whenever the $\overline{\text{RES}}$ signal goes low. A transition can also be made to the reset state when the watchdog timer overflows.

Figure 2.16 State Transitions

Bit	Bit Name	Initial Value	R/W	Description
10	IPR10	1	R/W	Sets the priority level of the corresponding interrupt source. 000: Priority level 0 (lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (highest)
9	IPR9	1	R/W	
8	IPR8	1	R/W	
7	—	0	R	Reserved This is a read-only bit and cannot be modified.
6	IPR6	1	R/W	Sets the priority level of the corresponding interrupt source. 000: Priority level 0 (lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (highest)
5	IPR5	1	R/W	
4	IPR4	1	R/W	
3	—	0	R	Reserved This is a read-only bit and cannot be modified.

A bl ck diag am f in e IRQn i h n in fig e 5.2.

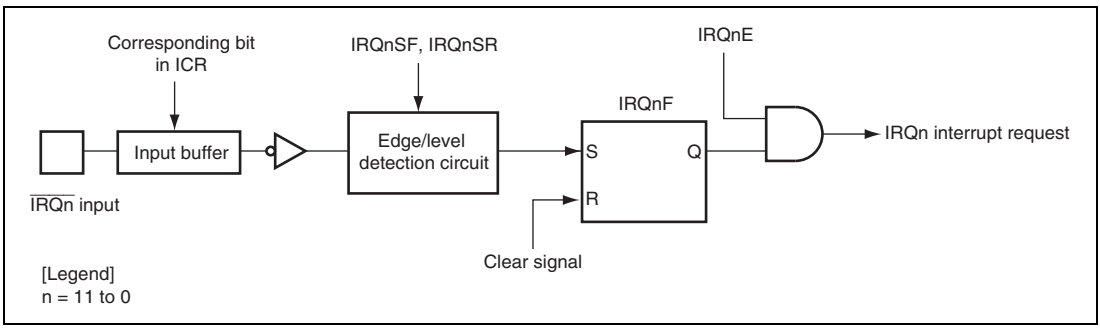


Figure 5.2 Block Diagram of Interrupts IRQn

When he IRQ en ing c n l in ISCR i e a l le el f ignal $\overline{\text{IRQn}}$, he le el f $\overline{\text{IRQn}}$ h ld be held l n il an in e handling a . Then e he c e nding in ignal $\overline{\text{IRQn}}$ high in he in e handling ine and clea he IRQnF 0. In e ma n be e ec ed

Name	Symbol	I/O	Function
Data transfer acknowledge 2 (DMAC_2)	DACK2	Output	Data transfer acknowledge signal for DMAC_2 single address transfer
Data transfer acknowledge 1 (DMAC_1)	DACK1	Output	Data transfer acknowledge signal for DMAC_1 single address transfer
Data transfer acknowledge 0 (DMAC_0)	DACK0	Output	Data transfer acknowledge signal for DMAC_0 single address transfer
External bus clock	Bϕ	Output	External bus clock

Table 6.3 Pin Functions in Each Interface

	Initial State			Basic Bus		Byte Control SRAM	Burst ROM		Address/Data Multiplexed I/O		
Pin Name	16	8	Single-Chip	16	8	16	16	8	16	8	Remarks
Bϕ	Output	Output	—	O	O	O	O	O	O	O	
CS0	Output	Output	—	O	O	O	O	O	—	—	
CS1	—	—	—	O	O	O	O	O	—	—	
CS2	—	—	—	O	O	O	—	—	—	—	
CS3	—	—	—	O	O	O	—	—	O	O	
CS4	—	—	—	O	O	O	—	—	O	O	
CS5	—	—	—	O	O	O	—	—	O	O	
CS6	—	—	—	O	O	O	—	—	O	O	
CS7	—	—	—	O	O	O	—	—	O	O	
BS	—	—	—	O	O	O	O	O	O	O	
RD/WR	—	—	—	O	O	O	O	O	O	O	
AS	Output	Output	—	O	O	O	O	O	—	—	
AH	—	—	—	—	—	—	—	—	O	O	
RD	Output	Output	—	O	O	O	O	O	O	O	
LHWR/LUB	Output	Output	—	O	—	O	O	—	O	—	
LLWR/LLB	Output	Output	—	O	O	O	O	O	O	O	
WAIT	—	—	—	O	O	O	O	O	O	O	Controlled by WAITE

[Legend]

O: Used as a bus control signal

—: Not used as a bus control signal (used as a port input when initialized)

A DMA an fe i ed and an in e b an e ended e ea a ea e fl can be e e ed he CPU hen he c n en f he add e egi e each he end add e f he e ended e ea a ea. When an e fl n he e ended e ea a ea e in DSAR cc hile he SARIE bi in DACR i e 1, he ESIF bi in DMDR i e 1 and he DTE bi in DMDR i clea ed 0 he an fe . A hi ime, if he ESIE bi in DMDR i e 1, an in e b an e ended e ea a ea e fl i e e ed he CPU. When he DARIE bi in DACR i e 1, an e fl n he e ended e ea a ea e in DDAR cc , meaning ha he de ina i n ide i a a ge . D ing he in e handling, e ing he DTE bi in DMDR e me he an fe .

Fig e 7.15 h an e am le f he e ended e ea a ea e a i n.

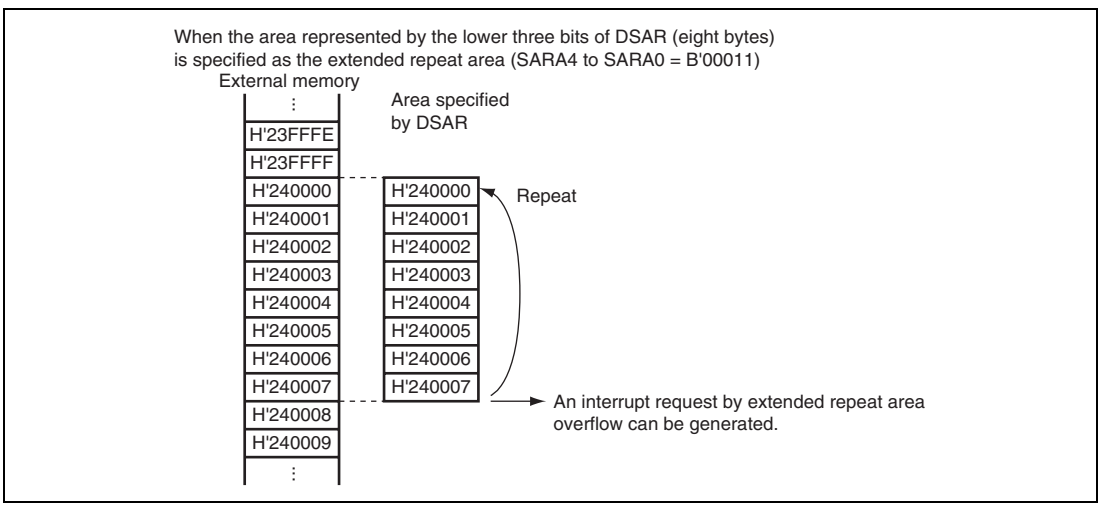


Figure 7.15 Example of Extended Repeat Area Operation

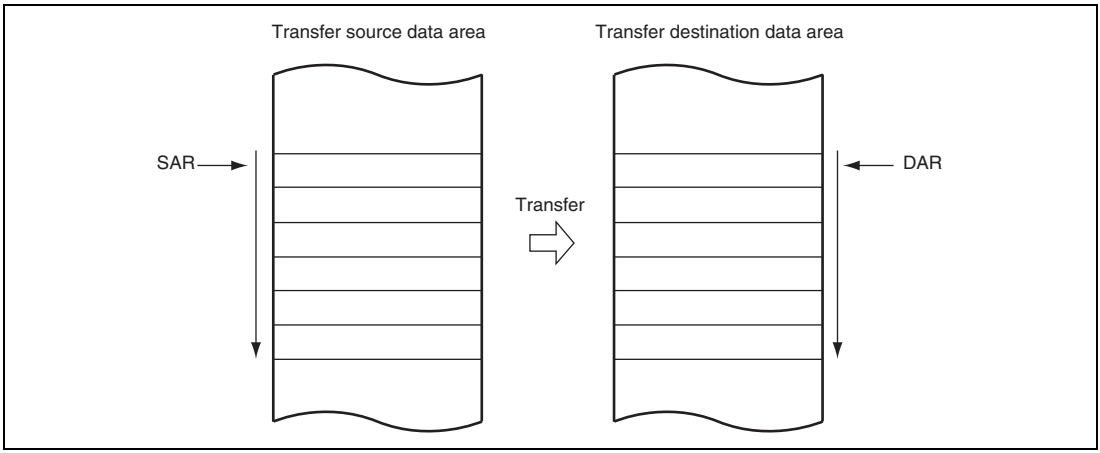


Figure 8.7 Memory Map in Normal Transfer Mode

8.5.5 Repeat Transfer Mode

In e ea an fe m de, ne e a i n an fe ne b e, ne d, ne l ng d f da a. B he DTS bi in MRB, ei he he ce de ina i n can be ecified a a e ea a ea. F m 1 256 an fe can be ecified. When he ecified n mbe f an fe end , he an fe c n e and add e egi e ecified a he e ea a ea i e ed he ini ial a e, and an fe i e ea ed. The he add e egi e i hen inc emen ed, dec emen ed, lef fi ed. In e ea an fe m de, he an fe c n e (CRAL) i da ed he al e ecified in CRAH hen CRAL bec me H 00. Th he an fe c n e al e d e n each H 00, and he ef e a CPU in e cann be e e ed hen DISEL = 0.

Table 8.7 li he egi e f nc i n in e ea an fe m de. Fig e 8.8 h he mem ma in e ea an fe m de.

9.2 Output Buffer Control

Thi ec i n de c ibe he i i f each in.

The name f each e i he al m d le in i f ll ed b "_OE". Thi (f e am le: MIOCA4_OE) indica e he he he f he c e nding f nc i n i alid (1) if an he e ing i ecified (0). Table 9.5 li each ignal alid e ing. F de ail n he c e nding ignal , ee he egi e de c i i n f each e i he al m d le. If he name f each e i he al m d le in i f ll ed b A B, he in f nc i n can be m dified b he f nc i n c n l egi e (PFCR). F de ail , ee ec i n 9.3, P F nc i n C n lle .

9.2.1 Port 1

(1) P17/$\overline{\text{IRQ7}}$-A/TCLKD-B

The in f nc i n i i ched a h n bel acc ding he P17DDR bi e ing.

		Setting
		I/O Port
Module Name	Pin Function	P17DDR
I/O port	P17 output	1
	P17 input (initial setting)	0

(2) P16/SCK3/$\overline{\text{DACK1}}$-A/$\overline{\text{IRQ6}}$-A/TCLKC-B

The in f nc i n i i ched a h n bel acc ding he c mbina i n f he DMAC and SCI egi e e ing and P16DDR bi e ing.

		Setting		
		DMAC	SCI	I/O Port
Module Name	Pin Function	DACK1A_OE	SCK3_OE	P16DDR
DMAC	DACK1-A output	1	—	—
SCI	SCK3 output	0	1	—
I/O port	P16 output	0	0	1
	P16 input (initial setting)	0	0	0

Port		Output Specification Signal Name	Output Signal Name	Signal Selection Register Settings	Peripheral Module Settings
P2	5	TIOCA4_OE	TIOCA4		TPU.TIOR4.IOA3 = 0, TPU.TIOR4.IOA[1,0] = 01/10/11
		PO5_OE	PO5		NDERL.NDER5 = 1
	4	TIOCB4_OE	TIOCB4		TPU.TIOR4.IOB3 = 0, TPU.TIOR4.IOB[1,0] = 01/10/11
		SCK1_OE	SCK1		When SCMR.SMIF = 1: SCR.TE = 1 or SCR.RE = 1 while SMR.GM = 0, SCR.CKE [1, 0] = 01 or while SMR.GM = 1 When SCMR.SMIF = 0: SCR.TE = 1 or SCR.RE = 1 while SMR.C/A = 0, SCR.CKE [1, 0] = 01 or while SMR.C/A = 1, SCR.CKE 1 = 0
		PO4_OE	PO4		NDERL.NDER4 = 1
	3	TIOCD3_OE	TIOCD3		TPU.TMDR.BFB = 0, TPU.TIORL3.IOD3 = 0, TPU.TIORL3.IOD[1,0] = 01/10/11
		PO3_OE	PO3		NDERL.NDER3 = 1
	2	TIOCC3_OE	TIOCC3		TPU.TMDR.BFA = 0, TPU.TIORL3.IOC3 = 0, TPU.TIORL3.IOD[1,0] = 01/10/11
		TMO0_OE	TMO0		TCSR.OS[3,2] = 01/10/11 or TCSR.OS[1,0] = 01/10/11
		TxD0_OE	TxD0		SCR.TE = 1
		PO2_OE	PO2		NDERL.NDER2 = 1
	1	TIOCA3_OE	TIOCA3		TPU.TIORH3.IOA3 = 0, TPU.TIORH3.IOA[1,0] = 01/10/11
		PO1_OE	PO1		NDERL.NDER1 = 1
	0	TIOCB3_OE	TIOCB3		TPU.TIORH3.IOB3 = 0, TPU.TIORH3.IOB[1,0] = 01/10/11
		SCK0_OE	SCK0		When SCMR.SMIF = 1: SCR.TE = 1 or SCR.RE = 1 while SMR.GM = 0, SCR.CKE [1, 0] = 01 or while SMR.GM = 1 When SCMR.SMIF = 0: SCR.TE = 1 or SCR.RE = 1 while SMR.C/A = 0, SCR.CKE [1, 0] = 01 or while SMR.C/A = 1, SCR.CKE 1 = 0
		PO0_OE	PO0		NDERL.NDER0 = 1

10.2 Input/Output Pins

Table 10.2 h TPU in c nfig a i n .

Table 10.2 Pin Configuration

Channel	Symbol	I/O	Function
All	TCLKA	Input	External clock A input pin (Channel 1 and 5 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 and 5 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 and 4 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 and 4 phase counting mode B phase input)
0	TIOCA0	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOCB0	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOCC0	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOCD0	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOCA1	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOCB1	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOCA2	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOCB2	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOCA3	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOCB3	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOCC3	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOCD3	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOCA4	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOCB4	I/O	TGRB_4 input capture input/output compare output/PWM output pin
5	TIOCA5	I/O	TGRA_5 input capture input/output compare output/PWM output pin
	TIOCB5	I/O	TGRB_5 input capture input/output compare output/PWM output pin

10.4.2 Synchronous Operation

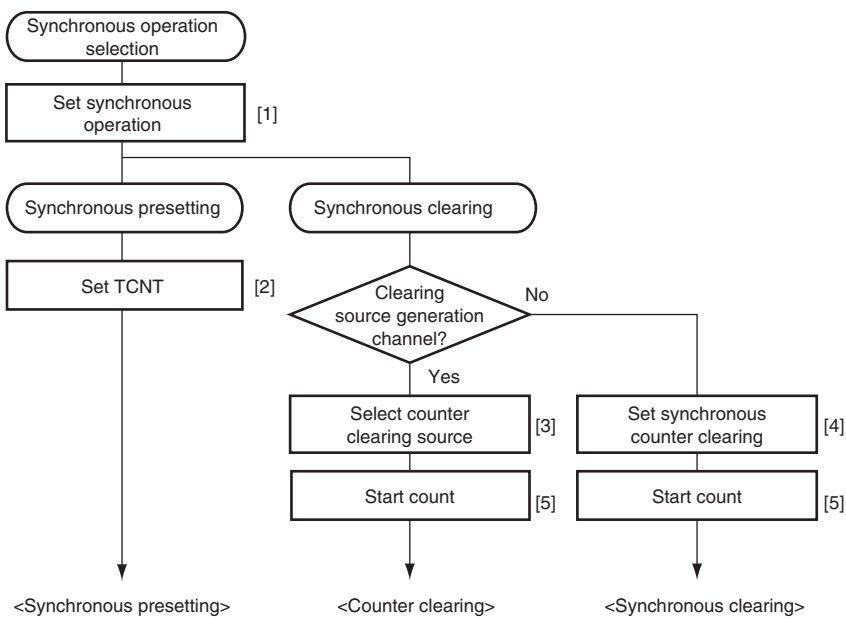
In nch n e a i n, he al e in m l i le TCNT c n e can be e i en im l ane l (nch n e e ing). Al , m l i le TCNT c n e can be clea ed im l ane l (nch n clea ing) b making he a ia e e ing in TCR.

S nch n e a i n enable TGR be inc emen ed i h e ec a ingle ime ba e.

Channel 0 5 can all be de igna ed f nch n e a i n.

(1) Example of Synchronous Operation Setting Procedure

Fig e 10.10 h an e am le f he nch n e a i n e ing ced e.



[1] Set the SYNC bits in TSYR corresponding to the channels to be designated for synchronous operation to 1.

[2] When the TCNT counter of any of the channels designated for synchronous operation is written to, the same value is simultaneously written to the other TCNT counters.

[3] Use bits CCLR2 to CCLR0 in TCR to specify TCNT clearing by input capture/output compare, etc.

[4] Use bits CCLR2 to CCLR0 in TCR to designate synchronous clearing for the counter clearing source.

[5] Set the CST bits in TSTR for the relevant channels to 1, to start the count operation.

Figure 10.10 Example of Synchronous Operation Setting Procedure

Table 14.8 BRR Settings for Various Bit Rates (Smart Card Interface Mode, n = 0, S = 372)

Bit Rate	Operating Frequency Pϕ (MHz)											
	7.1424			10.00			10.7136			13.00		
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	30	0	1	25	0	1	8.99

Bit Rate	Operating Frequency Pϕ (MHz)											
	14.2848			16.00			18.00			20.00		
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	15.99	0	2	6.60

Bit Rate	Operating Frequency Pϕ (MHz)											
	25.00			30.00			33.00			35.00		
(bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	12.49	0	3	5.01	0	4	7.59	0	4	1.99

Table 14.9 Maximum Bit Rate for Each Operating Frequency (Smart Card Interface Mode, S = 372)

Pϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	Pϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
7.1424	9600	0	0	18.00	24194	0	0
10.00	13441	0	0	20.00	26882	0	0
10.7136	14400	0	0	25.00	33602	0	0
13.00	17473	0	0	30.00	40323	0	0
14.2848	19200	0	0	33.00	44355	0	0
16.00	21505	0	0	35.00	47043	0	0