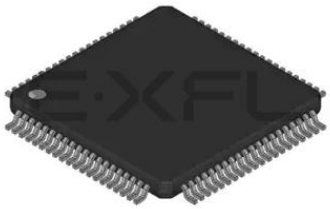
Infineon Technologies - XC2733X20F66LAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	166KB (166K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 19x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2733x20f66laakxuma1

16/32-Bit

Architecture

XC2733X

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance
XC2000 Family / Econo Line

Data Sheet

V1.3 2015-02

Microcontrollers

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
44	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
45	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
46	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1D	I	St/B	**CAN Node 1 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	TDI_B	I	St/B	**JTAG Test Data Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
59	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLK OUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	TMS_B	I	St/B	**JTAG Test Mode Selection Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
60	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U0C0_DOUT	O2	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU63_COU T62	O3	St/B	**CCU63 Channel 2 Output**
	TDO_A	OH	St/B	**DAP1/JTAG Test Data Output**
	SPD_0	I/OH	St/B	**SPD Input/Output**
	C0	I	St/B	**Configuration Pin 0**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**
61	XTAL2	O	Sp/M	**Crystal Oscillator Amplifier Output**

3 Functional Description

The architecture of the XC2733X combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC2733X.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC2733X.

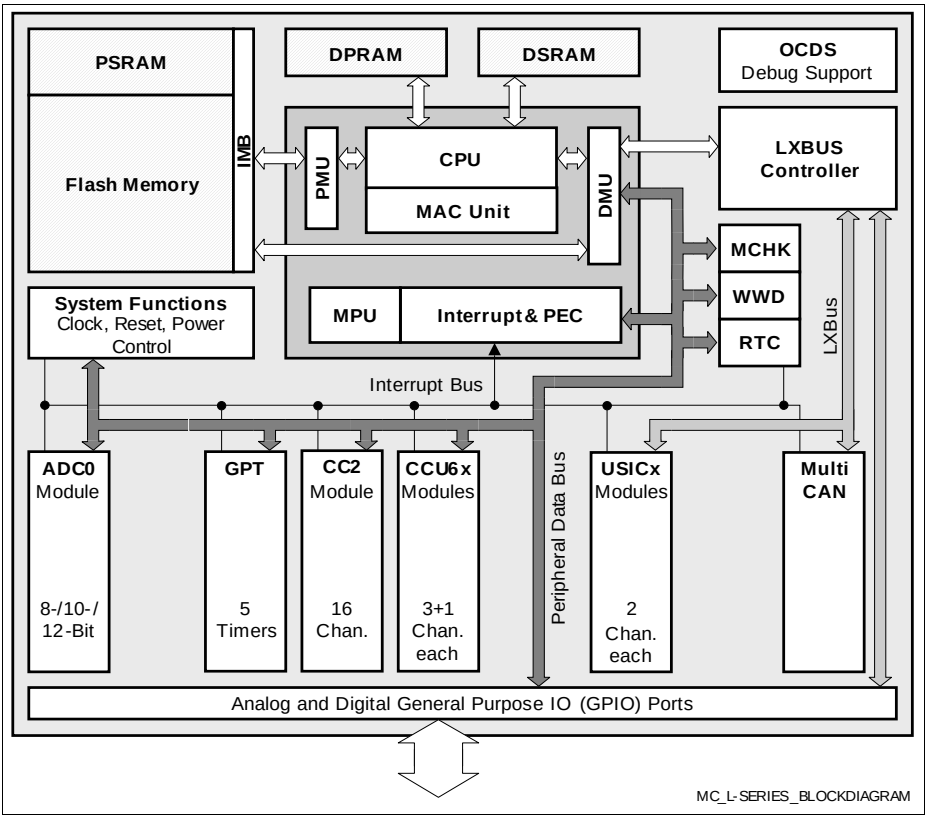

Figure 3 Block Diagram

3.5 Interrupt System

The architecture of the XC2733X supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is 'stolen' from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC2733X has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XC2733X can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 64 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC2733X provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called 'Hardware Traps'. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

3.12 Universal Serial Interface Channel Modules (USIC)

The XC2733X features the USIC modules USIC0 and USIC1. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

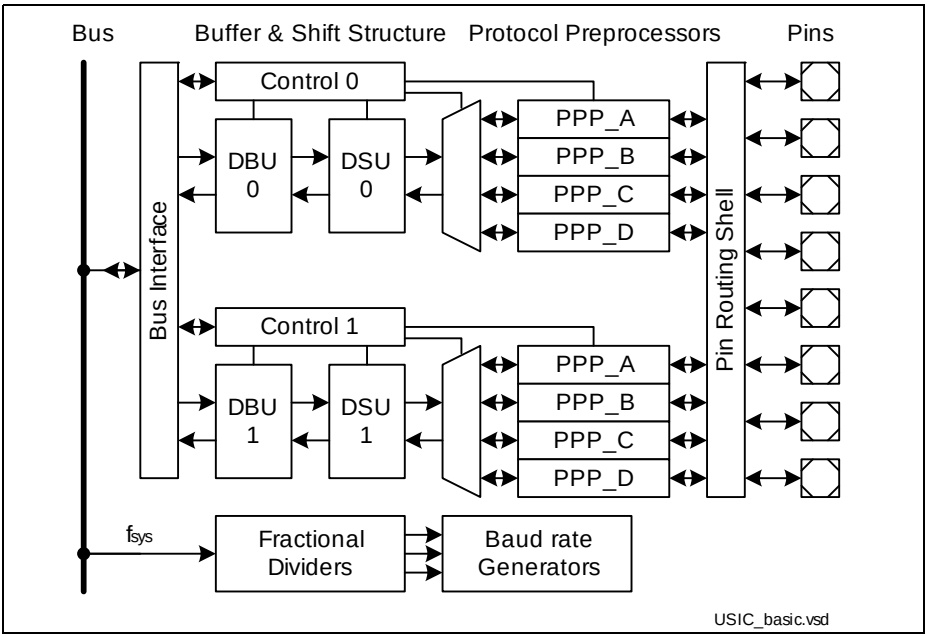

Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.14 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.15 Window Watchdog Timer

The Window Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Window Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Window Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Window Watchdog Timer overflows, generating a reset request.

The Window Watchdog Timer has a ‘programmable window boundary’, it disallows refresh during the Window Watchdog Timer’s count-up. A refresh during this window-boundary will cause the Window Watchdog Timer to also generate a reset request.

The Window Watchdog Timer is a 16-bit timer clocked with either the system clock or the independent wake-up oscillator clock, divided by 16,384 or 256. The Window Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Window Watchdog Timer is reloaded.

Table 11 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XC2733X, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4 Electrical Parameters

The operating range for the XC2733X is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-15	–	–	mA	
Output current on a pin when low value is driven	I_{OL} SR	–	–	15	mA	
Overload current	I_{OV} SR	-5	–	5	mA	1)
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	50	mA	1)
Junction Temperature	T_J SR	-40	–	150	°C	
Storage Temperature	T_{ST} SR	-65	–	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	-0.5	–	6.0	V	
Voltage on any pin with respect to ground (Vss)	V_{IN} SR	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

Note: Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Pullup/Pulldown Device Behavior

Most pins of the XC2733X feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 12** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

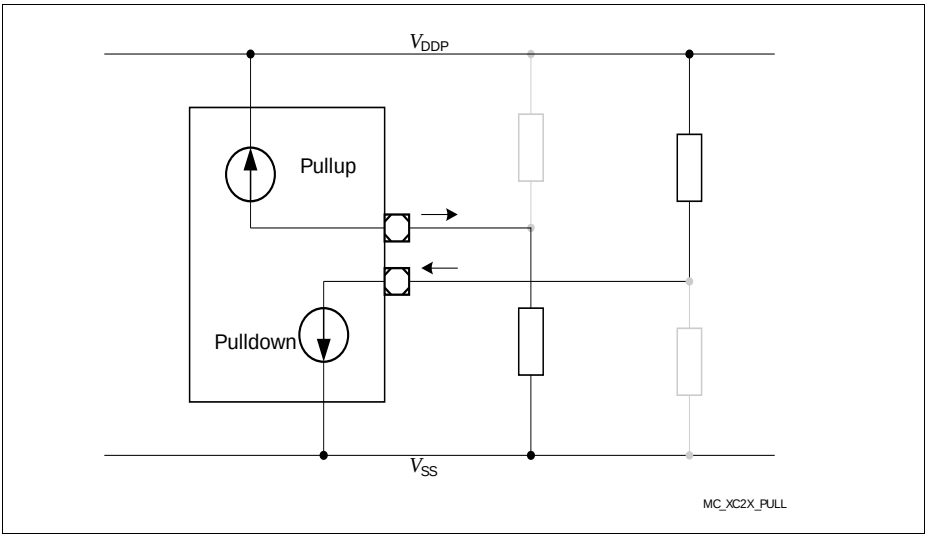

Figure 12 Pullup/Pulldown Current Definition

Table 18 Switching Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power supply current (active) with all peripherals active and EVVRs on	I_{SACT} CC	–	6 + 0.5 x f_{SYS} 1)	8 + 0.75 x f_{SYS} 1)	mA	power_mode= active ; voltage_range= both 2)3)4)
Power supply current in stopover mode, EVVRs on	I_{SSO} CC	–	0.7	2.0	mA	power_mode= stopover ; voltage_range= both

1) f_{SYS} in MHz

2) The pad supply voltage pins (V_{DDPB}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small current is consumed because the drivers input stages are switched.

3) Please consider the additional conditions described in section "Active Mode Power Supply Current".

4) The pad supply voltage only has a minor influence on this parameter.

Active Mode Power Supply Current

The actual power supply current in active mode not only depends on the system frequency but also on the configuration of the XC2733X's subsystem.

Besides the power consumed by the device logic the power supply pins also provide the current that flows through the pin output drivers.
A small current is consumed because the drivers' input stages are switched.

Table 22 ADC Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	8.5	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15.0	µs	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation.
2) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
3) If a reduced analog reference voltage between 1V and V_{DDPB} / 2 is used, then there are additional decrease in the ADC speed and accuracy.
4) If the analog reference voltage range is below V_{DDPB} but still in the defined range of V_{DDPB} / 2 and V_{DDPB} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain and Offset errors increase also by the factor 1/k.
5) If the analog reference voltage is > V_{DDPB}, then the ADC converter errors increase.
6) TUE is based on 12-bit conversion.
7) TUE is tested at V_{AREF} = V_{DDPB} = 3.3 V, V_{AGND} = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the measurement time.

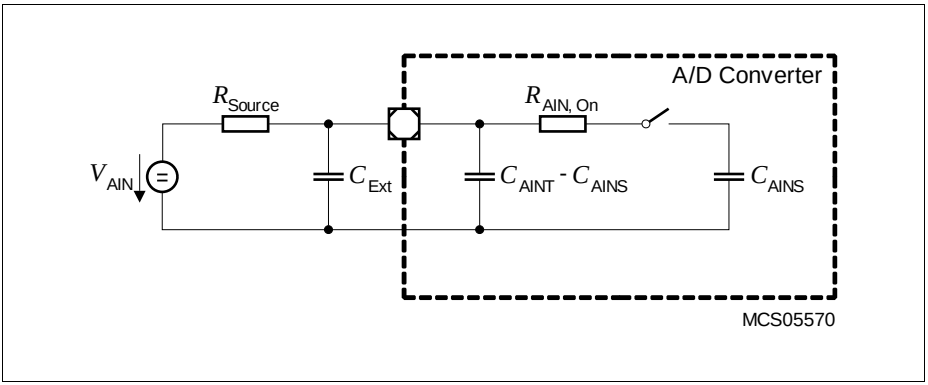

Figure 15 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the XC2733X's A/D converters are programmable. The timing above can be calculated using **Table 23**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Coding of bit fields LEVxV in SWD Configuration Registers

After power-on the supply watch dog is preconfigured to operate in the lower voltage range.

Table 25 Coding of bit fields LEVxV in Register SWDCON0

Code	Default Voltage Level	Notes[1)]
0000_B	-	out of valid operation range
0001_B	3.0 V	LEV1V: reset request
0010_B - 0101_B	3.1 V - 3.4 V	step width is 0.1 V
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B - 1110_B	4.6 V - 5.0 V	step width is 0.1 V
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Coding of bit fields LEVxV in PVC Configuration Registers

The core voltages are controlled internally to the nominal value of 1.5 V; a variation of ±10 % is allowed. These operation conditions limit the possible PVC monitoring values to the predefined reset values shown in **Table 26**.

Table 26 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B - 011_B	-	out of valid operation range
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B - 111_B	-	out of valid operation range

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

Table 27 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{ER} SR	–	–	15000	cycles	$t_{RET} \geq$ 5 years; Valid for up to 64 user selected sectors (data storage)
		–	–	1000	cycles	$t_{RET} \geq$ 20 years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
3) Value of IMB_IMBCTRL.WSFLASH.
4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC2733X Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Table 28 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency	f_{VCO} CC	50	–	110	MHz	*VCOSEL*= 00_B; *VCOmode*= controlled
		10	–	40	MHz	*VCOSEL*= 00_B; *VCOmode*= free running
		100	–	160	MHz	*VCOSEL*= 01_B; *VCOmode*= controlled
		20	–	80	MHz	*VCOSEL*= 01_B; *VCOmode*= free running

4.7.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

$f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.7.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer's Guide.

4.7.4 Pad Properties

The output pad drivers of the XC2733X can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 30 is valid under the following conditions: $V_{DDP} \leq$ 5.5 V; V_{DDP}typ. 5 V; $V_{DDP} \geq$ 4.5 V

Table 30 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC	–	–	3.0	mA	Driver_Strength = Medium
		–	–	5.0	mA	Driver_Strength = Strong
		–	–	0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	1.0	mA	Driver_Strength = Medium
		–	–	1.6	mA	Driver_Strength = Strong
		–	–	0.25	mA	Driver_Strength = Weak

Table 34 USIC SSC Slave Mode Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	7	–	33	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Table 35 is valid under the following conditions: C_L= 20 pF; *SSC*= slave ; voltage_range= lower

Table 35 USIC SSC Slave Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	7	–	–	ns	
Receive data input setup time to shift clock receive edge[1)]	t_{12} SR	7	–	–	ns	
Data input DX0 hold time from clock input DX1 receive edge[1)]	t_{13} SR	5	–	–	ns	
Data output DOUT valid time	t_{14} CC	8	–	41	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

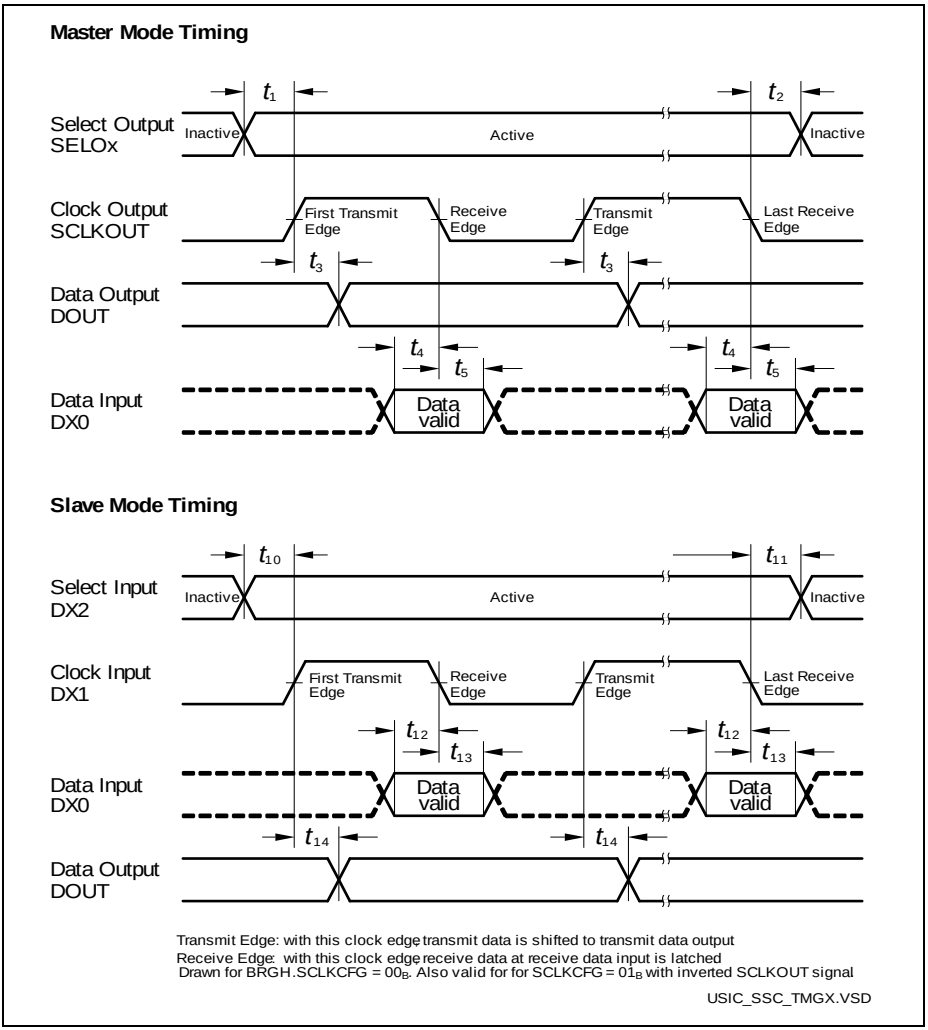

Figure 21 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Table 37 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 37 DAP Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period	t_{11} SR	100[1)]	–	–	ns	
DAP0 high time	t_{12} SR	8	–	–	ns	
DAP0 low time	t_{13} SR	8	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	4	ns	
DAP0 clock fall time	t_{15} SR	–	–	4	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6	–	–	ns	pad_type= standard
DAP1 hold after DAP0 rising edge	t_{17} SR	6	–	–	ns	pad_type= standard
DAP1 valid per DAP0 clock period[2)]	t_{19} CC	87	92	–	ns	pad_type= standard

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

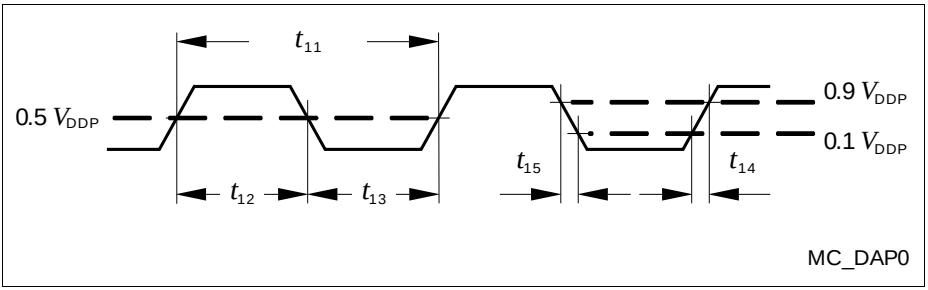

Figure 22 Test Clock Timing (DAP0)

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 38 is valid under the following conditions: C_L= 20 pF; voltage_range= upper

Table 38 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	100[1]	–	–	ns	[2]
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[3]	t_8 CC	–	29	32	ns	
TDO high impedance to valid output from TCK falling edge[4][3]	t_9 CC	–	29	32	ns	
TDO valid output to high impedance from TCK falling edge[3]	t_{10} CC	–	29	32	ns	
TDO hold after TCK falling edge[3]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) Under typical conditions, the JTAG interface can operate at transfer rates up to 10 MHz.

3) The falling edge on TCK is used to generate the TDO timing.

4) The setup time for TDO is given implicitly by the TCK cycle time.