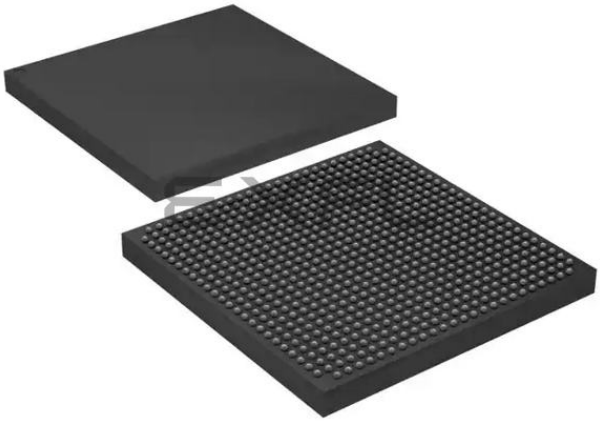

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	425984
Number of I/O	492
Number of Gates	1900000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2a15f672c7

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

Figure 1. APEX II Device Block Diagram

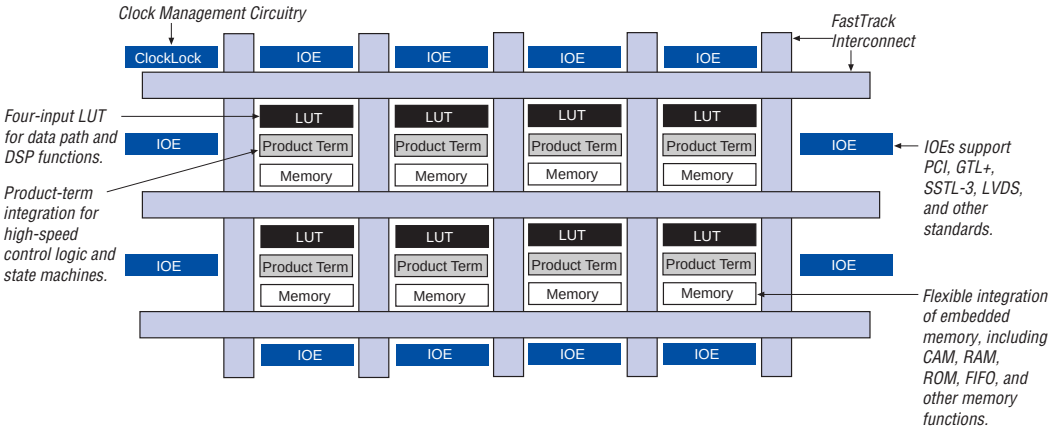


Table 4 lists the resources available in APEX II devices.

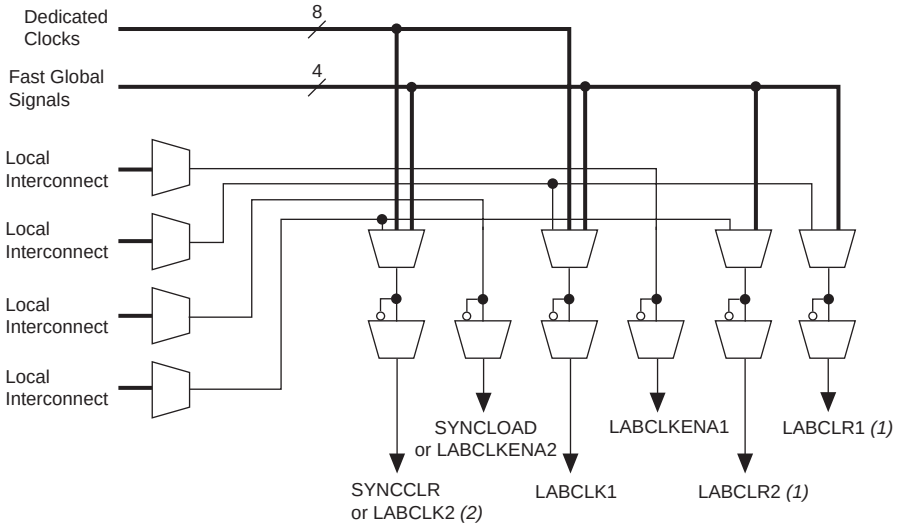
Table 4. APEX II Device Resources

Device	MegaLAB Rows	MegaLAB Columns	ESBs
EP2A15	26	4	104
EP2A25	38	4	152
EP2A40	40	4	160
EP2A70	70	4	280

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

LE Operating Modes

The APEX II LE can operate in one of the following three modes:

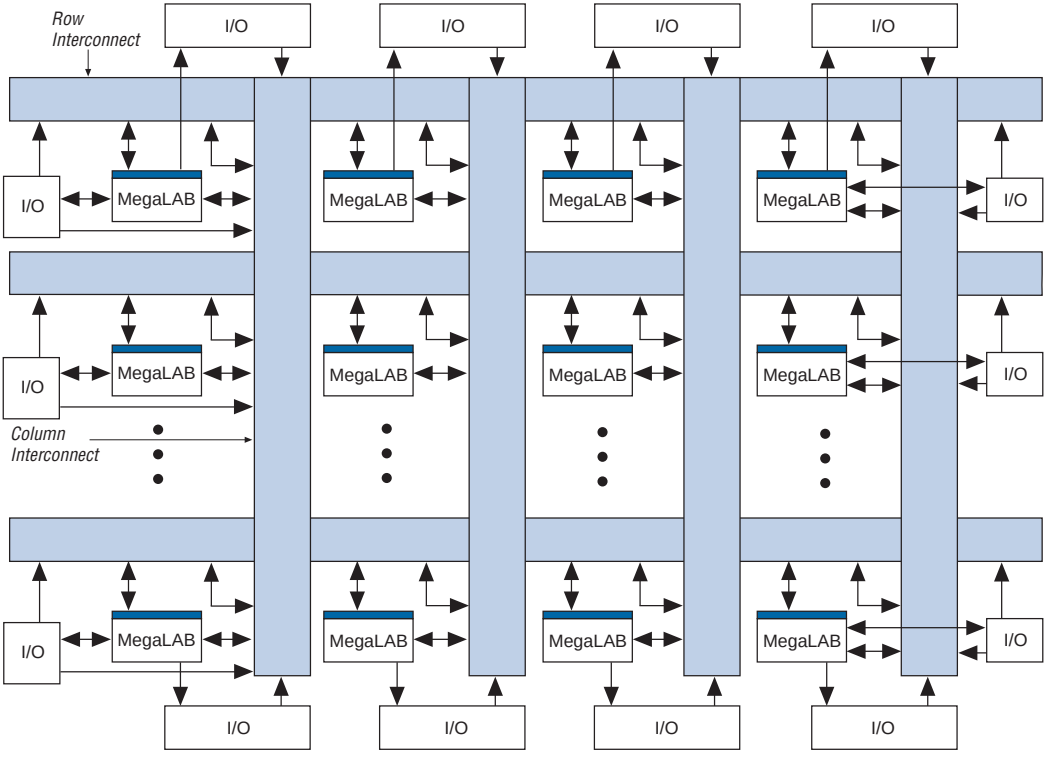
- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX II Interconnect Structure



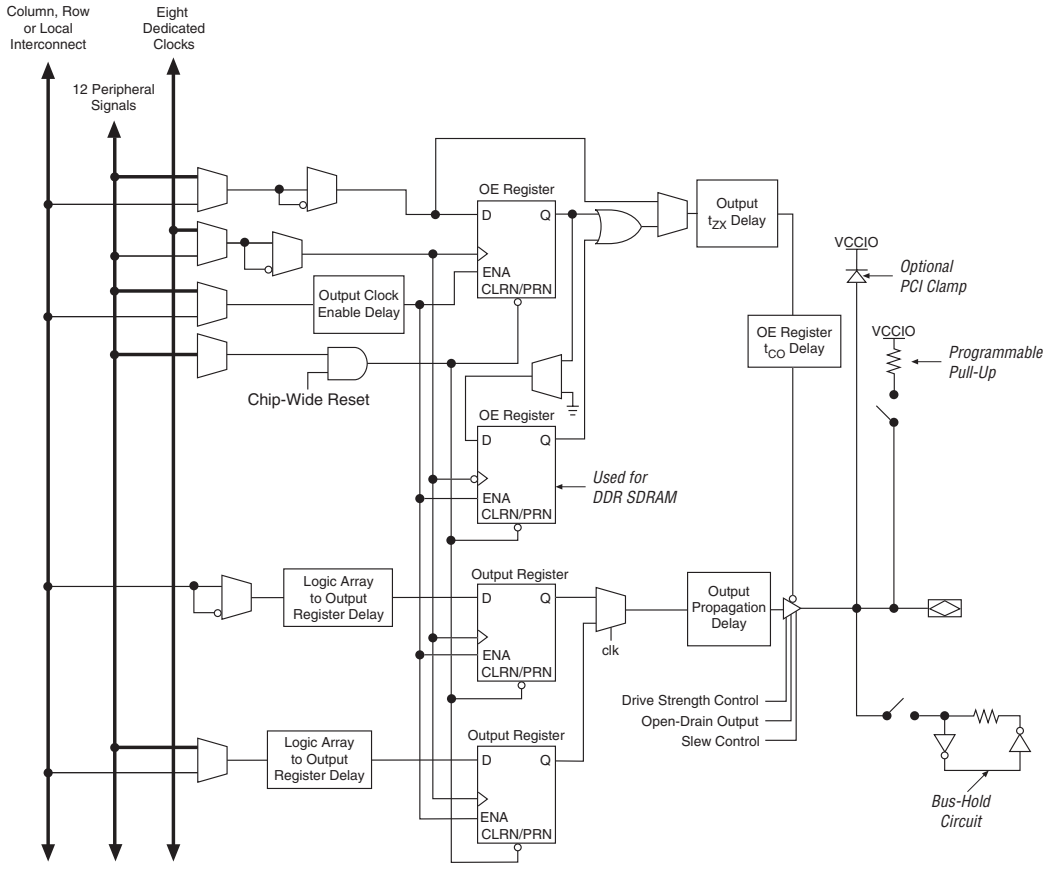
A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

Table 7. Peripheral Control Bus Destinations

Peripheral Bus	I/O Control Signal
Output Enable 0 [OE0]	OE
Output Enable 1 [OE1]	OE
Output Enable 2 [OE2]	OE
Output Enable 3 [OE3]	OE
Output Enable 4 [OE4]	OE
Output Enable 5 [OE5]	OE
Clock Enable 0 [CE0]	CE, CLK
Clock Enable 1 [CE1]	CE, OE
Clock Enable 2 [CE2]	CE, CLK
Clock Enable 3 [CE3]	CE, OE
Clock Enable 4 [CE4]	CE, CLR
Clock Enable 5 [CE5]	CE, CLR

In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, fast global signals, or row global signals. Figure 28 shows the IOE in bidirectional configuration.

Figure 30. APEX II IOE in DDR Output I/O Configuration



The APEX II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations.

APEX II I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM at 167 MHz (334 Mbps). The negative-edge-clocked OE register is used to hold the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements. QDR SRAMs are also supported with DDR I/O pins on separate read and write ports.

Bus Hold

Each APEX II device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signal is present, the bus-hold feature eliminates the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. The bus-hold feature should also be disabled if open-drain outputs are used with the GTL+ I/O standard.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ. Table 41 on page 74 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each APEX II device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the bank that the output pin resides in.

Dedicated Fast I/O Pins

APEX II devices incorporate dedicated bidirectional pins for signals with high internal fanout, such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and can drive the four global fast lines throughout the device, ideal for fast clock, clock enable, preset, clear, or high fanout logic signal distribution. The dedicated fast I/O pins have one output register and one OE register, but they do not have input registers. The dedicated fast lines can also be driven by a LE local interconnect to generate internal global signals.

Table 10 describes the I/O standards supported by APEX II devices.

Table 10. APEX II Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	N/A	1.5	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

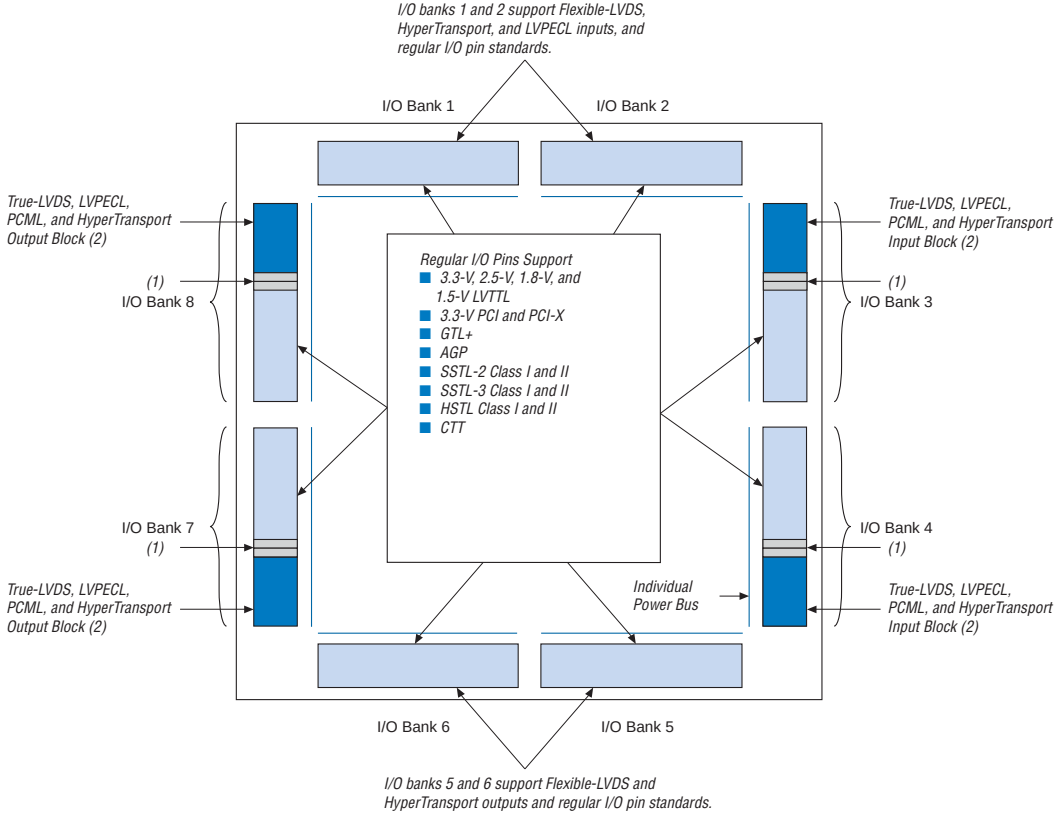
Note to Table 10:

(1) Differential HSTL is only supported on the eight dedicated global clock pins and four dedicated high-speed PLL clock pins.

For more information on I/O standards supported by APEX II devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

APEX II devices contain eight I/O banks, as shown in Figure 31. Two blocks within the right I/O banks contain circuitry to support high-speed True-LVDS, LVPECL, PCML, and HyperTransport inputs, and another two blocks within the left I/O banks support high-speed True-LVDS, LVPECL, PCML, and HyperTransport outputs. All other standards are supported by all I/O banks.

Figure 31. APEX II I/O Banks



Notes to Figure 31:

(1) For more information on placing I/O pins within LVDS blocks, refer to the "High-Speed Interface Pin Location" section in *Application Note 166 (Using High-Speed I/O Standards in APEX II Devices)*.

(2) If the True-LVDS pins or the Flexible-LVDS pins are not used for high-speed differential signalling, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V. However, True-LVDS pins do not support the HSTL Class II output.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level to support any one of the terminated standards (such as SSTL-3) independently.

Pre-programmed CDS may also be used to resolve clock-to-data skew greater than 50% of the bit period. However, internal logic must be used to implement the byte alignment circuitry for this operation.

Flexible-LVDS I/O Pins

A subset of pins in the top two I/O banks supports interfacing with Flexible-LVDS, LVPECL, and HyperTransport inputs. These Flexible-LVDS input pins include dedicated LVDS, LVPECL, and HyperTransport input buffers. A subset of pins in the bottom two I/O banks supports interfacing with Flexible-LVDS and HyperTransport outputs. These Flexible-LVDS output pins include dedicated LVDS and HyperTransport output buffers. The Flexible-LVDS pins do not require any external components except for 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization/deserialization circuitry; therefore, internal logic is used to perform serialization/deserialization functions.

The EP2A15 and EP2A25 devices support 56 input and 56 output Flexible-LVDS channels. The EP2A40 and larger devices support 88 input and 88 output Flexible-LVDS channels. All APEX II devices support the Flexible-LVDS interface up to 400 Mbps (DDR) per channel. Flexible-LVDS pins along with the True-LVDS pins provide up to 144-Gbps total device bandwidth. Table 13 shows the Flexible-LVDS timing specification.

Table 13. APEX II Flexible-LVDS Timing Specification

Symbol	Timing Parameter Definition	Speed Grade						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Data Rate	Maximum operating speed		400		311		311	Mbps
TCCS	Transmitter channel-to-channel skew		700		900		900	ps
SW	Receiver sampling window	1,100		1,400		1,400		ps

MultiVolt I/O Interface

The APEX II architecture supports the MultiVolt I/O interface feature, which allows APEX II devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.
(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.
(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.
(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Table 17. APEX II JTAG Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP2A15	1,524
EP2A25	1,884
EP2A40	2,328
EP2A70	3,228

Table 18. 32-Bit APEX II Device IDCODE				
Device	**IDCODE (32 Bits)** *(1)*			
	Version (4 Bits)	**Part Number (16 Bits)**	**Manufacturer Identity (11 Bits)**	**1 (1 Bit)** *(2)*
EP2A15	0000	1100 0100 0000 0000	000 0110 1110	1
EP2A25	0000	1100 0110 0000 0000	000 0110 1110	1
EP2A40	0000	1101 0000 0000 0000	000 0110 1110	1
EP2A70	0000	1110 0000 0000 0000	000 0110 1110	1

Notes to Tables 17 and 18:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 36 shows the timing requirements for the JTAG signals.

Figure 36. APEX II JTAG Waveforms

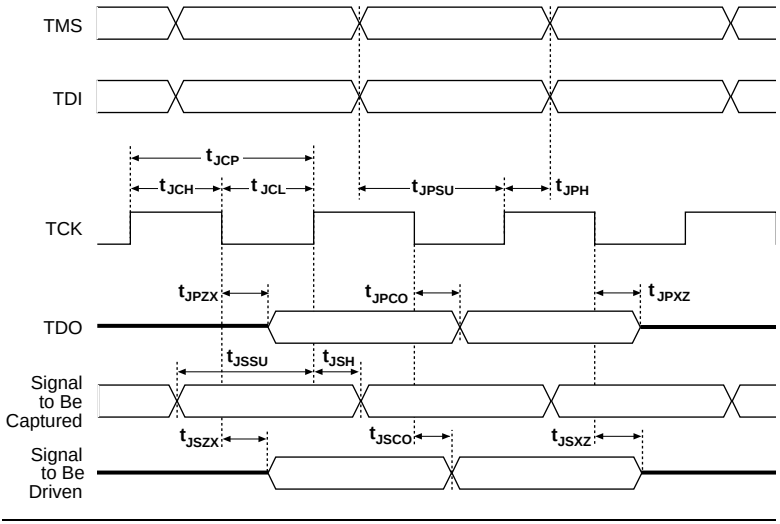


Table 19 shows the JTAG timing parameters and values for APEX II devices.

Table 19. APEX II JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

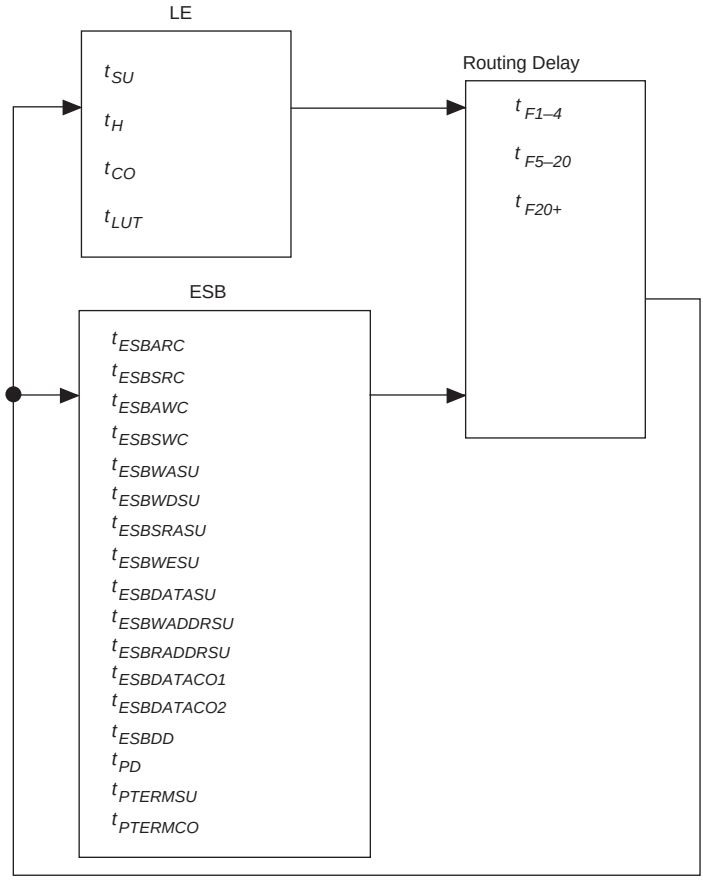
Table 42. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		850 *(1)*	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output Offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX II devices)		90	100	110	Ω

Table 43. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.3	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage		V_{CCIO} – 0.6		V_{CCIO} – 0.3	V
V_{OH}	High-level output voltage		V_{CCIO}		V_{CCIO} – 0.3	V
V_T	Output termination voltage			V_{CCIO}		V
V_{OD}	Differential output voltage		300	450	600	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
R_O	Output load			100		Ω
R_L	Receiver differential input resistor		45	50	55	Ω

Figure 41. f_{MAX} Timing Model



Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 63. EP2A40 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	0.89		1.33		1.88		ns
t_{CL}	0.89		1.33		1.88		ns
t_{CLRP}	0.12		0.14		0.16		ns
t_{PREP}	0.12		0.14		0.16		ns
t_{ESBCH}	0.89		1.33		1.88		ns
t_{ESBCL}	0.89		1.33		1.88		ns
t_{ESBWP}	1.05		1.20		1.38		ns
t_{ESBRP}	0.78		0.90		1.03		ns

Table 64. EP2A70 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.30		0.34		0.39		ns
t_{H}	0.30		0.34		0.39		ns
t_{CO}		0.22		0.25		0.29	ns
t_{LUT}		0.66		0.76		0.87	ns

Table 73. EP2A40 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.00		2.16		2.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.96	2.00	5.29	2.00	5.64	ns
t_{XZ}		7.04		7.59		8.19	ns
t_{ZX}		7.04		7.59		8.19	ns
$t_{INSUPLL}$	1.20		1.31		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.66	0.50	2.87	0.50	3.09	ns
t_{XZPLL}		4.74		5.17		5.64	ns
t_{ZXPLL}		4.74		5.17		5.64	ns

Table 74. EP2A70 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.48		2.68		2.90		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.76	2.00	5.12	2.00	5.51	ns
t_{XZ}		5.68		6.19		6.76	ns
t_{ZX}		5.68		6.19		6.76	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.52	0.50	2.74	0.50	2.98	ns
t_{XZPLL}		3.44		3.82		4.23	ns
t_{ZXPLL}		3.44		3.82		4.23	ns