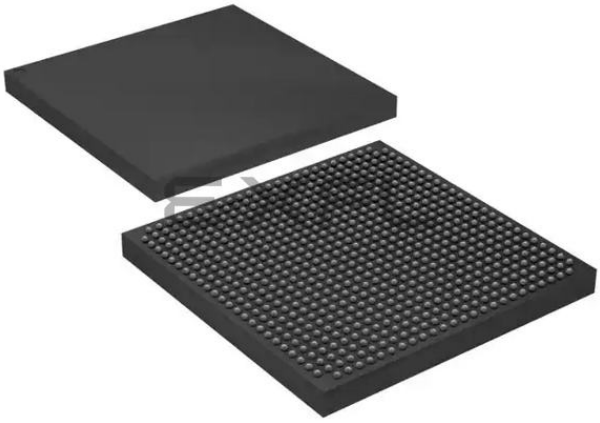


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	425984
Number of I/O	492
Number of Gates	1900000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2a15f672c9

Table 1. APEX II Device Features

Feature	EP2A15	EP2A25	EP2A40	EP2A70
Maximum gates	1,900,000	2,750,000	3,000,000	5,250,000
Typical gates	600,000	900,000	1,500,000	3,000,000
LEs	16,640	24,320	38,400	67,200
RAM ESBs	104	152	160	280
Maximum RAM bits	425,984	622,592	655,360	1,146,880
True-LVDS channels	36 *(1)*	36 *(1)*	36 *(1)*	36 *(1)*
Flexible-LVDS™ channels *(2)*	56	56	88	88
True-LVDS PLLs *(3)*	4	4	4	4
General-purpose PLL outputs *(4)*	8	8	8	8
Maximum user I/O pins	492	612	735	1,060

Notes to Table 1:

(1) Each device has 36 input channels and 36 output channels.
(2) EP2A15 and EP2A25 devices have 56 input and 56 output channels; EP2A40 and EP2A70 devices have 88 input and 88 output channels.
(3) PLL: phase-locked loop. True-LVDS PLLs are dedicated to implement True-LVDS functionality.
(4) Two internal outputs per PLL are available. Additionally, the device has one external output per PLL pair (two external outputs per device).

…and More Features

- I/O features
  - Up to 380 Gbps of I/O capability
  - 1-Gbps True-LVDS, LVPECL, PCML, and HyperTransport support on 36 input and 36 output channels that feature clock synchronization circuitry and independent clock multiplication and serialization/deserialization factors
  - Common networking and communications bus I/O standards such as RapidIO, CSIX, Utopia IV, and POS-PHY Level 4 enabled
  - 400-megabits per second (Mbps) Flexible-LVDS and HyperTransport support on up to 88 input and 88 output channels (input channels also support LVPECL)
  - Support for high-speed external memories, including ZBT, QDR, and DDR SRAM, and SDR and DDR SDRAM
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Compliant with 133-MHz PCI-X specifications
  - Support for other advanced I/O standards, including AGP, CTT, SSTL-3 and SSTL-2 Class I and II, GTL+, and HSTL Class I and II
  - Six dedicated registers in each I/O element (IOE): two input registers, two output registers, and two output-enable registers
  - Programmable bus hold feature
  - Programmable pull-up resistor on I/O pins available during user mode

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. APEX II Package Sizes

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Pitch (mm)	1.00	1.27	1.00	1.00
Area (mm^2)	729	1,225	1,089	1,600
Length × Width (mm × mm)	27 × 27	35 × 35	33 × 33	40 × 40

Table 3. APEX II Package Options & I/O Pin Count *Notes (1), (2)*

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2A15	492	492		
EP2A25	492	536		
EP2A40	492	536	735	
EP2A70		536		1,060

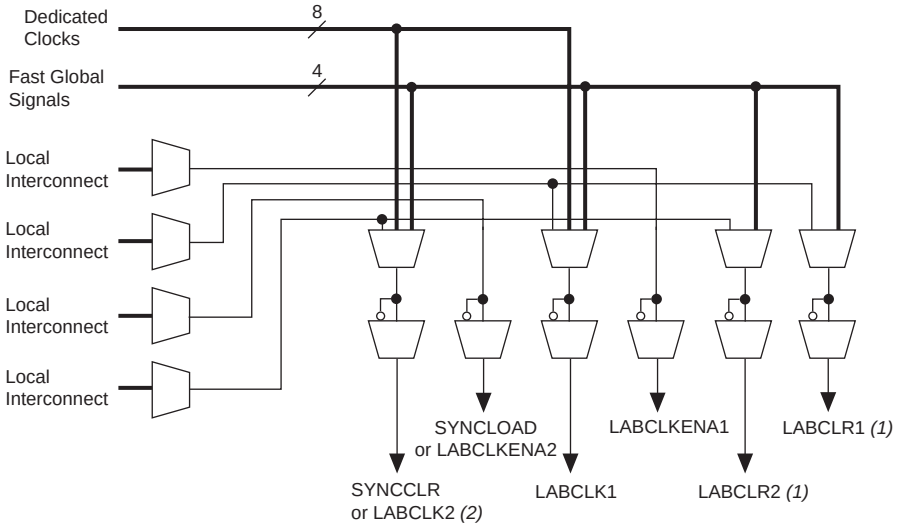
Notes to Table 3:

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

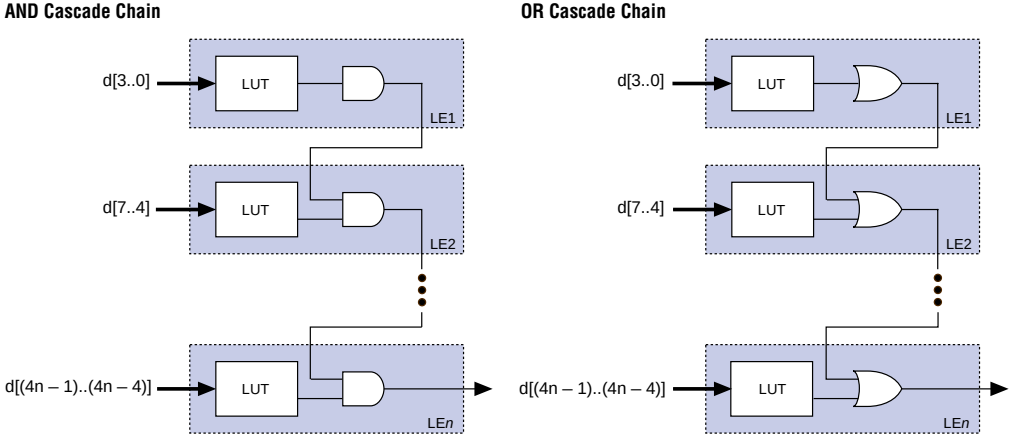
The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Cascade Chain

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX II Cascade Chain



A column line can be directly driven by the LEs, IOEs, or ESBs in that column. Row IOEs can drive a column line on a device's left or right edge. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

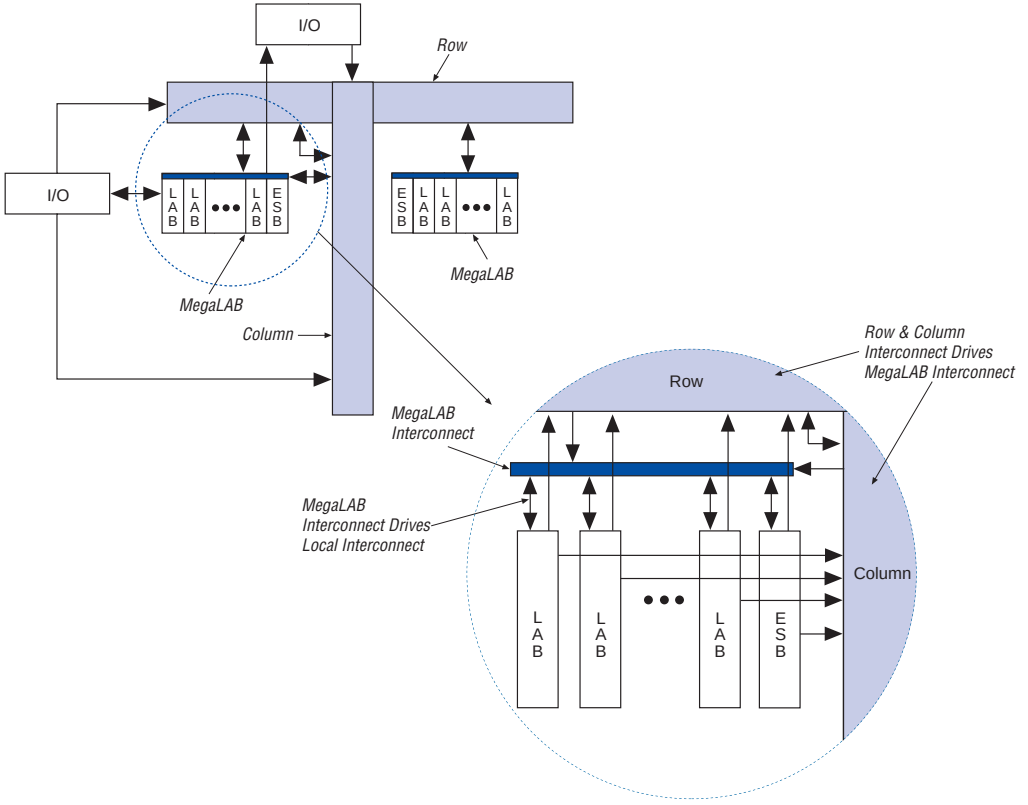


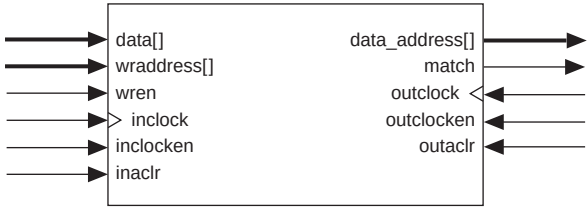
Figure 11 shows the intersection of a row and column interconnect and how these forms of interconnects and LEs drive each other.

Content-Addressable Memory

APEX II devices can implement CAM in ESBs. CAM can be thought of as the inverse of RAM. RAM stores data in a specific location; when the system submits an address, the RAM block provides the data. Conversely, when the system submits data to CAM, the CAM block provides the address where the data is found. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. CAM is ideally suited for applications such as Ethernet address lookup, data compression, pattern recognition, cache tags, fast routing table lookup, and high-bandwidth address filtering. Figure 21 shows the CAM block diagram.

Figure 21. CAM Block Diagram



The APEX II on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX II device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements a 32-word, 32-bit CAM. Wider or deeper CAM, such as a 32-word, 64-bit or 128-word, 32-bit block, can be implemented by combining multiple CAM blocks with some ancillary logic implemented in LEs. The Quartus II software automatically combines ESBs and LEs to create larger CAM blocks.

CAM supports writing “don’t care” bits into words of the memory. The don’t-care bit can be used as a mask for CAM comparisons; any bit set to don’t-care has no effect on matches.

Figure 26. Row IOE Connection to the Interconnect

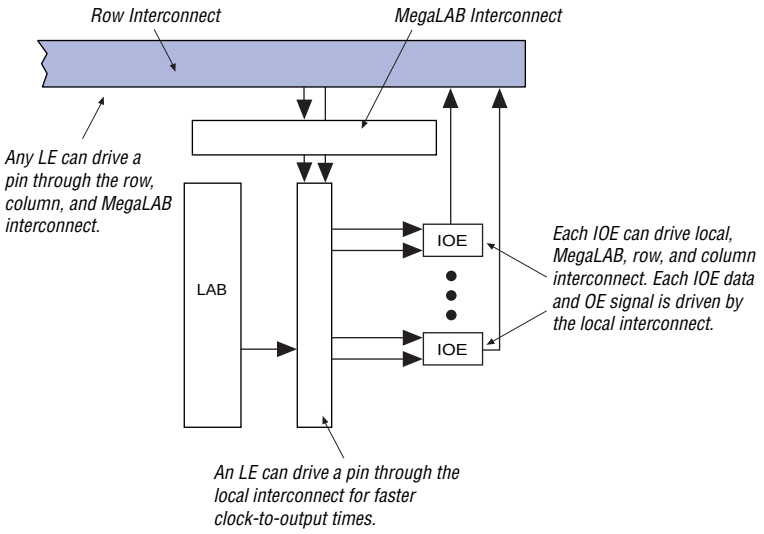
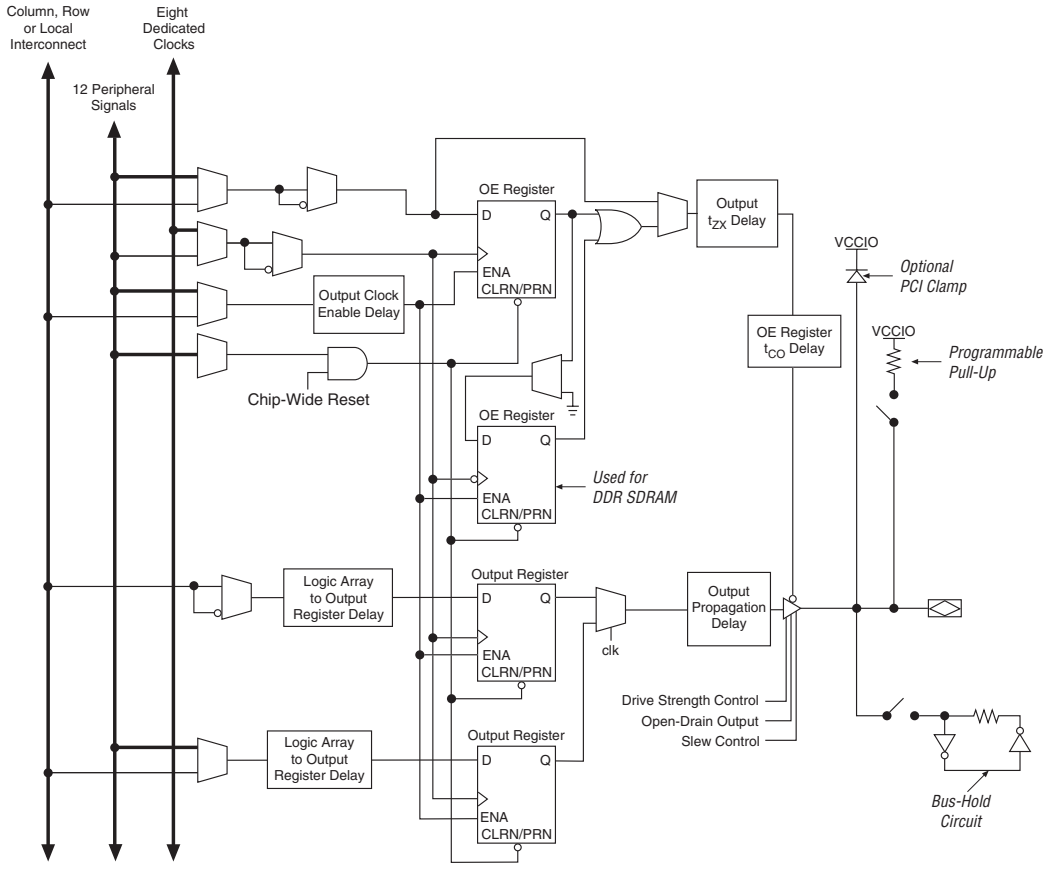


Figure 27 shows how a column IOE connects to the interconnect.

Figure 30. APEX II IOE in DDR Output I/O Configuration



The APEX II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations.

APEX II I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM at 167 MHz (334 Mbps). The negative-edge-clocked OE register is used to hold the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements. QDR SRAMs are also supported with DDR I/O pins on separate read and write ports.

Table 10 describes the I/O standards supported by APEX II devices.

Table 10. APEX II Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	N/A	1.5	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Note to Table 10:

(1) Differential HSTL is only supported on the eight dedicated global clock pins and four dedicated high-speed PLL clock pins.

For more information on I/O standards supported by APEX II devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

APEX II devices contain eight I/O banks, as shown in Figure 31. Two blocks within the right I/O banks contain circuitry to support high-speed True-LVDS, LVPECL, PCML, and HyperTransport inputs, and another two blocks within the left I/O banks support high-speed True-LVDS, LVPECL, PCML, and HyperTransport outputs. All other standards are supported by all I/O banks.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.
(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.
(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.
(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Figure 36. APEX II JTAG Waveforms

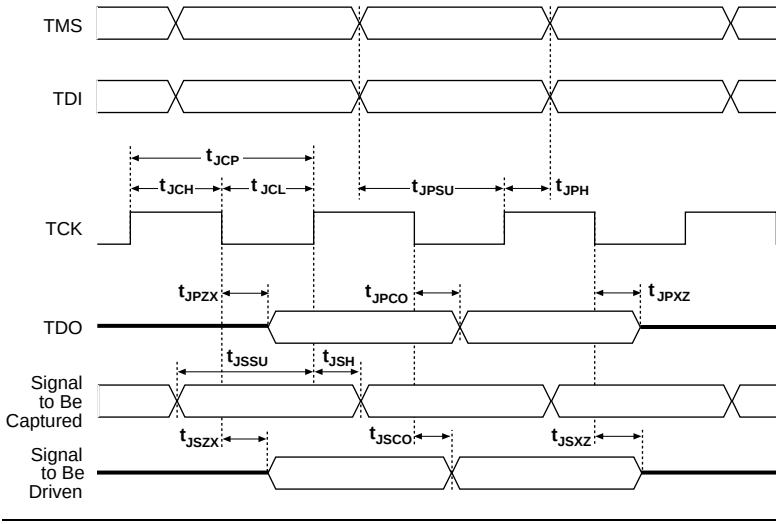


Table 19 shows the JTAG timing parameters and values for APEX II devices.

Table 19. APEX II JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Tables 20 through 41 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 20. APEX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 21. APEX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 22. APEX II Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 23. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–5	5	µA
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 24. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 37. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –8 mA *(10)*			0.4	V

Table 38. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –16 mA *(10)*			0.4	V

Table 39. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Figure 43. Dual-Port RAM Timing Microparameter Waveform

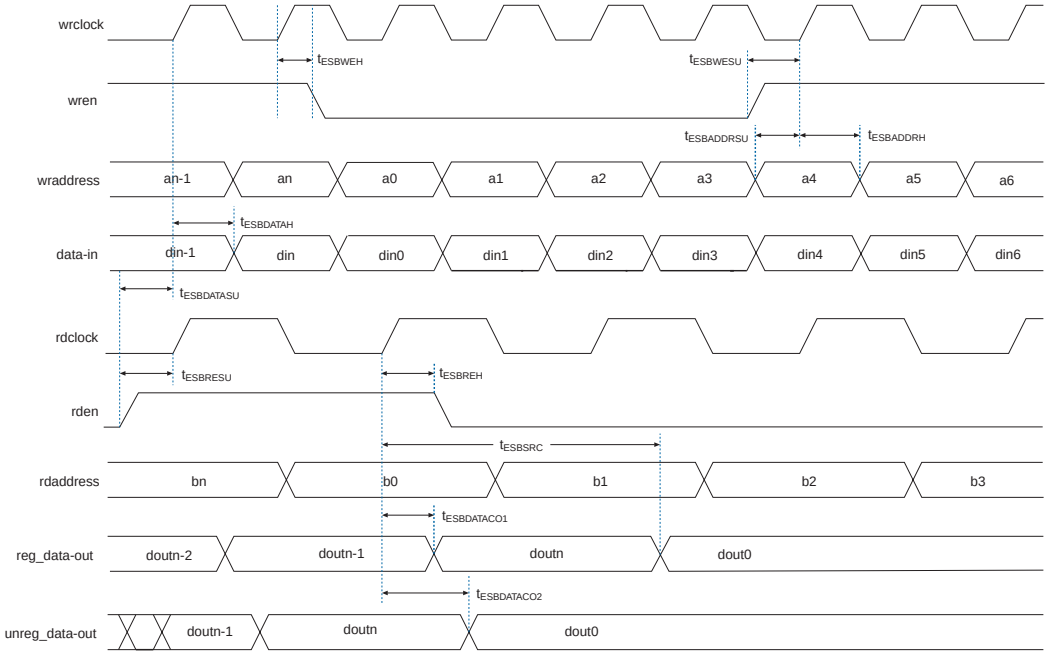


Table 49. APEX II f_{MAX} Routing Delays	
Symbol	**Parameter**
t_{F1-4}	Fan-out delay estimate using local interconnect; use to estimate routing delay for a signal with fan-out of 1 to 4
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect; use to estimate routing delay for a signal with fan-out of 5 to 20
t_{F20+}	Fan-out delay estimate using FastTrack interconnect; use to estimate routing delay for a signal with fan-out greater than 20

Table 50. APEX II Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Table 51. APEX II External Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
t_{XZ}	Clock-to-output buffer disable delay	
t_{ZX}	Clock-to-output buffer enable delay	Slow slew rate = OFF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF
t_{XZPLL}	PLL clock-to-output buffer disable delay	
t_{ZXPLL}	PLL clock-to-output buffer enable delay	Slow slew rate = OFF

Note to Table 51:

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 61. EP2A40 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.28		2.62		3.01	ns
t_{ESBSRC}		2.23		2.56		2.95	ns
t_{ESBAWC}		3.13		3.60		4.13	ns
t_{ESBSWC}		2.76		3.18		3.65	ns
$t_{ESBWASU}$	1.19		1.37		1.57		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.44		1.66		1.91		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.88		2.17		2.49		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.60		1.85		2.12		ns
$t_{ESBDATASU}$	0.74		0.85		0.98		ns
$t_{ESBWADDRSU}$	0.82		0.94		1.08		ns
$t_{ESBRADDRSU}$	0.73		0.84		.97		ns
$t_{ESBDATACO1}$		1.09		1.25		1.44	ns
$t_{ESBDATACO2}$		1.73		1.99		2.29	ns
t_{ESBDD}		3.26		3.75		4.32	ns
t_{PD}		1.55		1.78		2.05	ns
$t_{PTERMSU}$	0.99		1.13		1.30		ns
$t_{PTERMCO}$		0.79		0.90		1.04	ns

Table 62. EP2A40 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.17		0.19		0.22		ns
t_{F5-20}	1.12		1.28		1.48		ns
t_{F20+}	1.49		1.72		1.98		ns

Revision History

The information contained in the *APEX II Programmable Logic Device Family Data Sheet* version 3.0 supersedes information published in previous versions. The following changes were made to the *APEX II Programmable Logic Device Family Data Sheet* version 3.0:

- Changed the value from 624 to 400 Mbps throughout the document.
- Deleted the pin count (612) for the EP2A25 device in the 1,020-pin FineLine BGA package (see Table 3).
- Added Table 13.
- Changed the maximum value of 3.6 to 2.4 in Table 20.
- Updated Tables 60 through 67 and Tables 72 through 75.
- Updated Figures 25, 28, and 30.
- Added *Note (1)* to Figure 13.
- Added Figure 43.

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