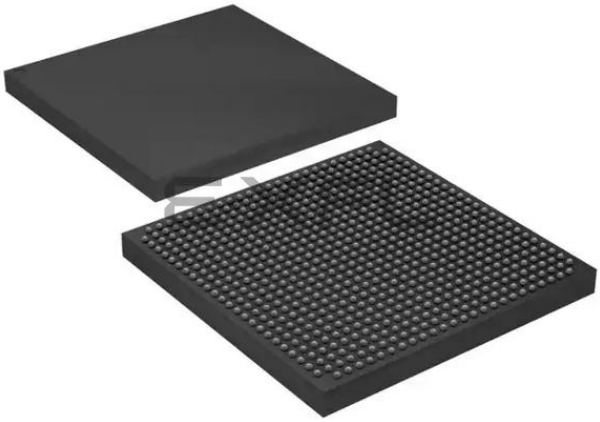

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1664
Number of Logic Elements/Cells	16640
Total RAM Bits	425984
Number of I/O	492
Number of Gates	1900000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2a15f672c9n

General Description

APEX II devices integrate high-speed differential I/O support using the True-LVDS interface. The dedicated serializer, deserializer, and CDS circuitry in the True-LVDS interface support the LVDS, LVPECL, HyperTransport, and PCML I/O standards. Flexible-LVDS pins located in regular user I/O banks offer additional differential support, increasing the total device bandwidth. This circuitry, together with enhanced IOEs and support for numerous I/O standards, allows APEX II devices to meet high-speed interface requirements.

APEX II devices also include other high-performance features such as bidirectional dual-port RAM, CAM, general-purpose PLLs, and numerous global clocks.

Configuration

The logic, circuitry, and interconnects in the APEX II architecture are configured with CMOS SRAM elements. APEX II devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs; APEX II devices can be configured on the board for the specific functionality required.

APEX II devices are configured at system power-up with data either stored in an Altera configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices, which configure APEX II devices via a serial data stream. The enhanced configuration devices can configure any APEX II device in under 100 ms. Moreover, APEX II devices contain an optimized interface that permits microprocessors to configure APEX II devices serially or in parallel, synchronously or asynchronously. This interface also enables microprocessors to treat APEX II devices as memory and to configure the device by writing to a virtual memory location, simplifying reconfiguration.

APEX II devices also support a new byte-wide, synchronous configuration scheme at speeds of up to 66 MHz using EPC16 configuration devices or a microprocessor. This parallel configuration reduces configuration time by using eight data lines to send configuration data versus one data line in serial configuration.

APEX II devices support multi-voltage configuration; device configuration can be performed at 3.3 V and 2.5 V or 1.8 V.

Figure 1. APEX II Device Block Diagram

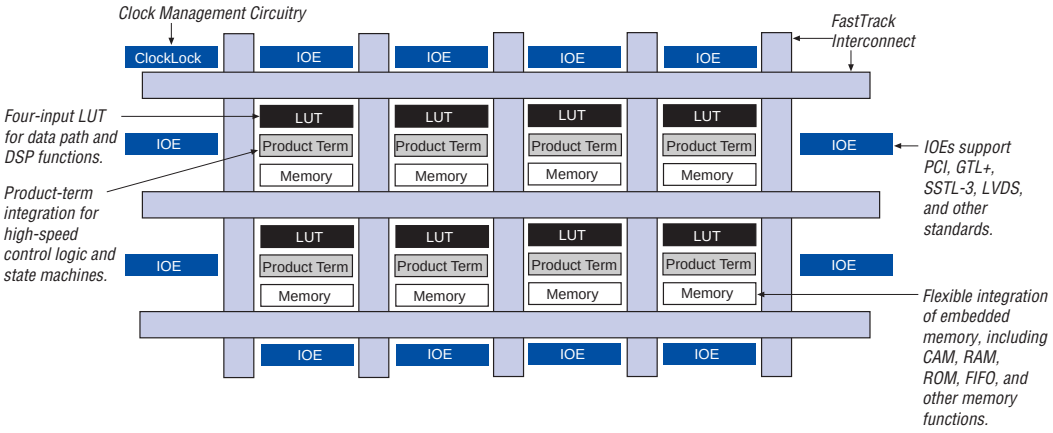


Table 4 lists the resources available in APEX II devices.

Table 4. APEX II Device Resources

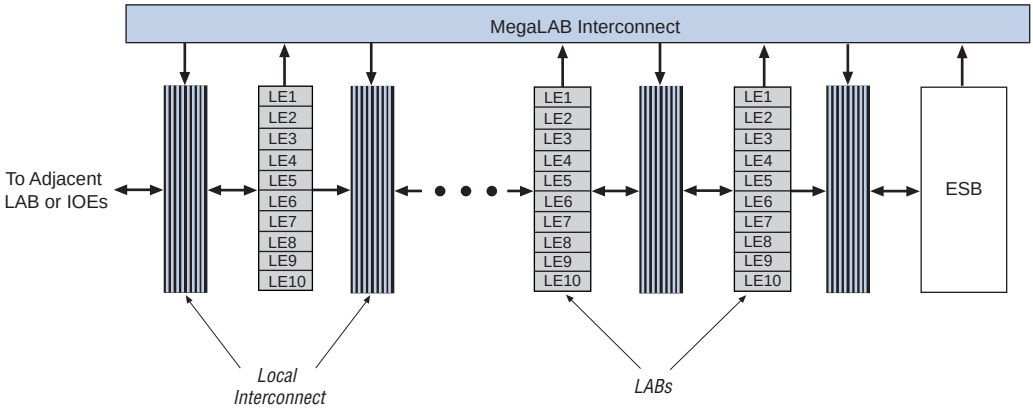
Device	MegaLAB Rows	MegaLAB Columns	ESBs
EP2A15	26	4	104
EP2A25	38	4	152
EP2A40	40	4	160
EP2A70	70	4	280

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



Logic Array Block

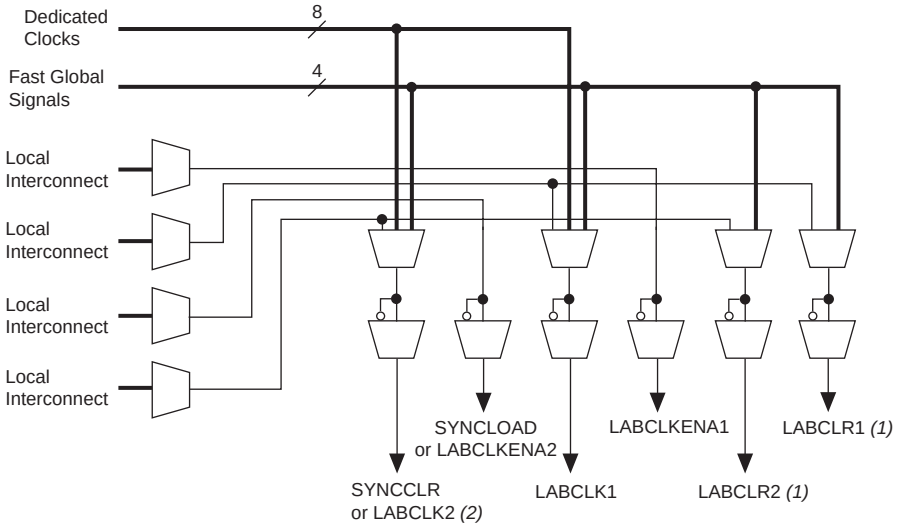
Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

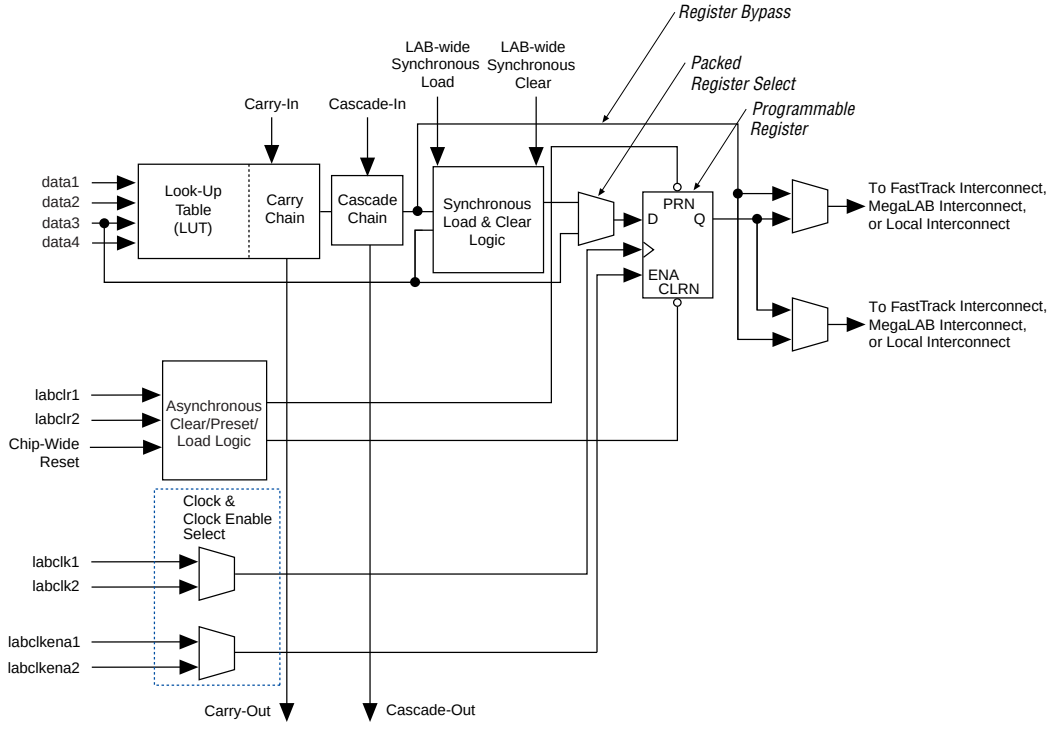
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

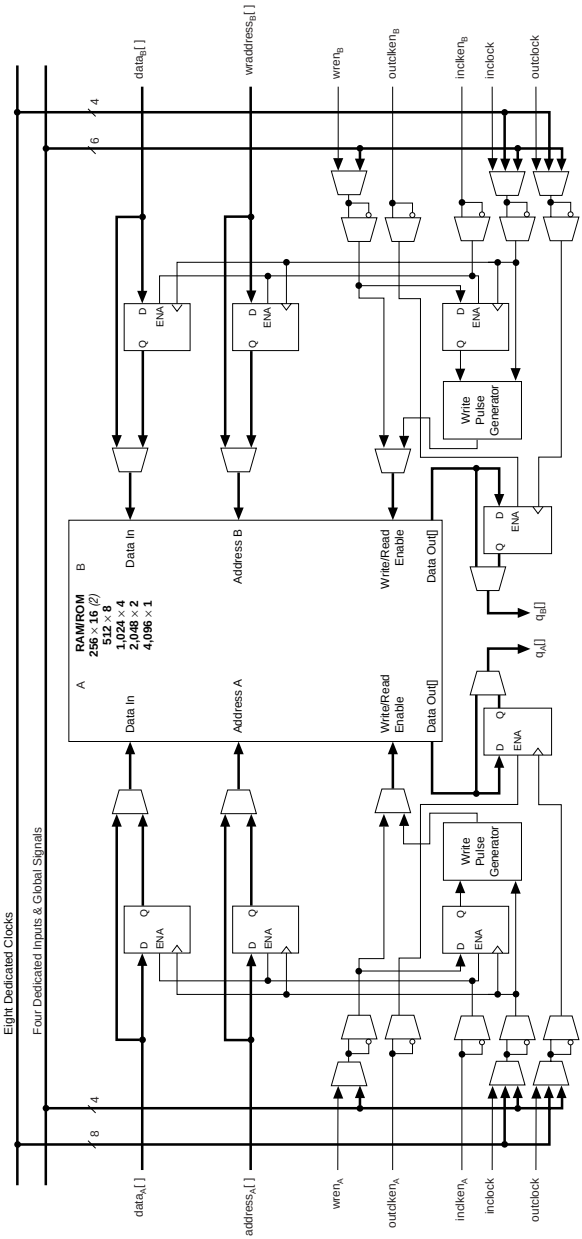
The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Figure 5. APEX II Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Figure 19. ESB in Input/Output Clock Mode *Note (1)*



Notes to Figure 19:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

(2) This configuration is not supported for bidirectional dual-port configuration.

If the same data is written into multiple locations in the memory, a CAM block can be used in multiple-match or fast multiple-match modes. The ESB outputs the matched data's locations as an encoded or unencoded address. In multiple-match mode, it takes two clock cycles to write into a CAM block. For reading, there are 16 outputs from each ESB at each clock cycle. Therefore, it takes two clock cycles to represent the 32 words from a single ESB port. In this mode, encoded and unencoded outputs are available. To implement the encoded version, the Quartus II software adds a priority encoder with LEs. Fast multiple-match is identical to the multiple match mode, however, it only takes one clock cycle to read from a CAM block and generate valid outputs. To do this, the entire ESB is used to represent 16 outputs. In fast multiple-match mode, the ESB can implement a maximum CAM block size of 16 words.

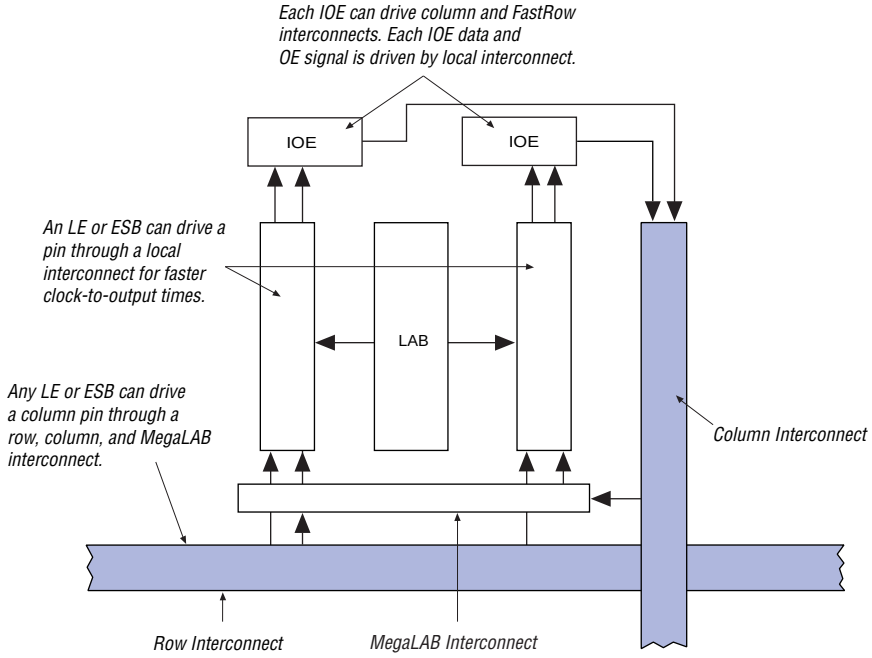
A CAM block can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When don't-care bits are used, a third clock cycle is required.

For more information on CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnects can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and synchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 27. Column IOE Connection to the Interconnect

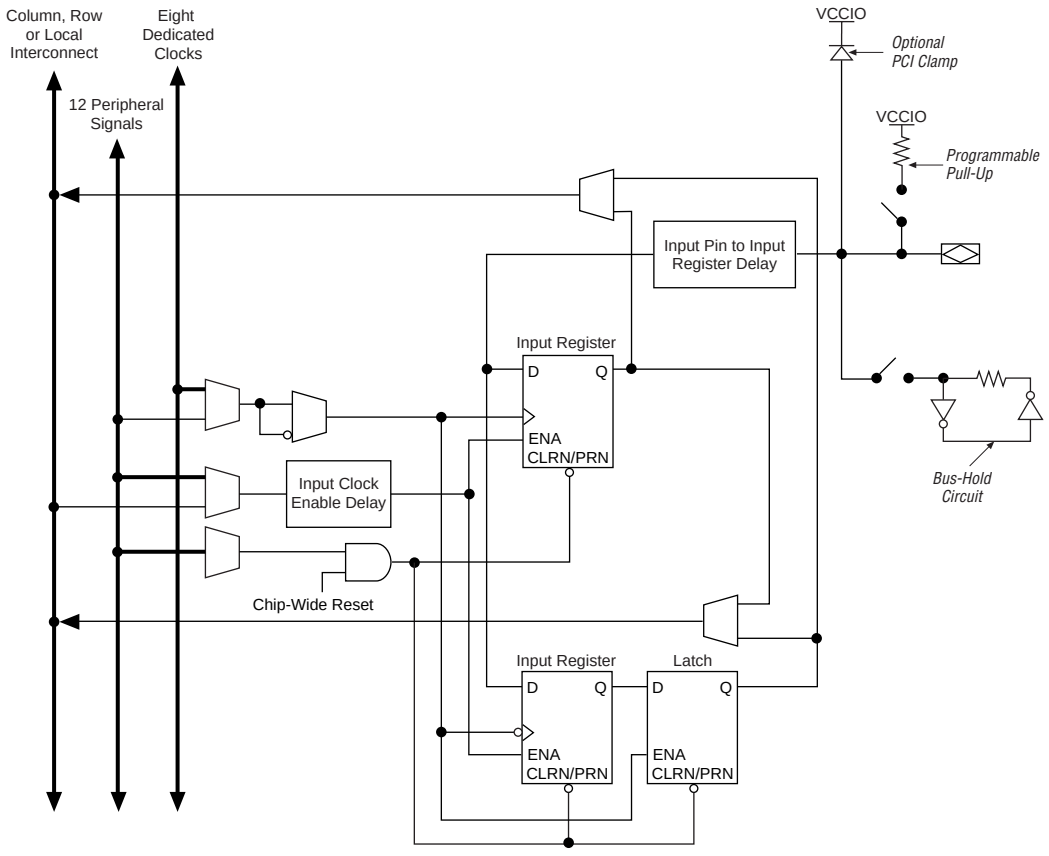


FastRow interconnects connect a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing.

APEX II devices have a peripheral control bus made up of 12 signals that drive the IOE control signals. The peripheral bus is composed of six output enables, `OE[5:0]` and six clock enables, `CE[5:0]`. These twelve signals can be driven from internal logic or from the Fast I/O signals. Table 7 lists the peripheral control signal destinations.

When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, APEX II device I/O pins also support interfacing with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) delay ensures that the t_{ZX} is greater than the clock-to-high-impedance time (t_{XZ}). Phase delay control of clocks to the OE/output and input registers using two general-purpose PLLs enable the APEX II device to meet ZBT t_{CO} and t_{SU} times.

Programmable Drive Strength

The output buffer for each APEX II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, 3.3-V GTL+, PCI, and PCI-X support a minimum setting. The minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 9 shows the possible settings for the I/O standards with drive strength control.

Advanced I/O Standard Support

APEX II device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5-V
- 1.8-V
- 2.5-V
- 3.3-V PCI
- 3.3-V PCI-X
- 3.3-V AGP (1×, 2×)
- LVDS
- LVPECL
- PCML
- HyperTransport
- GTL+
- HSTL class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- CTT
- Differential HSTL

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.
(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.
(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.
(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Note to Figure 35:

(1) *n* represents the prescale divider for the PLL input. *m* represents the multiplier. *k* and *v* represent the different post scale dividers for the two possible PLL outputs. *m* and *k* are integers that range from 1 to 160. *n* and *v* are integers that range from 1 to 16.

Advanced ClockBoost Multiplication & Division

APEX II PLLs include circuitry that provides clock synthesis for eight internal outputs and two external outputs using $m / (n \times$ output divider) scaling. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. The closed loop equation for Figure 35 gives an output frequency $f_{clock0} = (m / (n \times k))f_{IN}$ and $f_{clock1} = (m / (n \times v))f_{IN}$. These equations allow the multiplication or division of clocks by a programmable number. The Quartus II software automatically chooses the appropriate scaling factors according to the frequency, multiplication, and division values entered.

A single PLL in an APEX II device allows for multiple user-defined multiplication and division ratios that are not possible even with multiple delay-locked loops (DLLs). For example, if a frequency scaling factor of 3.75 is needed for a given input clock, a multiplication factor of 15 and a division factor of 4 can be entered. This advanced multiplication scaling can be performed with a single PLL, making it unnecessary to cascade PLL outputs.

External Clock Outputs

APEX II devices have two low-jitter external clocks available for external clock sources. Other devices on the board can use these outputs as clock sources.

There are three modes for external clock outputs.

- Zero Delay Buffer: The external clock output pin is phase aligned with the clock input pin for zero delay. Multiplication, programmable phase shift, and time delay shift are not allowed in this configuration. The MegaWizard interface for `altclklock` should be used to verify possible clock settings.
- External Feedback: The external feedback input pin is phase aligned with clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. This mode has the same restrictions as zero delay buffer mode.
- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX II devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX II devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX II devices support the JTAG instructions shown in Table 16.

Table 16. APEX II JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring an APEX II device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 16:

(1) Bus hold and weak pull-up features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The APEX II device instruction register length is 10 bits. The APEX II device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for APEX II devices.

Table 31. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(10)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(10)*			V_{TT} – 0.57	V

Table 32. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(10)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(10)*			V_{TT} – 0.76	V

Table 33. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(10)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(10)*			V_{TT} – 0.6	V

Table 44. LVPECL Specifications *Note (2)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		800		2,000	mV
V_{IH}	High-level input voltage		2,100		V_{CCIO}	mV
V_{OL}	Low-level output voltage		1,450		1,650	mV
V_{OH}	High-level output voltage		2,275		2,420	mV
V_{ID}	Differential input voltage		100	600	2,500	mV
V_{OD}	Differential output voltage		625	800	970	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps

Table 45. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage		380	600	820	mV
V_{OCM}	Output common mode voltage	R_{TT} = 100 Ω	500	600	700	mV
V_{ID}	Differential input voltage		300	600	900	mV
V_{ICM}	Input common mode voltage		450	600	750	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Notes to Tables 42 – 45:

(1) Maximum V_{OD} is measured under static conditions.

(2) When APEX II devices drive LVPECL signals, the APEX II LVPECL outputs must be terminated with a resistor network.

Capacitance

Table 46 and Figure 40 provide information on APEX II device capacitance.

Figure 41. f_{MAX} Timing Model

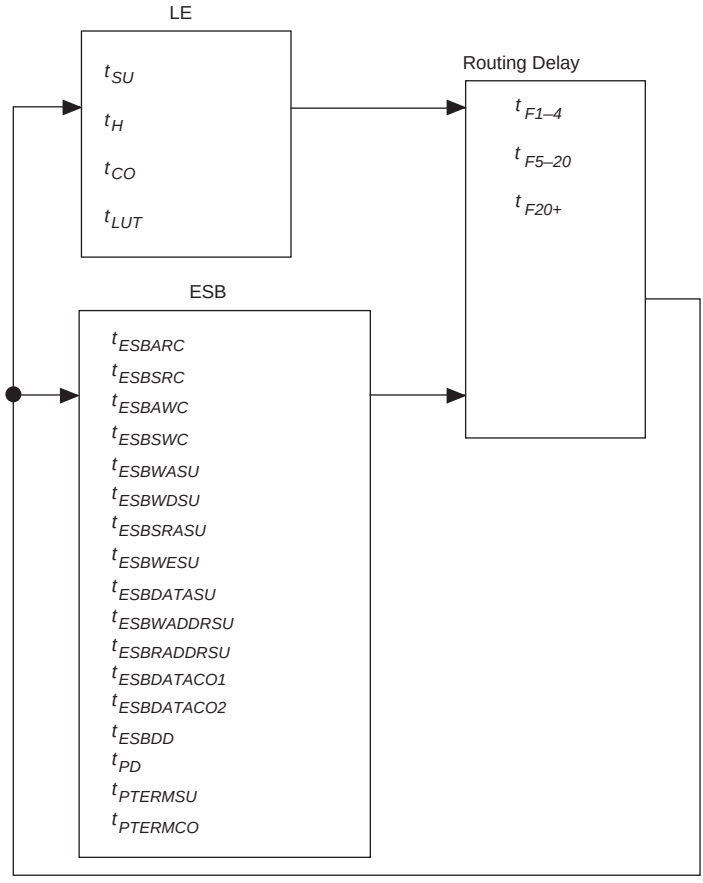


Table 59. EP2A25 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.50		2.12		ns
t_{CL}	1.00		1.50		2.12		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.50		2.12		ns
t_{ESBCL}	1.00		1.50		2.12		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 60. EP2A40 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.26		0.29		ns
t_{H}	0.22		0.26		0.29		ns
t_{CO}		0.16		0.18		0.21	ns
t_{LUT}		0.48		0.55		0.63	ns

Table 69. EP2A15 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.16		2.34		2.53		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.36	2.00	4.75	2.00	5.18	ns
t_{XZ}		5.57		6.24		6.97	ns
t_{ZX}		5.57		6.24		6.97	ns
$t_{INSUPLL}$	1.24		1.37		1.52		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.90	0.50	3.16	0.50	3.45	ns
t_{XZPLL}		4.12		4.65		5.23	ns
t_{ZXPLL}		4.12		4.65		5.23	ns

Table 70. EP2A25 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.92		2.08		2.26		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.29	2.00	4.62	2.00	4.98	ns
t_{XZ}		5.24		5.73		6.26	ns
t_{ZX}		5.24		5.73		6.26	ns
$t_{INSUPLL}$	1.17		1.27		1.40		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.61	0.50	2.83	0.50	3.07	ns
t_{XZPLL}		3.55		3.93		4.35	ns
t_{ZXPLL}		3.55		3.93		4.35	ns