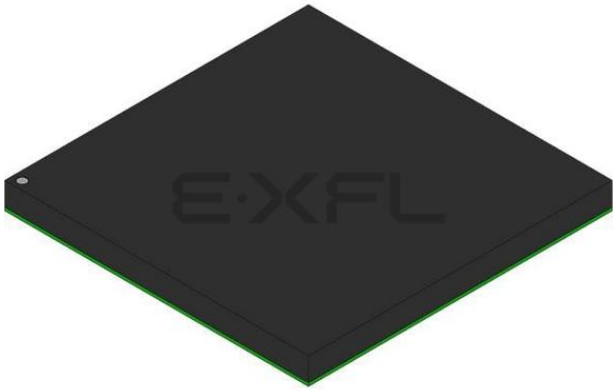

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	540
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	724-BBGA, FCBGA
Supplier Device Package	724-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a25b724c7

Table 1. APEX II Device Features

Feature	EP2A15	EP2A25	EP2A40	EP2A70
Maximum gates	1,900,000	2,750,000	3,000,000	5,250,000
Typical gates	600,000	900,000	1,500,000	3,000,000
LEs	16,640	24,320	38,400	67,200
RAM ESBs	104	152	160	280
Maximum RAM bits	425,984	622,592	655,360	1,146,880
True-LVDS channels	36 *(1)*	36 *(1)*	36 *(1)*	36 *(1)*
Flexible-LVDS™ channels *(2)*	56	56	88	88
True-LVDS PLLs *(3)*	4	4	4	4
General-purpose PLL outputs *(4)*	8	8	8	8
Maximum user I/O pins	492	612	735	1,060

Notes to Table 1:

(1) Each device has 36 input channels and 36 output channels.
(2) EP2A15 and EP2A25 devices have 56 input and 56 output channels; EP2A40 and EP2A70 devices have 88 input and 88 output channels.
(3) PLL: phase-locked loop. True-LVDS PLLs are dedicated to implement True-LVDS functionality.
(4) Two internal outputs per PLL are available. Additionally, the device has one external output per PLL pair (two external outputs per device).

…and More Features

- I/O features
  - Up to 380 Gbps of I/O capability
  - 1-Gbps True-LVDS, LVPECL, PCML, and HyperTransport support on 36 input and 36 output channels that feature clock synchronization circuitry and independent clock multiplication and serialization/deserialization factors
  - Common networking and communications bus I/O standards such as RapidIO, CSIX, Utopia IV, and POS-PHY Level 4 enabled
  - 400-megabits per second (Mbps) Flexible-LVDS and HyperTransport support on up to 88 input and 88 output channels (input channels also support LVPECL)
  - Support for high-speed external memories, including ZBT, QDR, and DDR SRAM, and SDR and DDR SDRAM
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Compliant with 133-MHz PCI-X specifications
  - Support for other advanced I/O standards, including AGP, CTT, SSTL-3 and SSTL-2 Class I and II, GTL+, and HSTL Class I and II
  - Six dedicated registers in each I/O element (IOE): two input registers, two output registers, and two output-enable registers
  - Programmable bus hold feature
  - Programmable pull-up resistor on I/O pins available during user mode

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up / down control, synchronous clear, and synchronous load options. The counter enable and synchronous up / down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data's location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 21 and 22 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 22. Encoded CAM Address Outputs

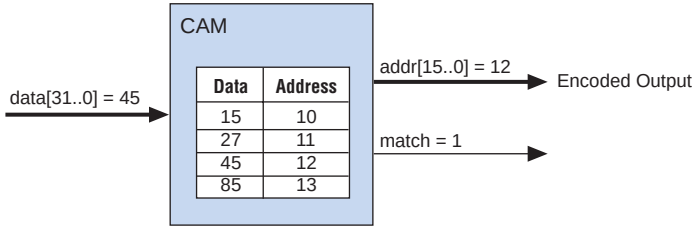
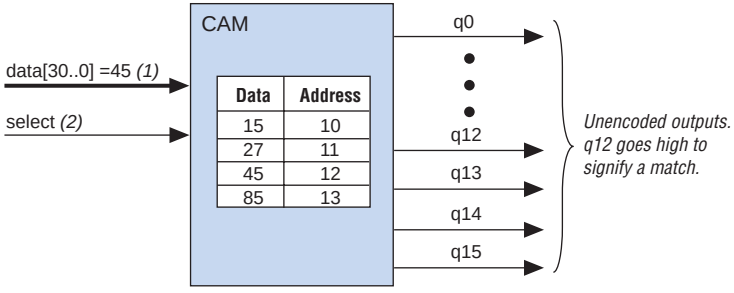


Figure 23. Unencoded CAM Address Outputs



Notes to Figures 22 and 23:

(1) For an unencoded output, the ESB only supports 31 input data bits. One input bit is used by the `select` line to choose one of the two banks of 16 outputs.

(2) If the `select` input is a 1, then CAM outputs odd words between 1 through 15. If the `select` input is a 0, CAM outputs even words between 0 through 14.

In single-match mode, it takes two clock cycles to write into CAM, but only one clock cycle to read from CAM. In this mode, both encoded and unencoded outputs are available without external logic. Single-match mode is better suited for designs without duplicate data in the memory.

Figure 26. Row IOE Connection to the Interconnect

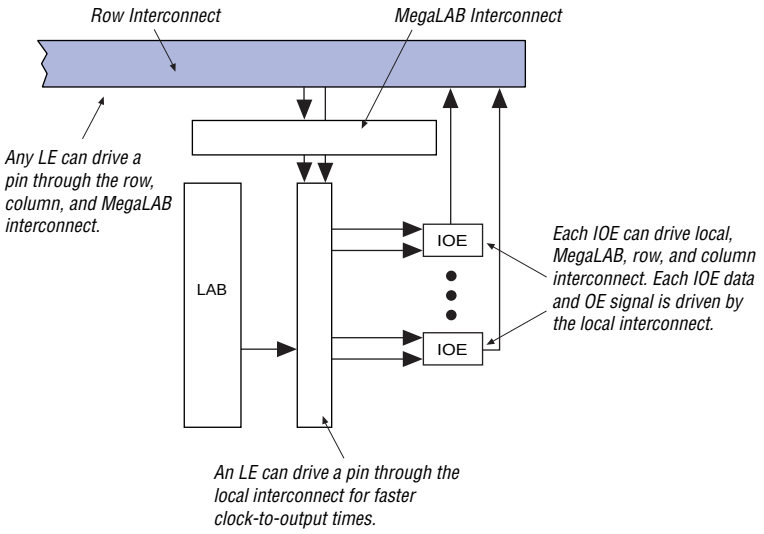


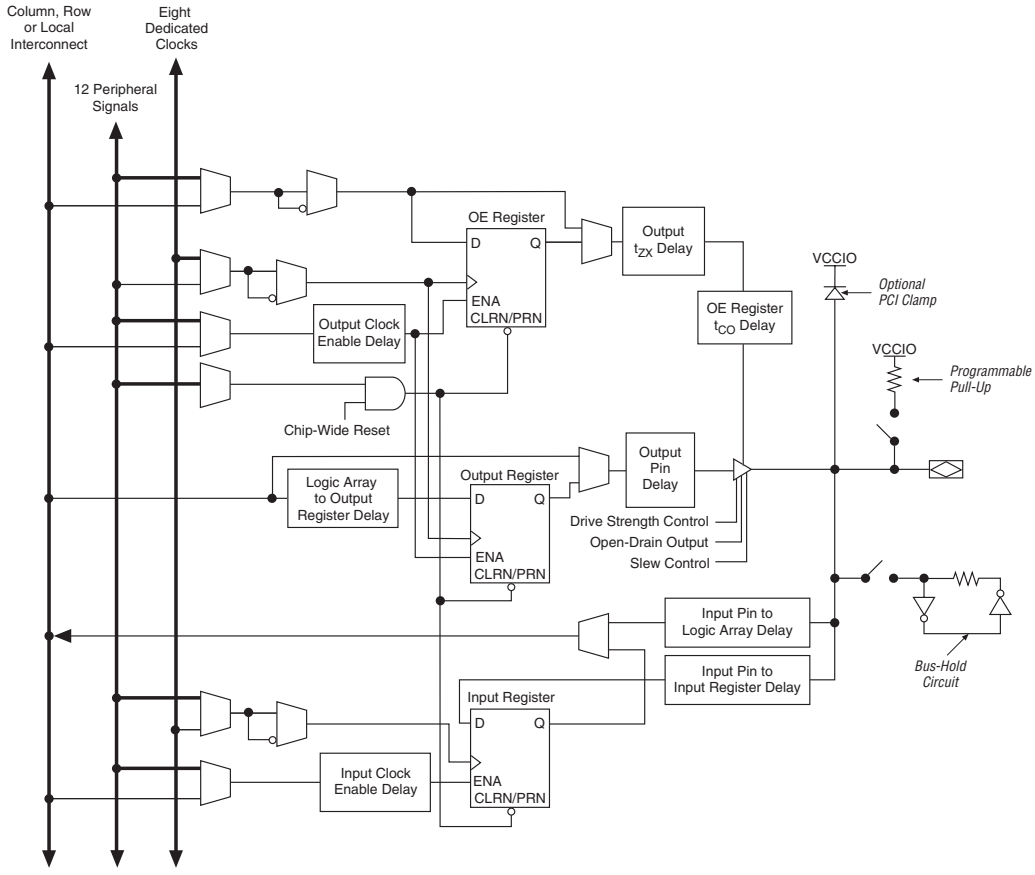
Figure 27 shows how a column IOE connects to the interconnect.

Table 7. Peripheral Control Bus Destinations

Peripheral Bus	I/O Control Signal
Output Enable 0 [OE0]	OE
Output Enable 1 [OE1]	OE
Output Enable 2 [OE2]	OE
Output Enable 3 [OE3]	OE
Output Enable 4 [OE4]	OE
Output Enable 5 [OE5]	OE
Clock Enable 0 [CE0]	CE, CLK
Clock Enable 1 [CE1]	CE, OE
Clock Enable 2 [CE2]	CE, CLK
Clock Enable 3 [CE3]	CE, OE
Clock Enable 4 [CE4]	CE, CLR
Clock Enable 5 [CE5]	CE, CLR

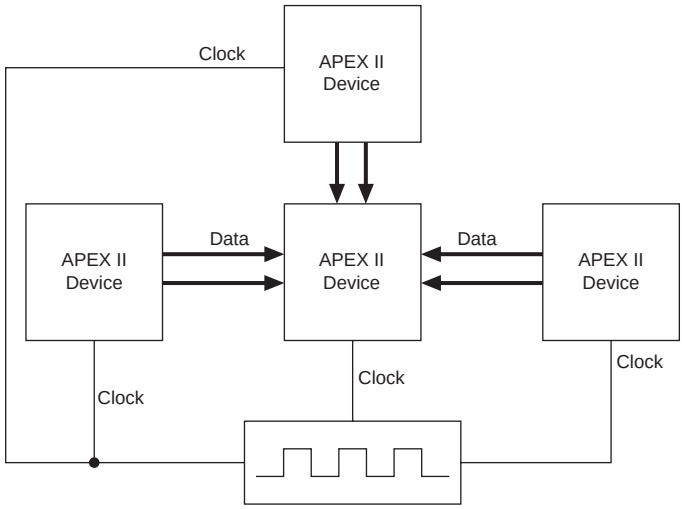
In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, fast global signals, or row global signals. Figure 28 shows the IOE in bidirectional configuration.

Figure 28. APEX II IOE in Bidirectional I/O Configuration



The APEX II IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

Figure 34. Multi-Bit CDS Supports N:1 Topology



When using multi-bit CDS, the *J* and *W* factors do not need to be the same value. The byte boundary cannot be distinguished with multi-bit CDS patterns (see Table 12). Therefore, the byte must be aligned using internal logic. Table 12 shows the possible training patterns for multi-bit CDS. Either pattern can be used.

Table 12. Multi-Bit CDS Patterns

W Factor	J Factor	Multi-Bit CDS Pattern
1, 2, 4 to 10	4 to 10	3 × J-bits of `010101` pattern
1, 2, 4 to 10	4 to 10	3 × J-bits of `101010` pattern

Pre-Programmed CDS

When the fixed clock-to-data skew is known, CDS can be pre-programmed into the device during configuration. If CDS is pre-programmed into the device, the training patterns do not need to be transmitted to the receiver channels. The resolution of each pre-programmed setting is 25% of the data period, to compensate for skew up to ±50% of the data period.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 25. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA		0.7	V

Table 26. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 27. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 34. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(10)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(10)*			V_{TT} – 0.8	V

Table 35. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 36. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 40. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	0 < V_{IN} < V_{CCIO}	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ð V_{OUT} ð V_{CCIO}	–10		10	µA

Table 41. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Units
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)			30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)			–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}				200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}				–200		–300		–500	µA

Notes to Tables 20 – 41:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Conditions beyond those listed in Table 20 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to - 2 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, RapidIO, and PCML are shown in parentheses.
(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(7) Typical values are for T_A = 25° C, V_{CCINT} = 1.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.
(8) This value is specified for normal device operation. The value may vary during power-up.
(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.
(10) Drive strength is programmable according to values in Table 9 on page 48.
(11) V_{REF} specifies the center point of the switching range.

Table 42. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		850 *(1)*	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output Offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX II devices)		90	100	110	Ω

Table 43. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.3	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage		V_{CCIO} – 0.6		V_{CCIO} – 0.3	V
V_{OH}	High-level output voltage		V_{CCIO}		V_{CCIO} – 0.3	V
V_T	Output termination voltage			V_{CCIO}		V
V_{OD}	Differential output voltage		300	450	600	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
R_O	Output load			100		Ω
R_L	Receiver differential input resistor		45	50	55	Ω

Table 44. LVPECL Specifications *Note (2)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage		800		2,000	mV
V_{IH}	High-level input voltage		2,100		V_{CCIO}	mV
V_{OL}	Low-level output voltage		1,450		1,650	mV
V_{OH}	High-level output voltage		2,275		2,420	mV
V_{ID}	Differential input voltage		100	600	2,500	mV
V_{OD}	Differential output voltage		625	800	970	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps

Table 45. HyperTransport Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{OD}	Differential output voltage		380	600	820	mV
V_{OCM}	Output common mode voltage	R_{TT} = 100 Ω	500	600	700	mV
V_{ID}	Differential input voltage		300	600	900	mV
V_{ICM}	Input common mode voltage		450	600	750	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Notes to Tables 42 – 45:

(1) Maximum V_{OD} is measured under static conditions.

(2) When APEX II devices drive LVPECL signals, the APEX II LVPECL outputs must be terminated with a resistor network.

Capacitance

Table 46 and Figure 40 provide information on APEX II device capacitance.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing structures ensure predictable performance, and accurate simulation and timing analysis. In contrast, the unpredictable performance of FPGAs is caused by their segmented connection scheme.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum drive strength.

Figure 41 shows the f_{MAX} timing model for APEX II devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. However, the Quartus II software timing analysis provides more accurate timing information because the Quartus II software usually has more up-to-date timing information than the data sheet until the timing model is final. Also, the Quartus II software can model delays caused by loading and distance effects more accurately than by using the numbers in this data sheet.

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 57. EP2A25 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	0.07		0.07		0.09		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 58. EP2A25 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.65		0.75		0.86		ns
t_{F20+}	1.11		1.27		1.46		ns

Table 77. APEX II Selectable I/O Standards Output Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		3.32		3.82		4.20	ns
1.8 V		2.65		3.05		3.36	ns
2.5 V		1.20		1.38		1.52	ns
3.3-V PCI		– 0.68		– 0.78		– 0.85	ns
3.3-V PCI-X		– 0.68		– 0.78		– 0.85	ns
GTL+		– 0.45		– 0.52		– 0.57	ns
SSTL-3 Class I		– 0.52		– 0.60		– 0.66	ns
SSTL-3 Class II		– 0.52		– 0.60		– 0.66	ns
SSTL-2 Class I		– 0.68		– 0.78		– 0.86	ns
SSTL-2 Class II		– 0.81		– 0.93		– 1.02	ns
HSTL Class I		– 0.08		– 0.09		– 0.10	ns
HSTL Class II		– 0.23		– 0.27		– 0.30	ns
LVDS		– 1.41		– 1.62		– 1.79	ns
LVPECL		– 1.38		– 1.58		– 1.74	ns
PCML		– 1.30		– 1.50		– 1.65	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 1.22		– 1.41		– 1.55	ns
Differential HSTL		– 1.41		– 1.62		– 1.79	ns

Power Consumption

Detailed power consumption information for APEX II devices will be released via a future interactive power estimator on the Altera web site.

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Revision History

The information contained in the *APEX II Programmable Logic Device Family Data Sheet* version 3.0 supersedes information published in previous versions. The following changes were made to the *APEX II Programmable Logic Device Family Data Sheet* version 3.0:

- Changed the value from 624 to 400 Mbps throughout the document.
- Deleted the pin count (612) for the EP2A25 device in the 1,020-pin FineLine BGA package (see Table 3).
- Added Table 13.
- Changed the maximum value of 3.6 to 2.4 in Table 20.
- Updated Tables 60 through 67 and Tables 72 through 75.
- Updated Figures 25, 28, and 30.
- Added *Note (1)* to Figure 13.
- Added Figure 43.

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