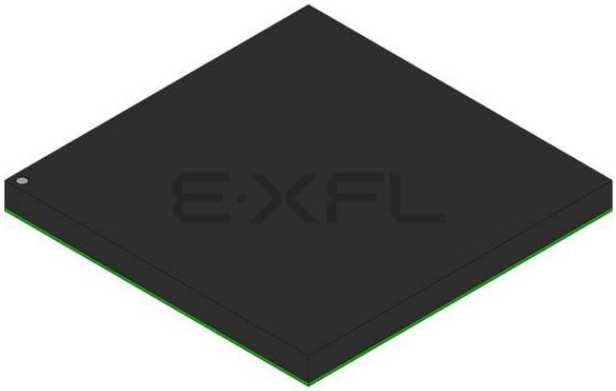

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2430 |
| Number of Logic Elements/Cells | 24320 |
| Total RAM Bits | 622592 |
| Number of I/O | 540 |
| Number of Gates | 2750000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 724-BBGA, FCBGA |
| Supplier Device Package | 724-BGA (35x35) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a25b724c8 |

Each I/O pin is fed by an IOE located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and six registers that can be used for registering input, output, and output-enable signals. When used with a dedicated clock pin, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM and ZBT and QDR SRAM devices.

IOEs provide a variety of features such as: 3.3-V, 64-bit, 66-MHz PCI compliance, 3.3-V, 64-bit, 133-MHz PCI-X compliance, Joint Test Action Group (JTAG) boundary-scan test (BST) support, output drive strength control, slew-rate control, tri-state buffers, bus-hold circuitry, programmable pull-up resistors, programmable input and output delays, and open-drain outputs.

APEX II devices offer enhanced I/O support, including support for 1.5 V, 1.8 V, 2.5 V, 3.3 V, LVCMOS, LVTTL, HSTL, LVDS, LVPECL, HyperTransport, PCML, 3.3-V PCI, PCI-X, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. High-speed (up to 1.0 Gbps) differential transfers are supported with True-LVDS circuitry for LVDS, LVPECL, HyperTransport, and PCML I/O standards. The optional CDS feature corrects any clock-to-data skew at the True-LVDS receiver channels, allowing for flexible board topologies. Up to 88 Flexible-LVDS channels support differential transfer at up to 400 Mbps (DDR) for LVDS and HyperTransport I/O standards.

An ESB can implement many types of memory, including Dual-Port+ RAM, CAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. The abundance of cascadable ESBs ensures that the APEX II device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX II device.

*Figure 1. APEX II Device Block Diagram*

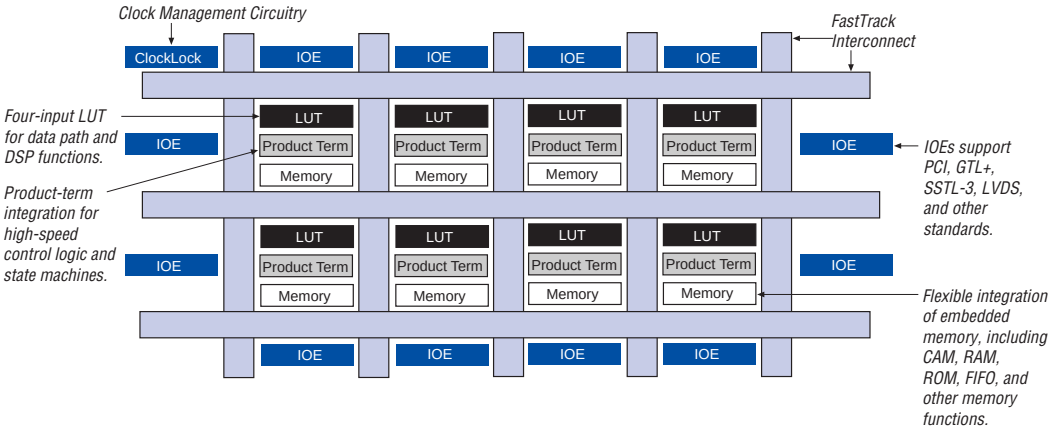


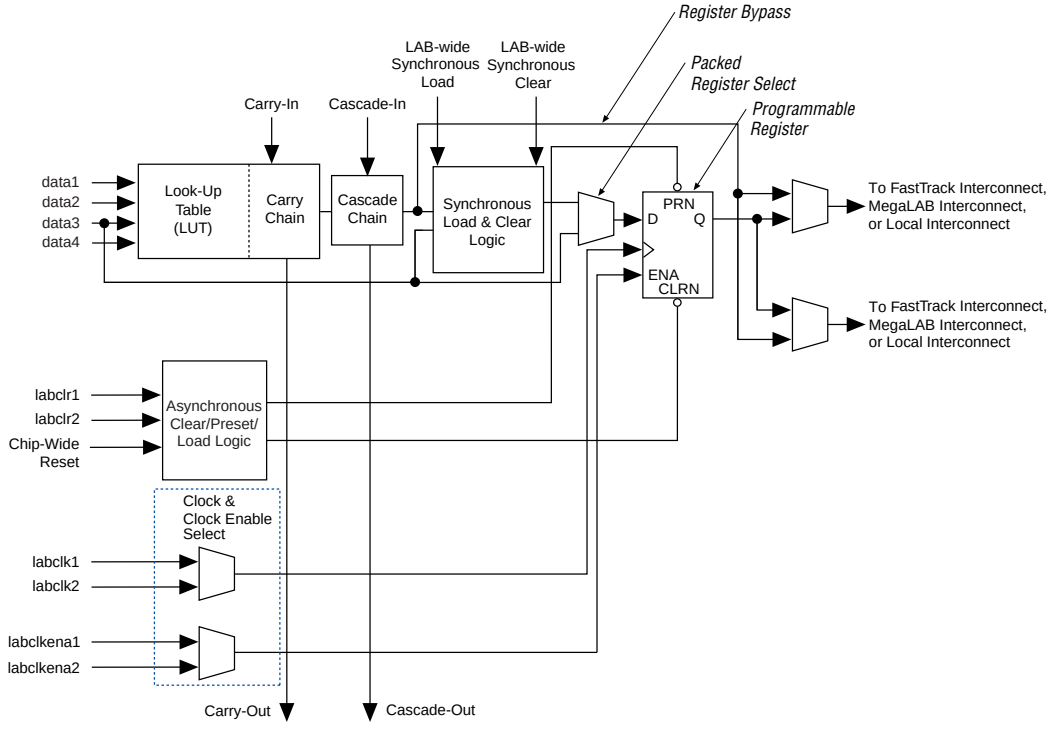

Table 4 lists the resources available in APEX II devices.

*Table 4. APEX II Device Resources*

| Device | MegaLAB Rows | MegaLAB Columns | ESBs |
|---|---|---|---|
| EP2A15 | 26 | 4 | 104 |
| EP2A25 | 38 | 4 | 152 |
| EP2A40 | 40 | 4 | 160 |
| EP2A70 | 70 | 4 | 280 |

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

*Figure 5. APEX II Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

*Figure 6. APEX II Carry Chain*

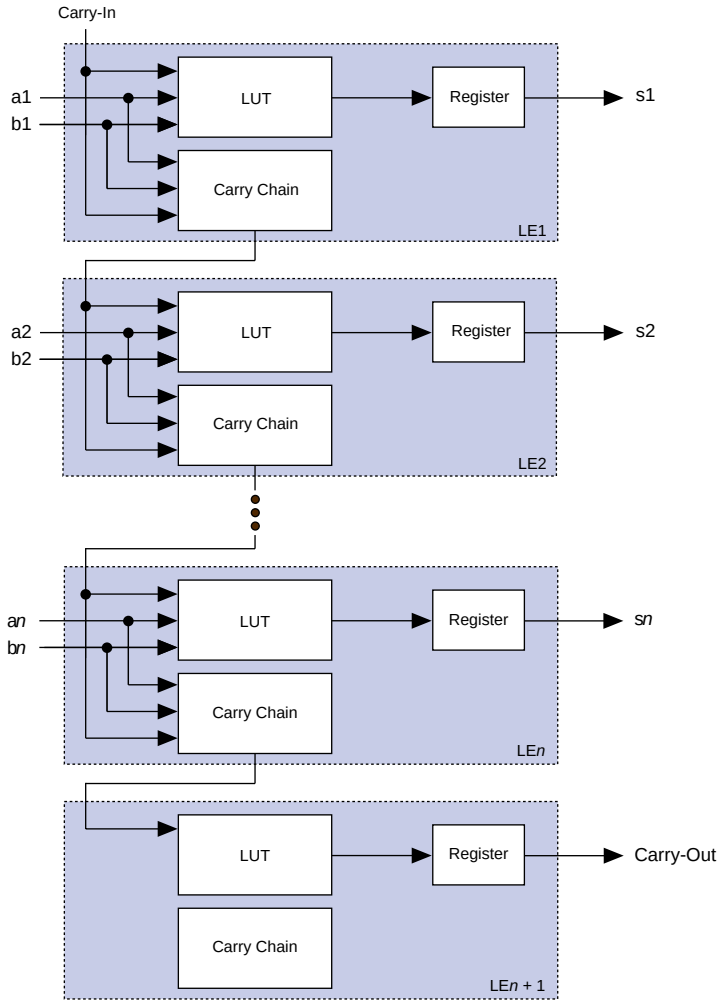
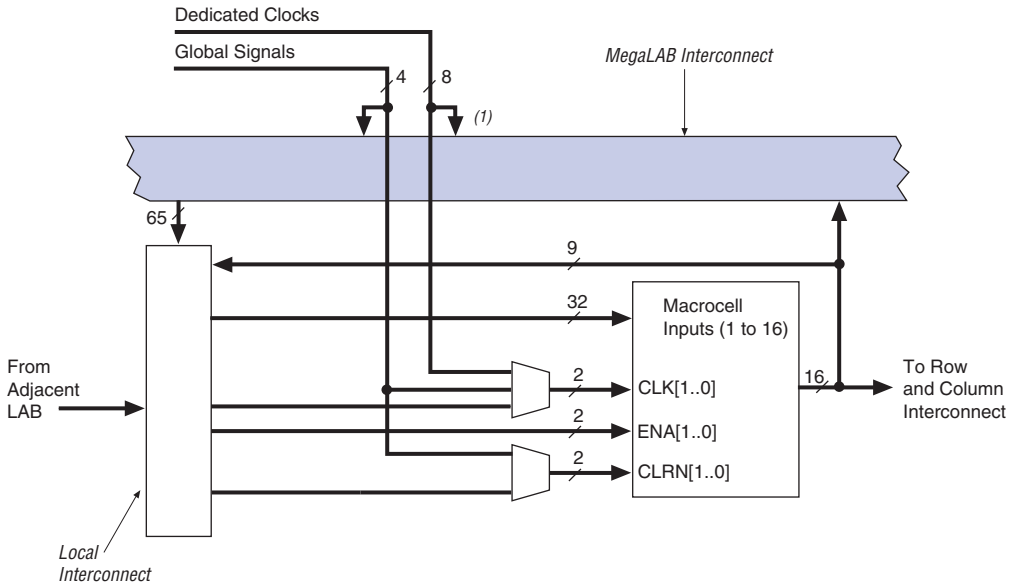


*Figure 13. Product-Term Logic in ESB*



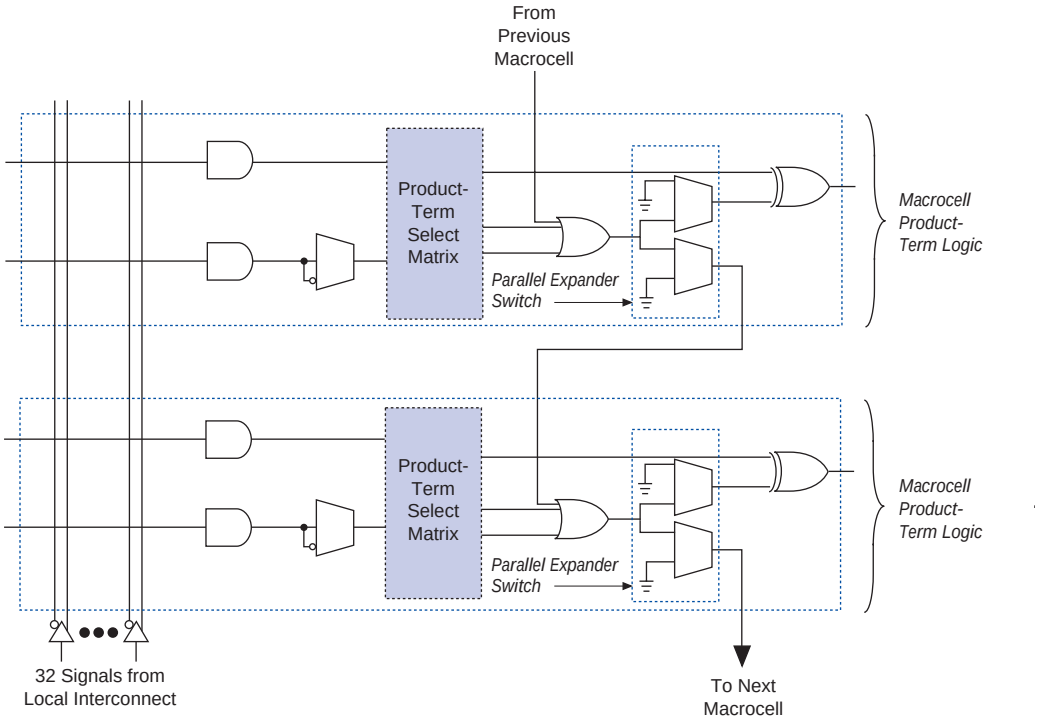

***Note ot Figure 13:***
(1) PLL outputs cannot drive data input ports.

### *Macrocells*

APEX II macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX II macrocell.

*Figure 16. APEX II Parallel Expanders*

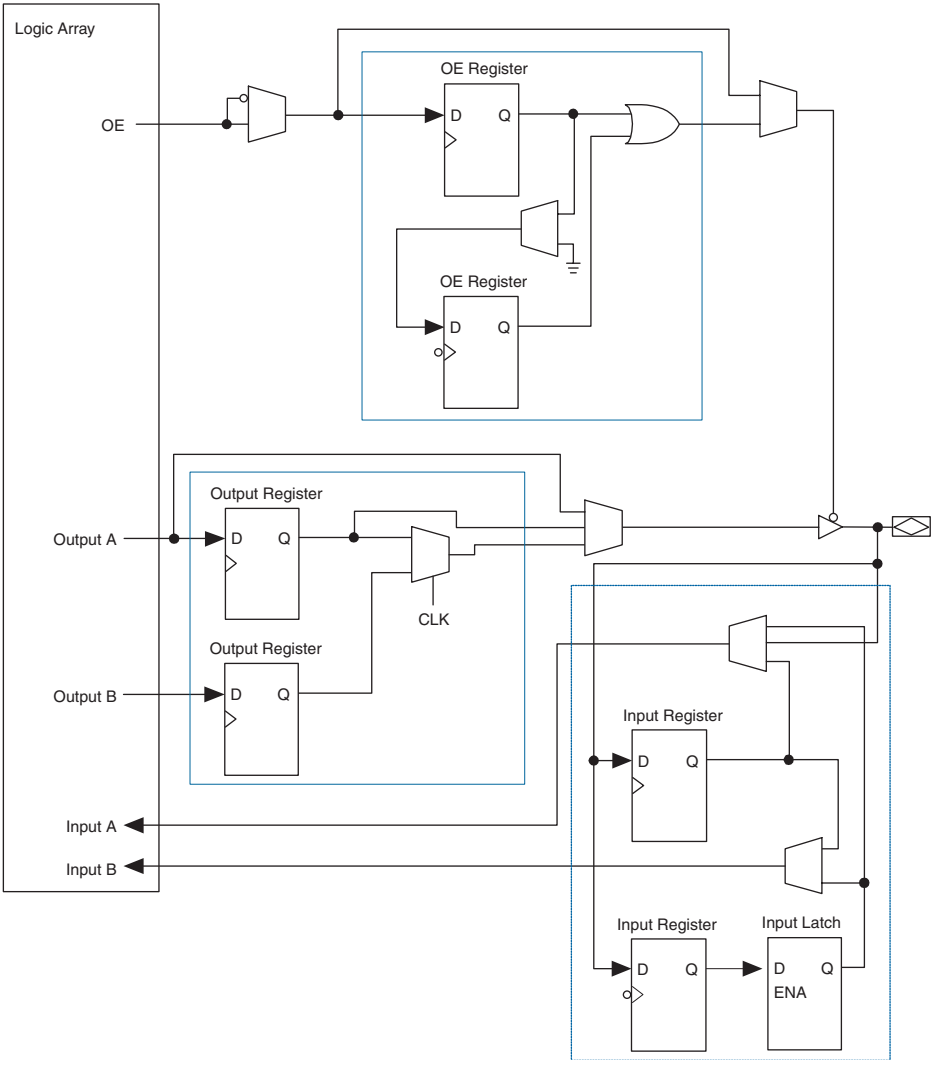



## Embedded System Block

The ESB can implement various types of memory blocks, including Dual-Port+ RAM (bidirectional dual-port RAM), dual- and single-port RAM, ROM, FIFO, and CAM blocks.

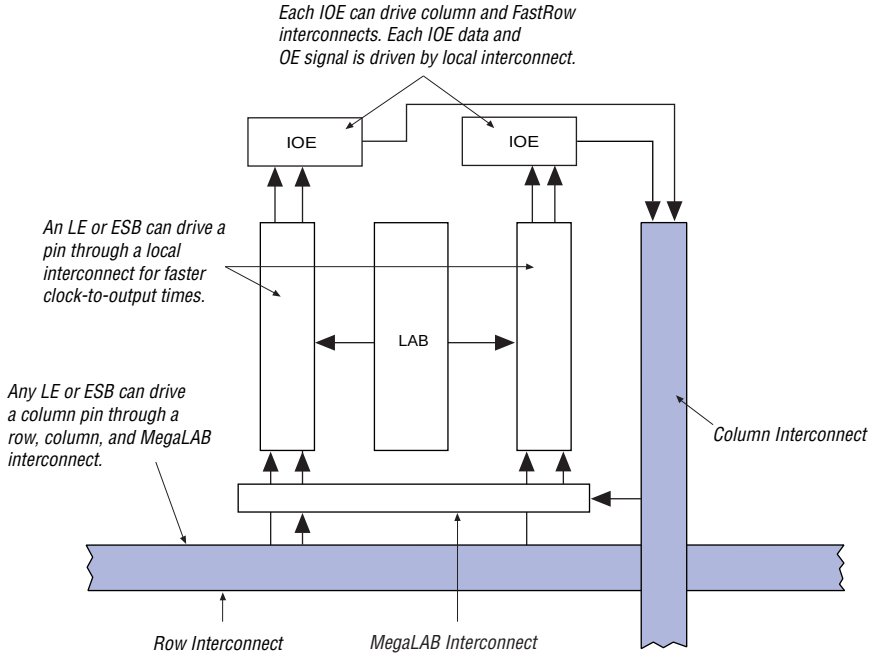
The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a bidirectional, dual-port mode, which supports any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 25. APEX II IOE Structure*




The IOEs are located around the periphery of the APEX II device. Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the FastTrack or column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

*Figure 27. Column IOE Connection to the Interconnect*




FastRow interconnects connect a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing.

APEX II devices have a peripheral control bus made up of 12 signals that drive the IOE control signals. The peripheral bus is composed of six output enables, `OE[5:0]` and six clock enables, `CE[5:0]`. These twelve signals can be driven from internal logic or from the Fast I/O signals. Table 7 lists the peripheral control signal destinations.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the $t_{ZX}$ delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

*Table 8. APEX II Programmable Delay Chain*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input pin to logic array delay *(1)* | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input register |
| Output propagation delay | Increase delay to output pin |
| Output enable register $t_{CO}$ delay | Increase delay to output enable pin |
| Output $t_{ZX}$ delay | Increase $t_{ZX}$ delay to output pin |
| Output clock enable delay | Increase output clock enable delay |
| Input clock enable delay | Increase input clock enable delay |
| Logic array to output register delay | Decrease input delay to output register |

***Note to Table 8:***
(1) This delay has four settings: off and three levels of delay.

The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

## Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

## Zero Bus Turnaround SRAM Interface Support

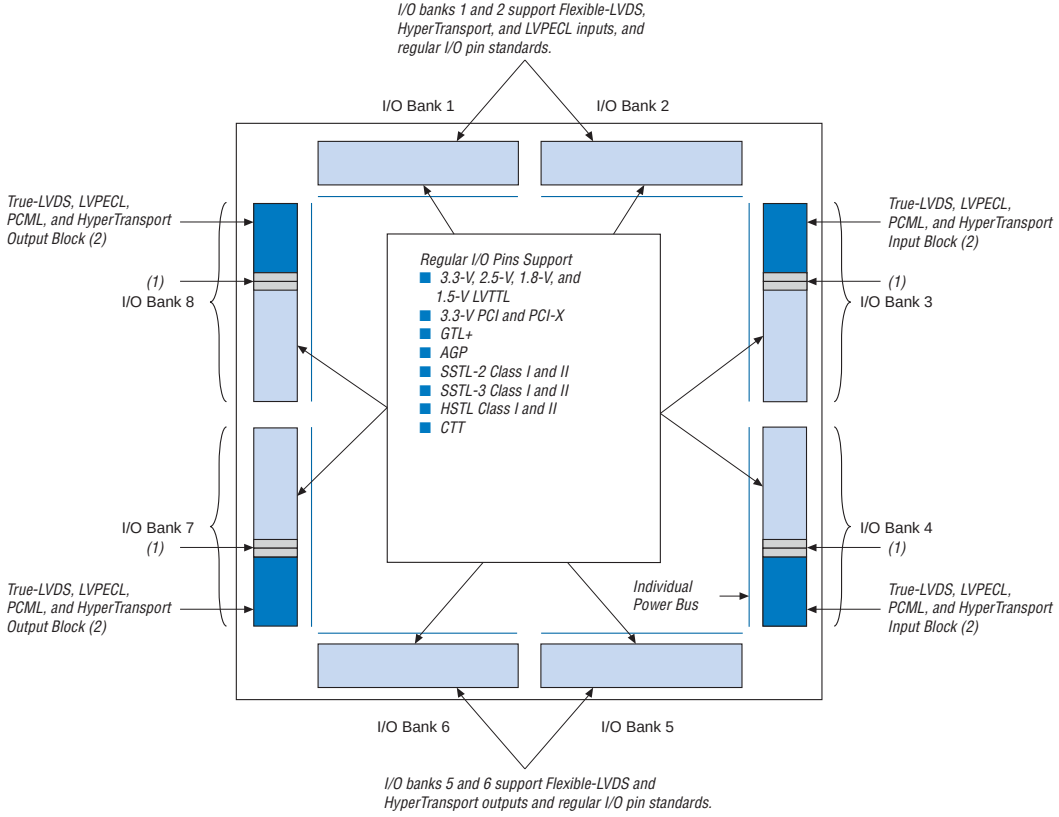
In addition to DDR SDRAM support, APEX II device I/O pins also support interfacing with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time ($t_{ZX}$) delay ensures that the $t_{ZX}$ is greater than the clock-to-high-impedance time ($t_{XZ}$). Phase delay control of clocks to the OE/output and input registers using two general-purpose PLLs enable the APEX II device to meet ZBT $t_{CO}$ and $t_{SU}$ times.

## Programmable Drive Strength

The output buffer for each APEX II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, 3.3-V GTL+, PCI, and PCI-X support a minimum setting. The minimum setting is the lowest drive strength that guarantees the $I_{OH}/I_{OL}$ of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 9 shows the possible settings for the I/O standards with drive strength control.

*Figure 31. APEX II I/O Banks*




***Notes to Figure 31:***

(1) For more information on placing I/O pins within LVDS blocks, refer to the "High-Speed Interface Pin Location" section in *Application Note 166 (Using High-Speed I/O Standards in APEX II Devices)*.

(2) If the True-LVDS pins or the Flexible-LVDS pins are not used for high-speed differential signalling, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with $V_{CCIO}$ set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V. However, True-LVDS pins do not support the HSTL Class II output.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level to support any one of the terminated standards (such as SSTL-3) independently.

Signals can be driven into APEX II devices before and during power-up without damaging the device. In addition, APEX II devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX II devices operate as specified by the user.

## General-Purpose PLLs

APEX II devices have ClockLock, ClockBoost, and ClockShift features, which use four general-purpose PLLs (separate from the four dedicated True-LVDS PLLs) to provide clock management and clock-frequency synthesis. These PLLs allow designers to increase performance and provide clock-frequency synthesis. The PLL reduces the clock delay within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The PLLs, which provide programmable multiplication, allow the designer to distribute a low-speed clock and multiply that clock on-device. APEX II devices include a high-speed clock tree: unlike ASICs, the user does not have to design and optimize the clock tree. The PLLs work in conjunction with the APEX II device's high-speed clock to provide significant improvements in system performance and bandwidth.

The PLLs in APEX II devices are enabled through the Quartus II software. External devices are not required to use these features. Table 15 shows the general-purpose PLL features for APEX II devices. Figure 35 shows an APEX II general-purpose PLL.

*Table 15. APEX II General-Purpose PLL Features*

| Number of PLLs | ClockBoost Feature | Number of External Clock Outputs | Number of Feedback Inputs |
|---|---|---|---|
| 4 | $m/(n \times k, v)$ | 8 | 2 |

*Figure 35. APEX II General-Purpose PLL* *Note (1)*

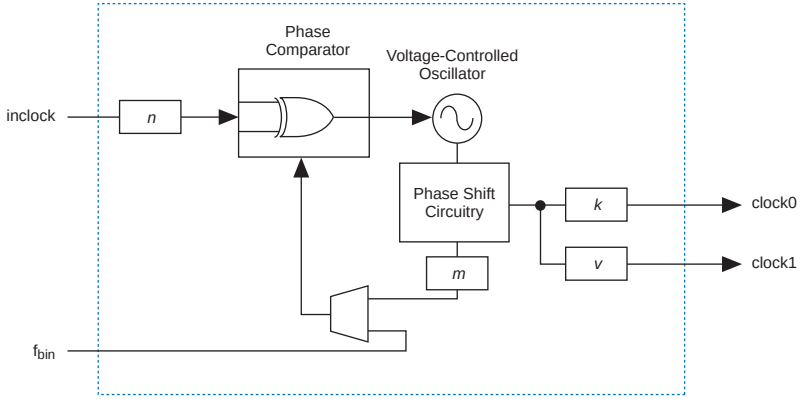


*Figure 36. APEX II JTAG Waveforms*

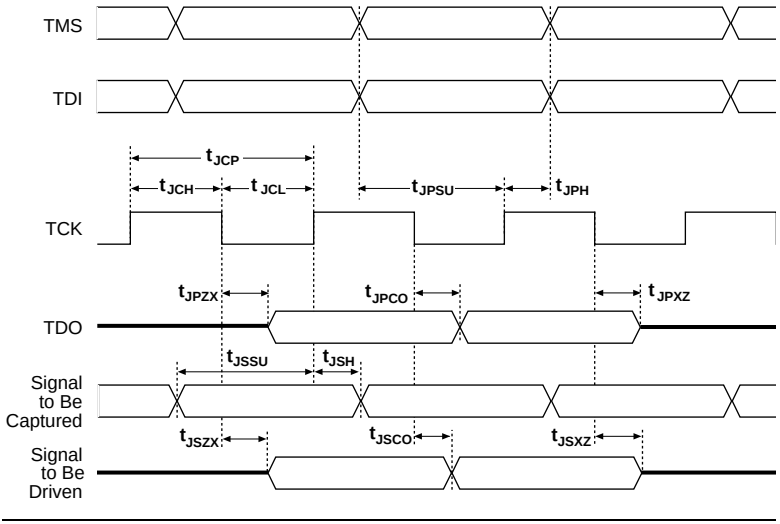



Table 19 shows the JTAG timing parameters and values for APEX II devices.

*Table 19. APEX II JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

*Table 34. SSTL-3 Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{TT}$ | Termination voltage | | $V_{REF}$ – 0.05 | $V_{REF}$ | $V_{REF}$ + 0.05 | V |
| $V_{REF}$ | Reference voltage | | 1.3 | 1.5 | 1.7 | V |
| $V_{IH}$ | High-level input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(10)* | $V_{TT}$ + 0.8 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(10)* | | | $V_{TT}$ – 0.8 | V |

*Table 35. 3.3-V AGP 2× Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{REF}$ | Reference voltage | | $0.39 \times V_{CCIO}$ | | $0.41 \times V_{CCIO}$ | V |
| $V_{IH}$ | High-level input voltage *(11)* | | $0.5 \times V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage *(11)* | | | | $0.3 \times V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –20 µA | $0.9 \times V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 20 µA | | | $0.1 \times V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | $0 < V_{IN} < V_{CCIO}$ | –10 | | 10 | µA |

*Table 36. 3.3-V AGP 1× Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{IH}$ | High-level input voltage *(11)* | | $0.5 \times V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage *(11)* | | | | $0.3 \times V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –20 µA | $0.9 \times V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 20 µA | | | $0.1 \times V_{CCIO}$ | V |
| $I_I$ | Input pin leakage current | $0 < V_{IN} < V_{CCIO}$ | –10 | | 10 | µA |

*Table 42. 3.3-V LVDS I/O Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{OD}$ | Differential output voltage | $R_L$ = 100 Ω | 250 | | 850 *(1)* | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{OS}$ | Output Offset voltage | $R_L$ = 100 Ω | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Change in $V_{OS}$ between high and low | $R_L$ = 100 Ω | | | 50 | mV |
| $V_{TH}$ | Differential input threshold | $V_{CM}$ = 1.2 V | –100 | | 100 | mV |
| $V_{IN}$ | Receiver input voltage range | | 0.0 | | 2.4 | V |
| $R_L$ | Receiver differential input resistor (external to APEX II devices) | | 90 | 100 | 110 | Ω |

*Table 43. 3.3-V PCML Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{IL}$ | Low-level input voltage | | | | $V_{CCIO}$ – 0.3 | V |
| $V_{IH}$ | High-level input voltage | | $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CCIO}$ – 0.6 | | $V_{CCIO}$ – 0.3 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CCIO}$ | | $V_{CCIO}$ – 0.3 | V |
| $V_T$ | Output termination voltage | | | $V_{CCIO}$ | | V |
| $V_{OD}$ | Differential output voltage | | 300 | 450 | 600 | mV |
| $t_R$ | Rise time (20 to 80%) | | 85 | | 325 | ps |
| $t_F$ | Fall time (20 to 80%) | | 85 | | 325 | ps |
| $R_O$ | Output load | | | 100 | | Ω |
| $R_L$ | Receiver differential input resistor | | 45 | 50 | 55 | Ω |

| Table 50. APEX II Minimum Pulse Width Timing Parameters | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

| Table 51. APEX II External Timing Parameters Note (1) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSU}$ | Setup time with global clock at IOE input register | |
| $t_{INH}$ | Hold time with global clock at IOE input register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | C1 = 35 pF |
| $t_{XZ}$ | Clock-to-output buffer disable delay | |
| $t_{ZX}$ | Clock-to-output buffer enable delay | Slow slew rate = OFF |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | C1 = 35 pF |
| $t_{XZPLL}$ | PLL clock-to-output buffer disable delay | |
| $t_{ZXPLL}$ | PLL clock-to-output buffer enable delay | Slow slew rate = OFF |

***Note to Table 51:***

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

*Table 57. EP2A25 $f_{MAX}$ ESB Timing Parameters*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.28 | | 1.47 | | 1.69 | ns |
| $t_{ESBSRC}$ | | 2.49 | | 2.86 | | 3.29 | ns |
| $t_{ESBAWC}$ | | 2.20 | | 2.53 | | 2.91 | ns |
| $t_{ESBSWC}$ | | 3.02 | | 3.47 | | 3.99 | ns |
| $t_{ESBWASU}$ | 0.07 | | 0.07 | | 0.09 | | ns |
| $t_{ESBWAH}$ | 0.15 | | 0.18 | | 0.20 | | ns |
| $t_{ESBWDSU}$ | 0.37 | | 0.43 | | 0.49 | | ns |
| $t_{ESBWDH}$ | 0.16 | | 0.18 | | 0.21 | | ns |
| $t_{ESBRASU}$ | 0.84 | | 0.96 | | 1.11 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 0.14 | | 0.16 | | 0.19 | | ns |
| $t_{ESBDATASU}$ | – 0.02 | | – 0.03 | | – 0.03 | | ns |
| $t_{ESBWADDRSU}$ | – 0.40 | | – 0.46 | | – 0.53 | | ns |
| $t_{ESBRADDRSU}$ | – 0.38 | | – 0.44 | | – 0.51 | | ns |
| $t_{ESBDATACO1}$ | | 1.30 | | 1.50 | | 1.72 | ns |
| $t_{ESBDATACO2}$ | | 1.84 | | 2.12 | | 2.44 | ns |
| $t_{ESBDD}$ | | 2.42 | | 2.78 | | 3.19 | ns |
| $t_{PD}$ | | 1.69 | | 1.94 | | 2.23 | ns |
| $t_{PTERMSU}$ | 1.10 | | 1.26 | | 1.45 | | ns |
| $t_{PTERMCO}$ | | 0.82 | | 0.94 | | 1.08 | ns |

*Table 58. EP2A25 $f_{MAX}$ Routing Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | 0.19 | | 0.21 | | 0.25 | | ns |
| $t_{F5-20}$ | 0.65 | | 0.75 | | 0.86 | | ns |
| $t_{F20+}$ | 1.11 | | 1.27 | | 1.46 | | ns |

*Table 73. EP2A40 External Timing Parameters for Column I/O Pins*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.00 | | 2.16 | | 2.33 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.96 | 2.00 | 5.29 | 2.00 | 5.64 | ns |
| $t_{XZ}$ | | 7.04 | | 7.59 | | 8.19 | ns |
| $t_{ZX}$ | | 7.04 | | 7.59 | | 8.19 | ns |
| $t_{INSUPLL}$ | 1.20 | | 1.31 | | 1.43 | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.66 | 0.50 | 2.87 | 0.50 | 3.09 | ns |
| $t_{XZPLL}$ | | 4.74 | | 5.17 | | 5.64 | ns |
| $t_{ZXPLL}$ | | 4.74 | | 5.17 | | 5.64 | ns |

*Table 74. EP2A70 External Timing Parameters for Row I/O Pins*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.48 | | 2.68 | | 2.90 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.76 | 2.00 | 5.12 | 2.00 | 5.51 | ns |
| $t_{XZ}$ | | 5.68 | | 6.19 | | 6.76 | ns |
| $t_{ZX}$ | | 5.68 | | 6.19 | | 6.76 | ns |
| $t_{INSUPLL}$ | 1.19 | | 1.30 | | 1.43 | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.52 | 0.50 | 2.74 | 0.50 | 2.98 | ns |
| $t_{XZPLL}$ | | 3.44 | | 3.82 | | 4.23 | ns |
| $t_{ZXPLL}$ | | 3.44 | | 3.82 | | 4.23 | ns |

*Table 76. APEX II Selectable I/O Standards Input Adder Delays*

| Symbol | -7 Speed Grade | | -8 Speed Grade | | -9 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 1.5 V | | 0.10 | | 0.11 | | 0.12 | ns |
| 1.8 V | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.00 | | 0.00 | ns |
| 3.3-V PCI | | 0.00 | | 0.00 | | 0.00 | ns |
| 3.3-V PCI-X | | 0.00 | | 0.00 | | 0.00 | ns |
| GTL+ | | – 0.20 | | – 0.22 | | – 0.24 | ns |
| SSTL-3 Class I | | – 0.17 | | – 0.19 | | – 0.20 | ns |
| SSTL-3 Class II | | – 0.17 | | – 0.19 | | – 0.20 | ns |
| SSTL-2 Class I | | – 0.24 | | – 0.26 | | – 0.29 | ns |
| SSTL-2 Class II | | – 0.24 | | – 0.26 | | – 0.29 | ns |
| HSTL Class I | | – 0.03 | | – 0.03 | | – 0.03 | ns |
| HSTL Class II | | – 0.03 | | – 0.03 | | – 0.03 | ns |
| LVDS | | – 0.23 | | – 0.26 | | – 0.28 | ns |
| LVPECL | | – 0.23 | | – 0.26 | | – 0.28 | ns |
| PCML | | – 0.23 | | – 0.26 | | – 0.28 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| 3.3-V AGP 1× | | 0.00 | | 0.00 | | 0.00 | ns |
| 3.3-V AGP 2× | | 0.00 | | 0.00 | | 0.00 | ns |
| HyperTransport | | – 0.23 | | – 0.26 | | – 0.28 | ns |
| Differential HSTL | | – 0.23 | | – 0.26 | | – 0.28 | ns |

## Revision History

The information contained in the *APEX II Programmable Logic Device Family Data Sheet* version 3.0 supersedes information published in previous versions. The following changes were made to the *APEX II Programmable Logic Device Family Data Sheet* version 3.0:

- Changed the value from 624 to 400 Mbps throughout the document.
- Deleted the pin count (612) for the EP2A25 device in the 1,020-pin FineLine BGA package (see Table 3).
- Added Table 13.
- Changed the maximum value of 3.6 to 2.4 in Table 20.
- Updated Tables 60 through 67 and Tables 72 through 75.
- Updated Figures 25, 28, and 30.
- Added *Note (1)* to Figure 13.
- Added Figure 43.

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