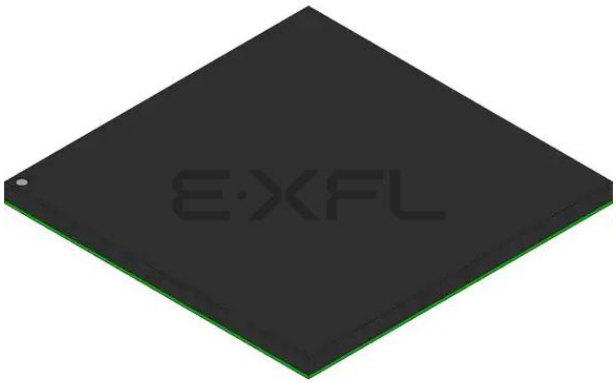

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a25f672c7

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. APEX II Package Sizes

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Pitch (mm)	1.00	1.27	1.00	1.00
Area (mm^2)	729	1,225	1,089	1,600
Length × Width (mm × mm)	27 × 27	35 × 35	33 × 33	40 × 40

Table 3. APEX II Package Options & I/O Pin Count *Notes (1), (2)*

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2A15	492	492		
EP2A25	492	536		
EP2A40	492	536	735	
EP2A70		536		1,060

Notes to Table 3:

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

After an APEX II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Software

APEX II devices are supported by the Altera Quartus II development system: a single, integrated package that offers hardware description language (HDL) and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software includes the LogicLock incremental design feature. The LogicLock feature allows the designer to make pin and timing assignments, verify functionality and performance, and then set constraints to lock down the placement and performance of a specific block of logic using LogicLock constraints. Constraints set by the LogicLock function guarantee repeatable placement when implementing a block of logic in a current project or exporting the block to another project. The constraints set by the LogicLock feature can lock down logic to a fixed location in the device. The LogicLock feature can also lock the logic down to a floating location, and the Quartus II software determines the best relative placement of the block to meet design requirements. Adding additional logic to a project will not affect the performance of blocks locked down with LogicLock constraints.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can open the Quartus II software from within third-party design tools. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX II devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX II architecture.

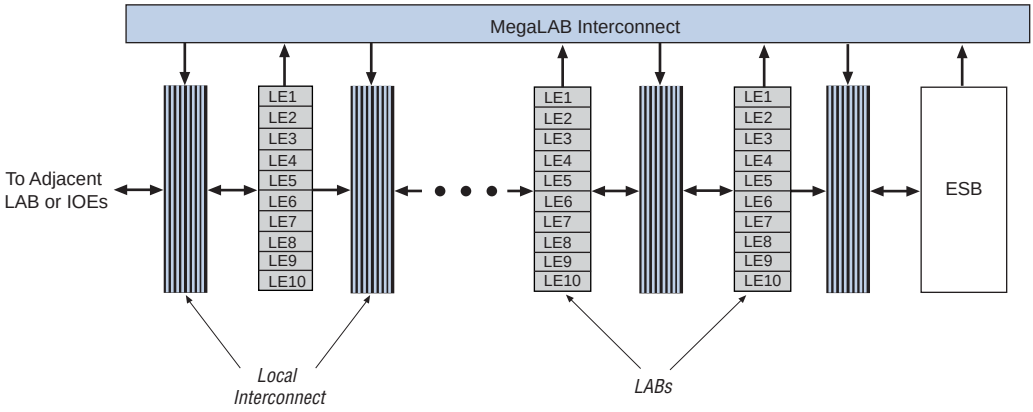
Functional Description

APEX II devices incorporate LUT-based logic, product-term-based logic, memory, and high-speed I/O standards into one device. Signal interconnections within APEX II devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

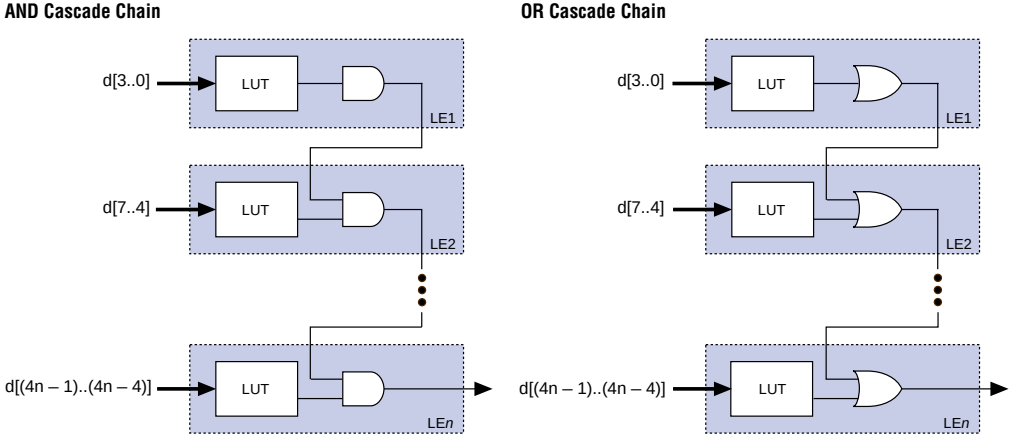
APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

Cascade Chain

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

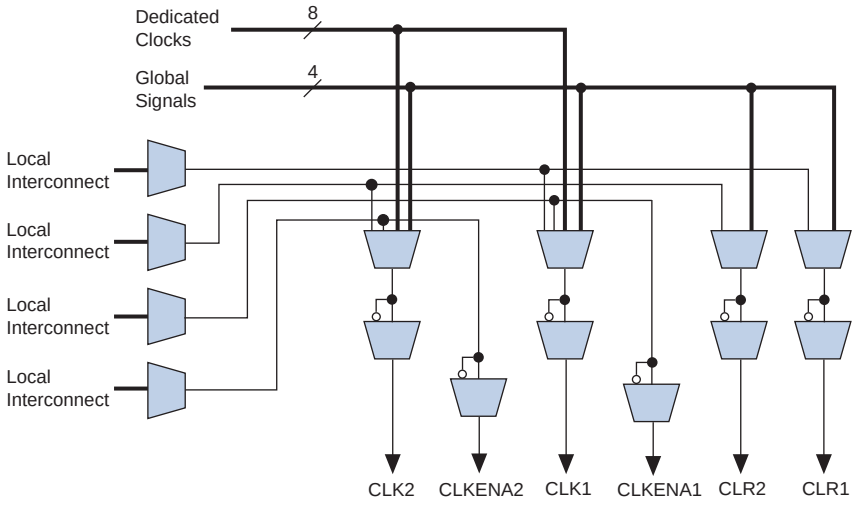
Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX II Cascade Chain



The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic



Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX II parallel expanders.

The ESB also enables variable width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the ESB can be written in 1× mode at port A while being read in 16× mode from port B. Table 6 lists the supported variable width configurations for an ESB in dual-port mode.

Table 6. Variable Width Configurations for Dual-Port RAM

Read Port Width	Write Port Width
1 bit	2 bits, 4 bits, 8 bits, or 16 bits
2 bits, 4 bits, 8 bits, or 16 bits	1 bit

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM only need to meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack interconnects. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack interconnects and the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 512 × 8, 1,024 × 4, 2,048 × 2, or 4,096 × 1. For dual-port and single-port modes, the ESB can be configured for 256 × 16 in addition to the list above.

The ESB can also be split in half and used for two independent 2,048-bit single-port RAM blocks. The two independent RAM blocks must have identical configurations with a maximum width of 256 × 8. For example, one half of the ESB can be used as a 256 × 8 single-port memory while the other half is also used for a 256 × 8 single-port memory. This effectively doubles the number of RAM blocks an APEX II device can implement for its given number of ESBs. The Quartus II software automatically merges two logical memory functions in a design into an ESB; the designer does not need to merge the functions manually.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data's location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 21 and 22 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 22. Encoded CAM Address Outputs

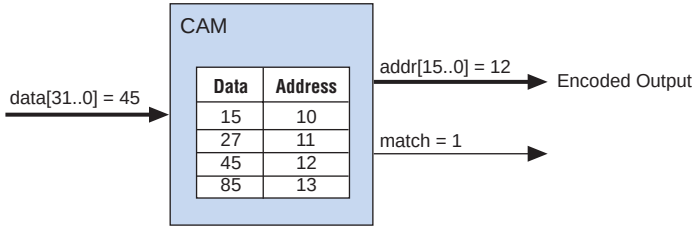
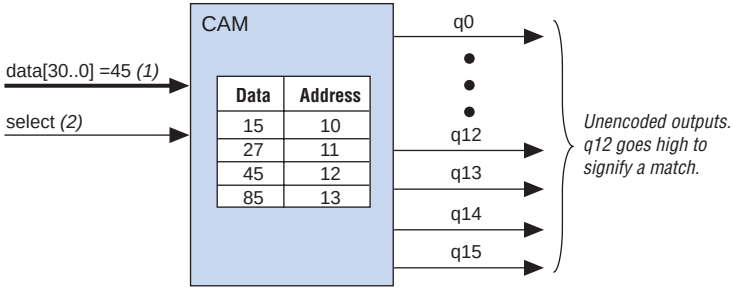


Figure 23. Unencoded CAM Address Outputs



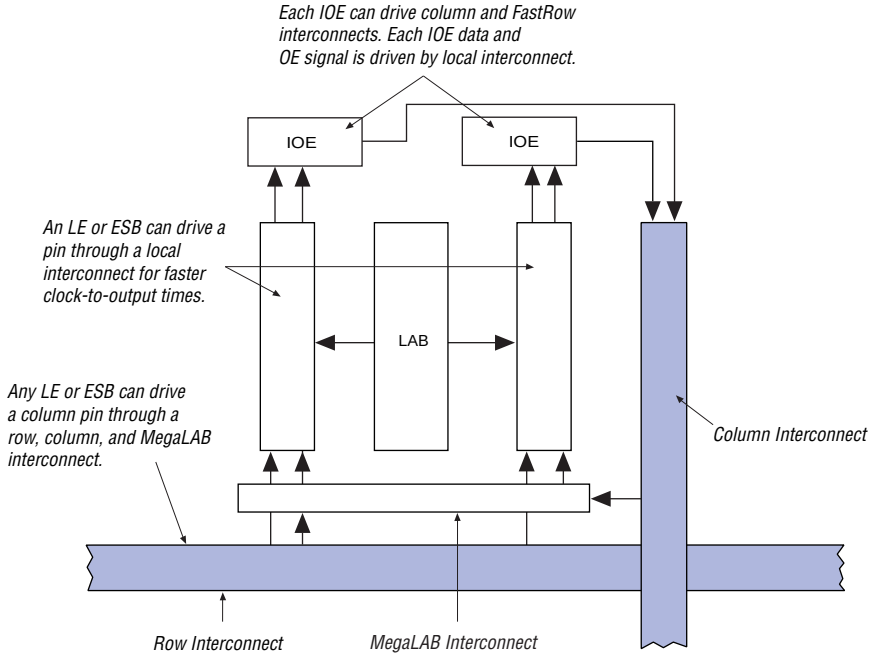
Notes to Figures 22 and 23:

(1) For an unencoded output, the ESB only supports 31 input data bits. One input bit is used by the `select` line to choose one of the two banks of 16 outputs.

(2) If the `select` input is a 1, then CAM outputs odd words between 1 through 15. If the `select` input is a 0, CAM outputs even words between 0 through 14.

In single-match mode, it takes two clock cycles to write into CAM, but only one clock cycle to read from CAM. In this mode, both encoded and unencoded outputs are available without external logic. Single-match mode is better suited for designs without duplicate data in the memory.

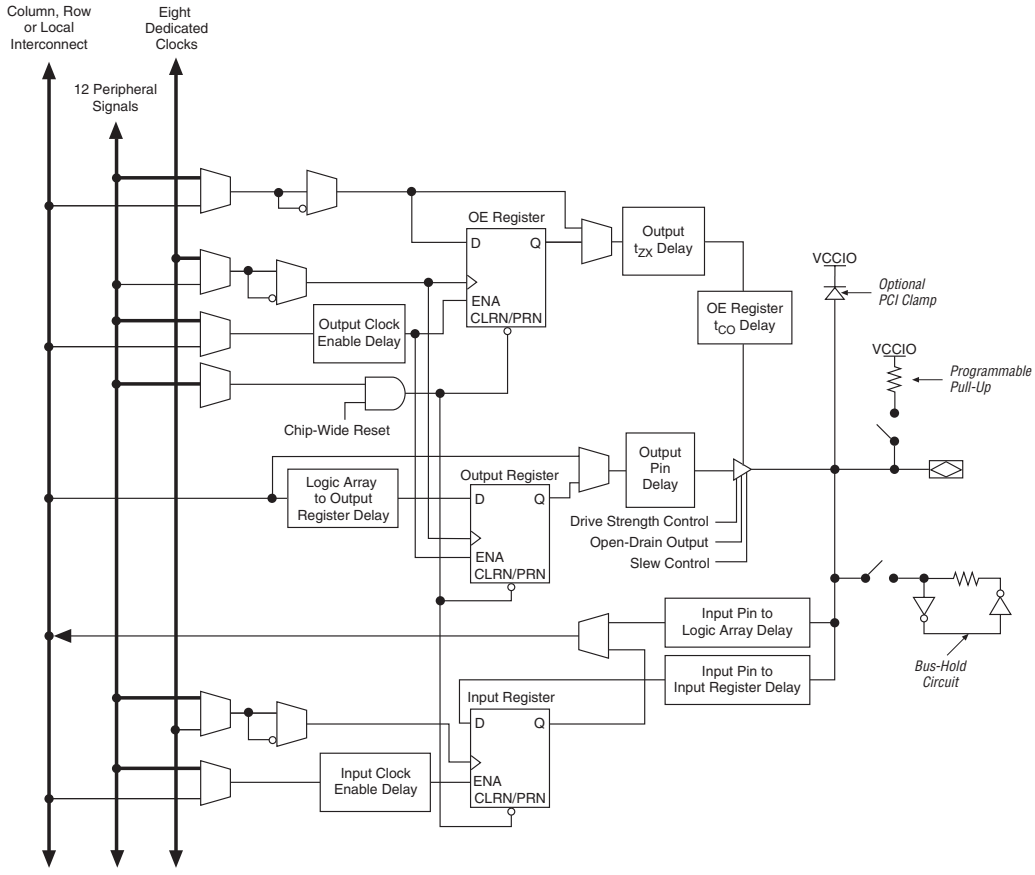
Figure 27. Column IOE Connection to the Interconnect



FastRow interconnects connect a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing.

APEX II devices have a peripheral control bus made up of 12 signals that drive the IOE control signals. The peripheral bus is composed of six output enables, `OE[5:0]` and six clock enables, `CE[5:0]`. These twelve signals can be driven from internal logic or from the Fast I/O signals. Table 7 lists the peripheral control signal destinations.

Figure 28. APEX II IOE in Bidirectional I/O Configuration



The APEX II IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

Table 8. APEX II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay *(1)*	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output propagation delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register

Note to Table 8:
(1) This delay has four settings: off and three levels of delay.

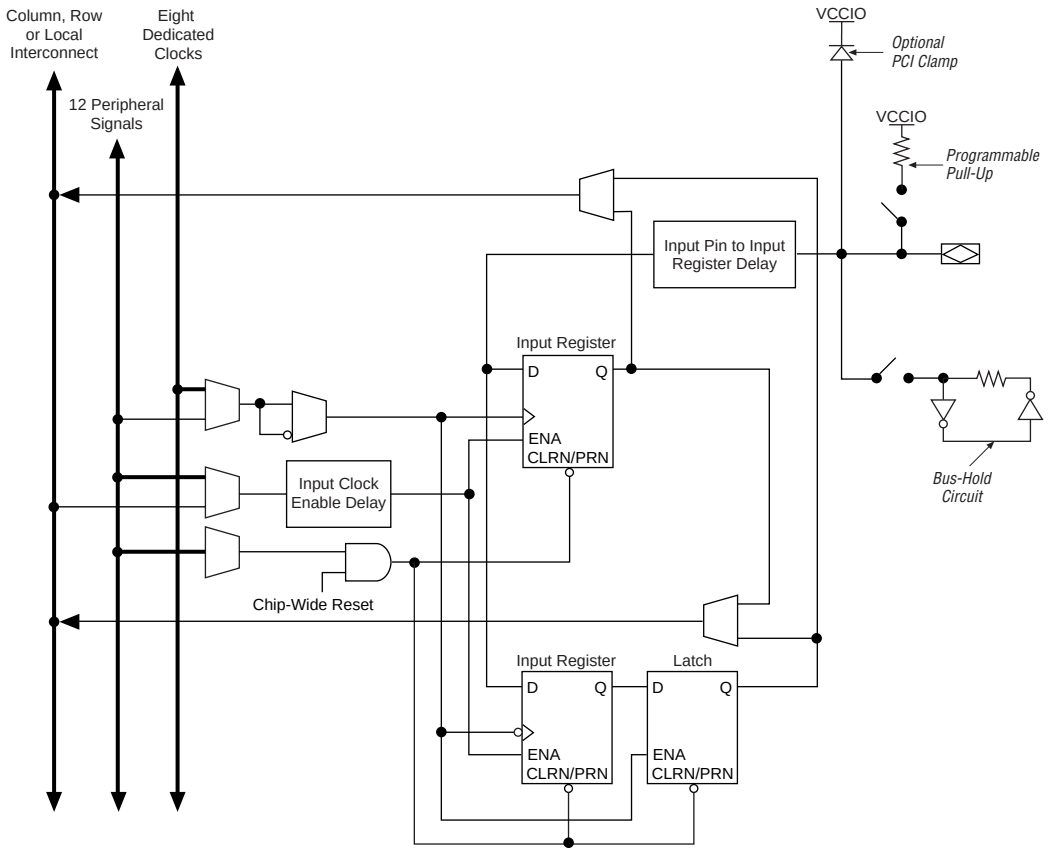
The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Table 9. Programmable Drive Strength	
I/O Standard	**I_{OH}/I_{OL} Current Strength Setting**
LVTTL (3.3 V)	4 mA
	12 mA
	24 mA (default)
LVTTL (2.5 V)	2 mA
	16 mA (default)
LVTTL (1.8 V)	2 mA
	8mA (default)
LVTTL (1.5 V)	2 mA (default)
SSTL-3 class I and II SSTL-2 class I and II HSTL class I and II GTL+ (3.3 V) PCI PCI-X	Minimum (default)

Open-Drain Output

APEX II devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each APEX II device I/O pin has a programmable output slew rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each I/O pin has an individual slew rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges.

Bus Hold

Each APEX II device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signal is present, the bus-hold feature eliminates the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. The bus-hold feature should also be disabled if open-drain outputs are used with the GTL+ I/O standard.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ. Table 41 on page 74 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

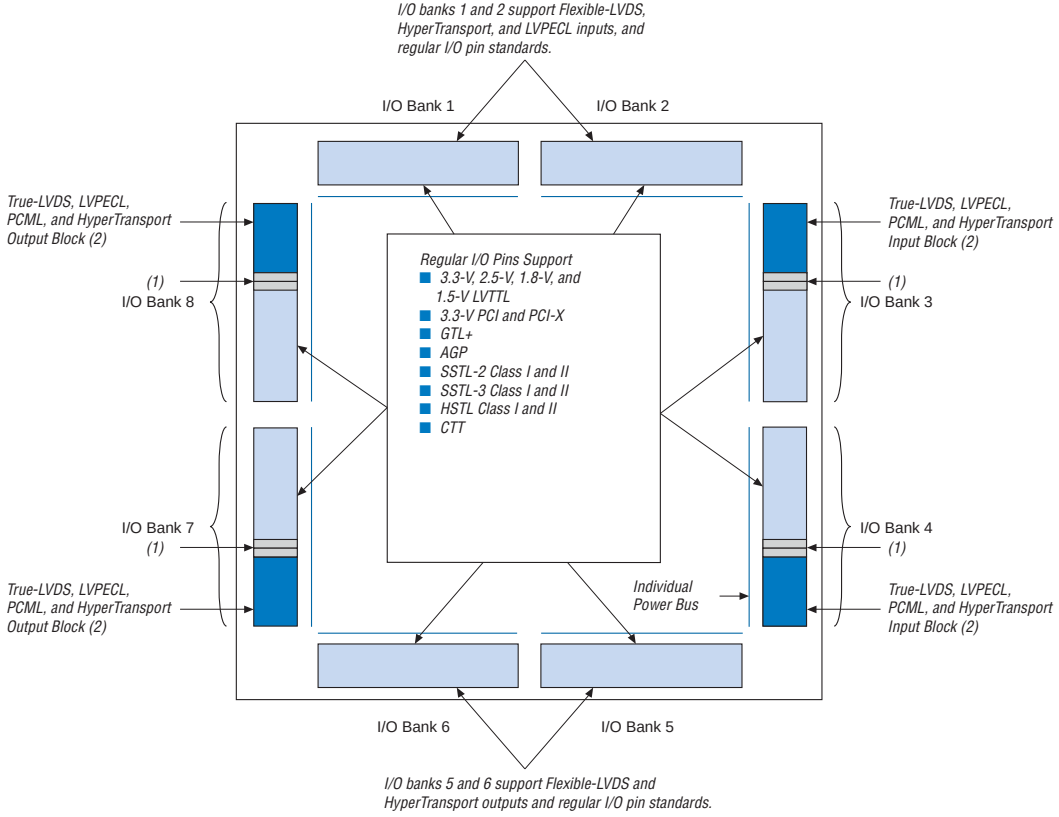
Programmable Pull-Up Resistor

Each APEX II device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the bank that the output pin resides in.

Dedicated Fast I/O Pins

APEX II devices incorporate dedicated bidirectional pins for signals with high internal fanout, such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and can drive the four global fast lines throughout the device, ideal for fast clock, clock enable, preset, clear, or high fanout logic signal distribution. The dedicated fast I/O pins have one output register and one OE register, but they do not have input registers. The dedicated fast lines can also be driven by a LE local interconnect to generate internal global signals.

Figure 31. APEX II I/O Banks



Notes to Figure 31:

(1) For more information on placing I/O pins within LVDS blocks, refer to the "High-Speed Interface Pin Location" section in *Application Note 166 (Using High-Speed I/O Standards in APEX II Devices)*.

(2) If the True-LVDS pins or the Flexible-LVDS pins are not used for high-speed differential signalling, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V. However, True-LVDS pins do not support the HSTL Class II output.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level to support any one of the terminated standards (such as SSTL-3) independently.

Pre-programmed CDS may also be used to resolve clock-to-data skew greater than 50% of the bit period. However, internal logic must be used to implement the byte alignment circuitry for this operation.

Flexible-LVDS I/O Pins

A subset of pins in the top two I/O banks supports interfacing with Flexible-LVDS, LVPECL, and HyperTransport inputs. These Flexible-LVDS input pins include dedicated LVDS, LVPECL, and HyperTransport input buffers. A subset of pins in the bottom two I/O banks supports interfacing with Flexible-LVDS and HyperTransport outputs. These Flexible-LVDS output pins include dedicated LVDS and HyperTransport output buffers. The Flexible-LVDS pins do not require any external components except for 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization/deserialization circuitry; therefore, internal logic is used to perform serialization/deserialization functions.

The EP2A15 and EP2A25 devices support 56 input and 56 output Flexible-LVDS channels. The EP2A40 and larger devices support 88 input and 88 output Flexible-LVDS channels. All APEX II devices support the Flexible-LVDS interface up to 400 Mbps (DDR) per channel. Flexible-LVDS pins along with the True-LVDS pins provide up to 144-Gbps total device bandwidth. Table 13 shows the Flexible-LVDS timing specification.

Table 13. APEX II Flexible-LVDS Timing Specification

Symbol	Timing Parameter Definition	Speed Grade						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Data Rate	Maximum operating speed		400		311		311	Mbps
TCCS	Transmitter channel-to-channel skew		700		900		900	ps
SW	Receiver sampling window	1,100		1,400		1,400		ps

MultiVolt I/O Interface

The APEX II architecture supports the MultiVolt I/O interface feature, which allows APEX II devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

Tables 20 through 41 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 20. APEX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 21. APEX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 28. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 29. PCI-X Specifications

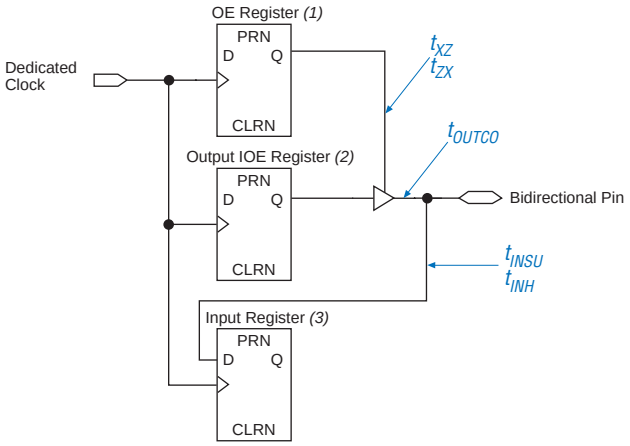
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
L_{PIN}	Pin inductance				15	nH

Table 30. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(10)*			0.65	V

Figure 42 shows the timing model for bi-directional, input, and output IOE timing.

Figure 42. Synchronous External TIming Model



Notes to Figure 42:

(1) The output enable register is in the IOE and is controlled by the "Fast Output Enable Register = ON" option in the Quartus II software.

(2) The output register is in the IOE and is controlled by the "Fast Output Register = ON" option in the Quartus II software.

(3) The input register is in the IOE and is controlled by the "Fast Input Register = ON" option in the Quartus II software.

Tables 47 through 50 show APEX II LE, ESB, and routing delays and minimum pulse-width timing parameters for the f_{MAX} timing model.

Table 47. APEX II f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 61. EP2A40 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.28		2.62		3.01	ns
t_{ESBSRC}		2.23		2.56		2.95	ns
t_{ESBAWC}		3.13		3.60		4.13	ns
t_{ESBSWC}		2.76		3.18		3.65	ns
$t_{ESBWASU}$	1.19		1.37		1.57		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.44		1.66		1.91		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.88		2.17		2.49		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.60		1.85		2.12		ns
$t_{ESBDATASU}$	0.74		0.85		0.98		ns
$t_{ESBWADDRSU}$	0.82		0.94		1.08		ns
$t_{ESBRADDRSU}$	0.73		0.84		.97		ns
$t_{ESBDATACO1}$		1.09		1.25		1.44	ns
$t_{ESBDATACO2}$		1.73		1.99		2.29	ns
t_{ESBDD}		3.26		3.75		4.32	ns
t_{PD}		1.55		1.78		2.05	ns
$t_{PTERMSU}$	0.99		1.13		1.30		ns
$t_{PTERMCO}$		0.79		0.90		1.04	ns

Table 62. EP2A40 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.17		0.19		0.22		ns
t_{F5-20}	1.12		1.28		1.48		ns
t_{F20+}	1.49		1.72		1.98		ns

Table 73. EP2A40 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.00		2.16		2.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.96	2.00	5.29	2.00	5.64	ns
t_{XZ}		7.04		7.59		8.19	ns
t_{ZX}		7.04		7.59		8.19	ns
$t_{INSUPLL}$	1.20		1.31		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.66	0.50	2.87	0.50	3.09	ns
t_{XZPLL}		4.74		5.17		5.64	ns
t_{ZXPLL}		4.74		5.17		5.64	ns

Table 74. EP2A70 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.48		2.68		2.90		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.76	2.00	5.12	2.00	5.51	ns
t_{XZ}		5.68		6.19		6.76	ns
t_{ZX}		5.68		6.19		6.76	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.52	0.50	2.74	0.50	2.98	ns
t_{XZPLL}		3.44		3.82		4.23	ns
t_{ZXPLL}		3.44		3.82		4.23	ns