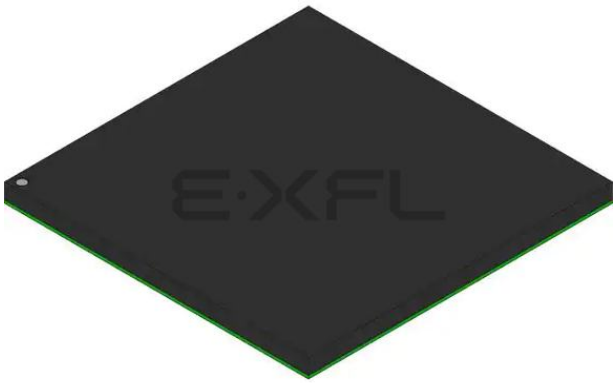


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	492
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a25f672c9

After an APEX II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Software

APEX II devices are supported by the Altera Quartus II development system: a single, integrated package that offers hardware description language (HDL) and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software includes the LogicLock incremental design feature. The LogicLock feature allows the designer to make pin and timing assignments, verify functionality and performance, and then set constraints to lock down the placement and performance of a specific block of logic using LogicLock constraints. Constraints set by the LogicLock function guarantee repeatable placement when implementing a block of logic in a current project or exporting the block to another project. The constraints set by the LogicLock feature can lock down logic to a fixed location in the device. The LogicLock feature can also lock the logic down to a floating location, and the Quartus II software determines the best relative placement of the block to meet design requirements. Adding additional logic to a project will not affect the performance of blocks locked down with LogicLock constraints.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can open the Quartus II software from within third-party design tools. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX II devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX II architecture.

Functional Description

APEX II devices incorporate LUT-based logic, product-term-based logic, memory, and high-speed I/O standards into one device. Signal interconnections within APEX II devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Figure 1. APEX II Device Block Diagram

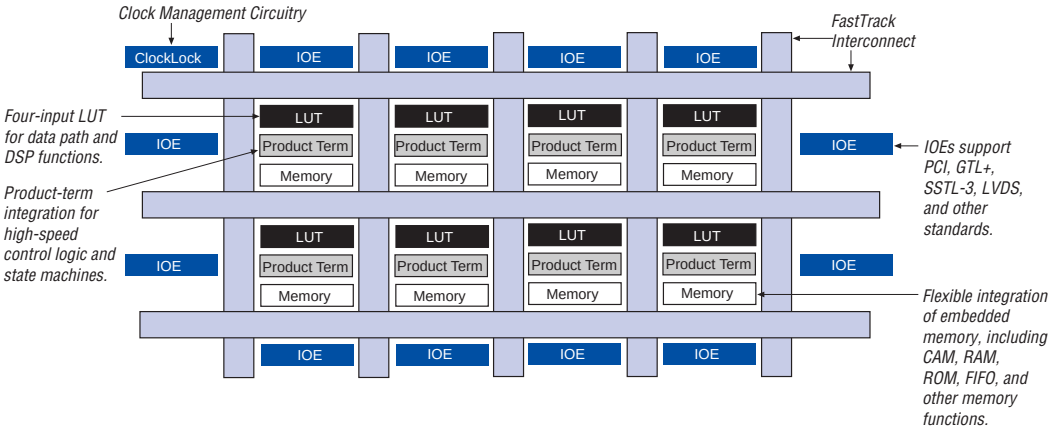


Table 4 lists the resources available in APEX II devices.

Table 4. APEX II Device Resources

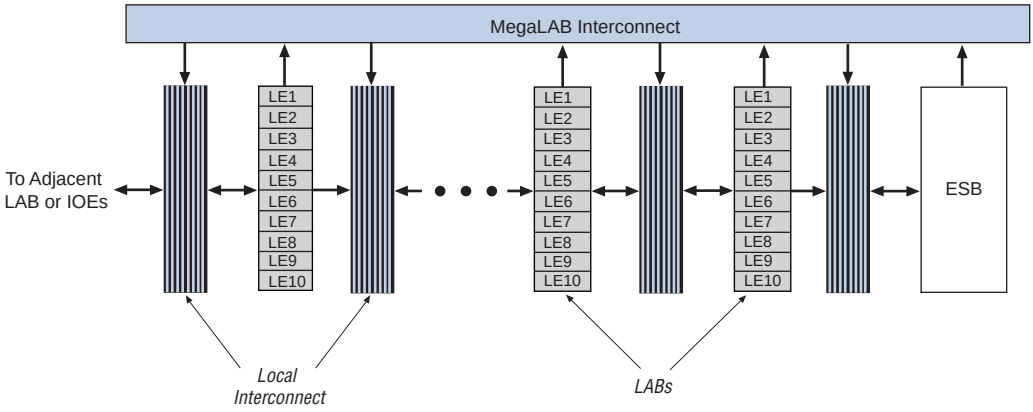
Device	MegaLAB Rows	MegaLAB Columns	ESBs
EP2A15	26	4	104
EP2A25	38	4	152
EP2A40	40	4	160
EP2A70	70	4	280

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



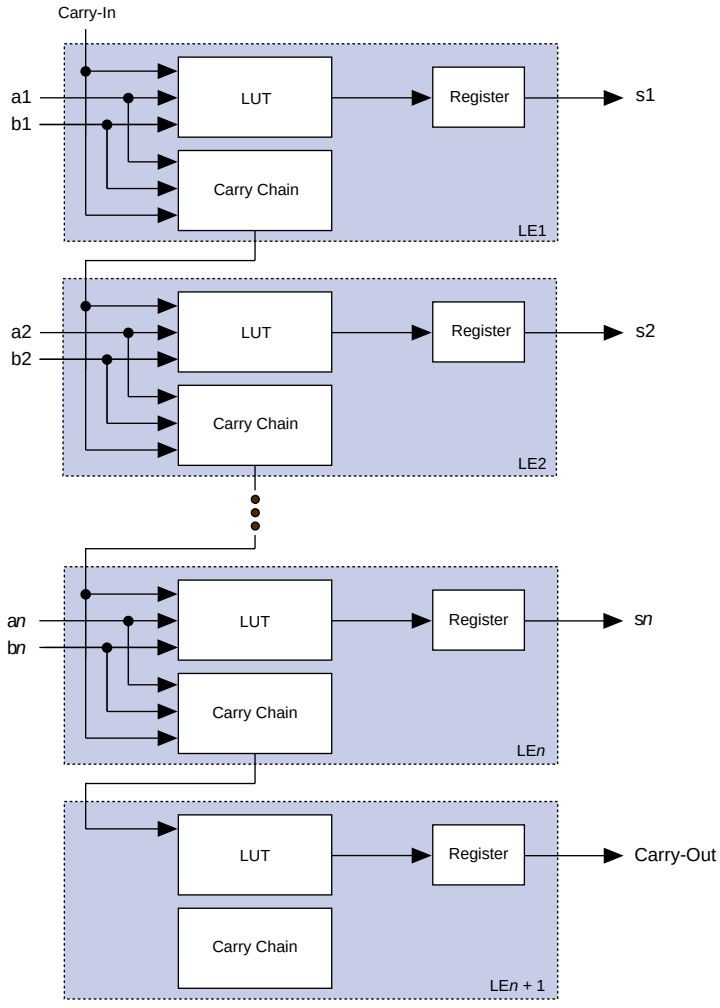
Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

Figure 6. APEX II Carry Chain



Cascade Chain

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX II Cascade Chain

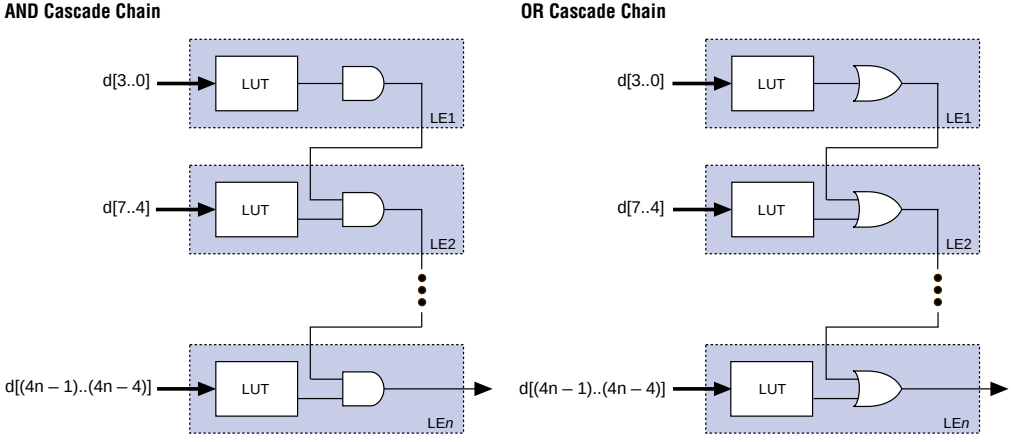
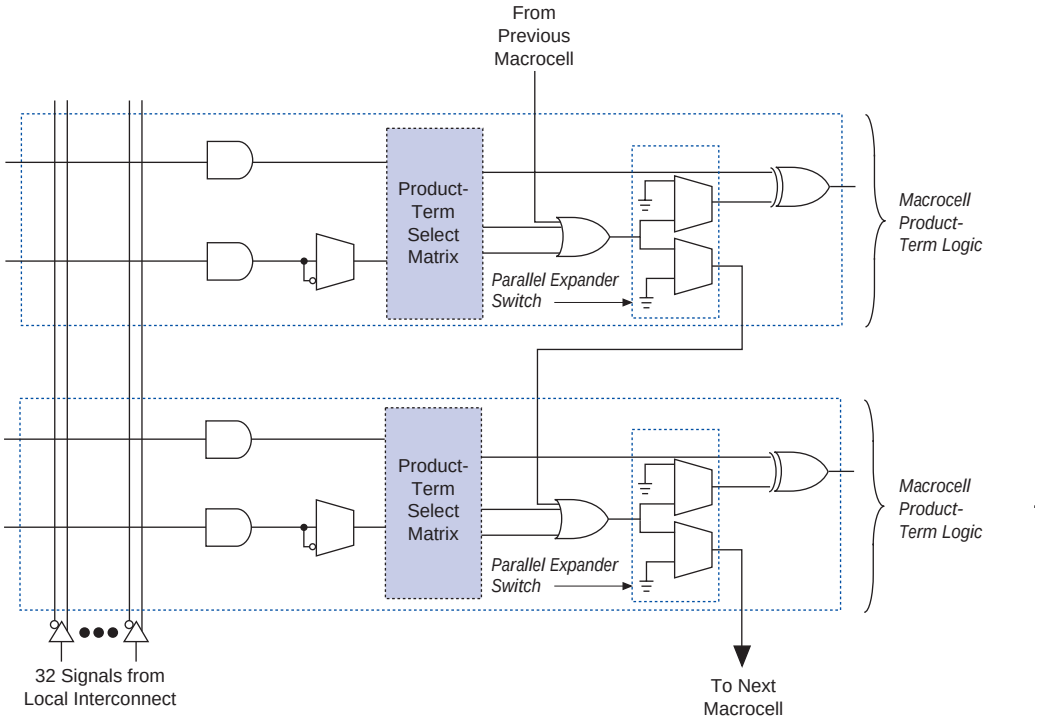


Figure 16. APEX II Parallel Expanders

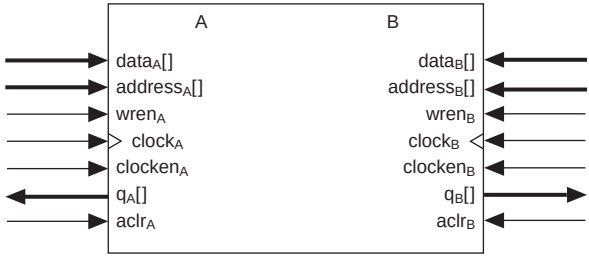


Embedded System Block

The ESB can implement various types of memory blocks, including Dual-Port+ RAM (bidirectional dual-port RAM), dual- and single-port RAM, ROM, FIFO, and CAM blocks.

The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a bidirectional, dual-port mode, which supports any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 17 shows the ESB block diagram.

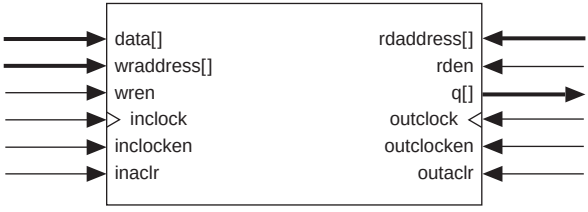
Figure 17. Bidirectional Dual-Port Memory Configuration



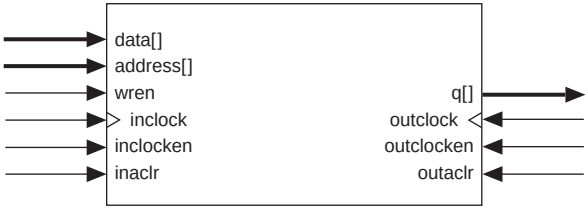
In addition to bidirectional dual-port memory, the ESB also supports dual-port, and single-port RAM. Dual-port memory supports a simultaneous read and write. Single-port memory supports independent read and write. Figure 18 shows these different RAM memory port configurations for an ESB.

Figure 18. Dual- & Single-Port Memory Configurations

Dual-Port Memory



Single-Port Memory *(1)*



Note to Figure 18:

(1) Two single-port memory blocks can be implemented in a single ESB.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data's location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 21 and 22 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 22. Encoded CAM Address Outputs

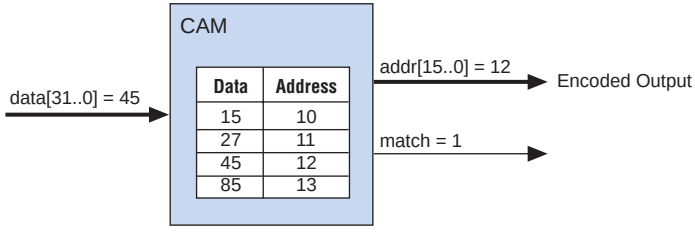
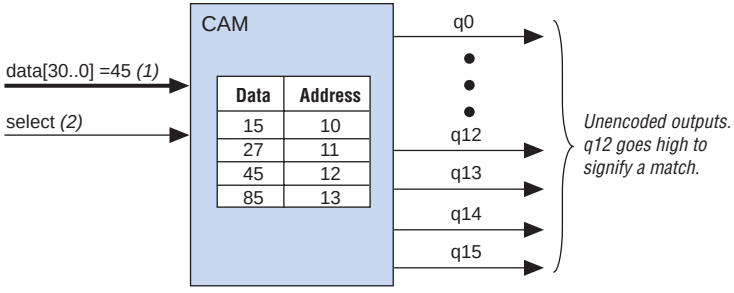


Figure 23. Unencoded CAM Address Outputs



Notes to Figures 22 and 23:

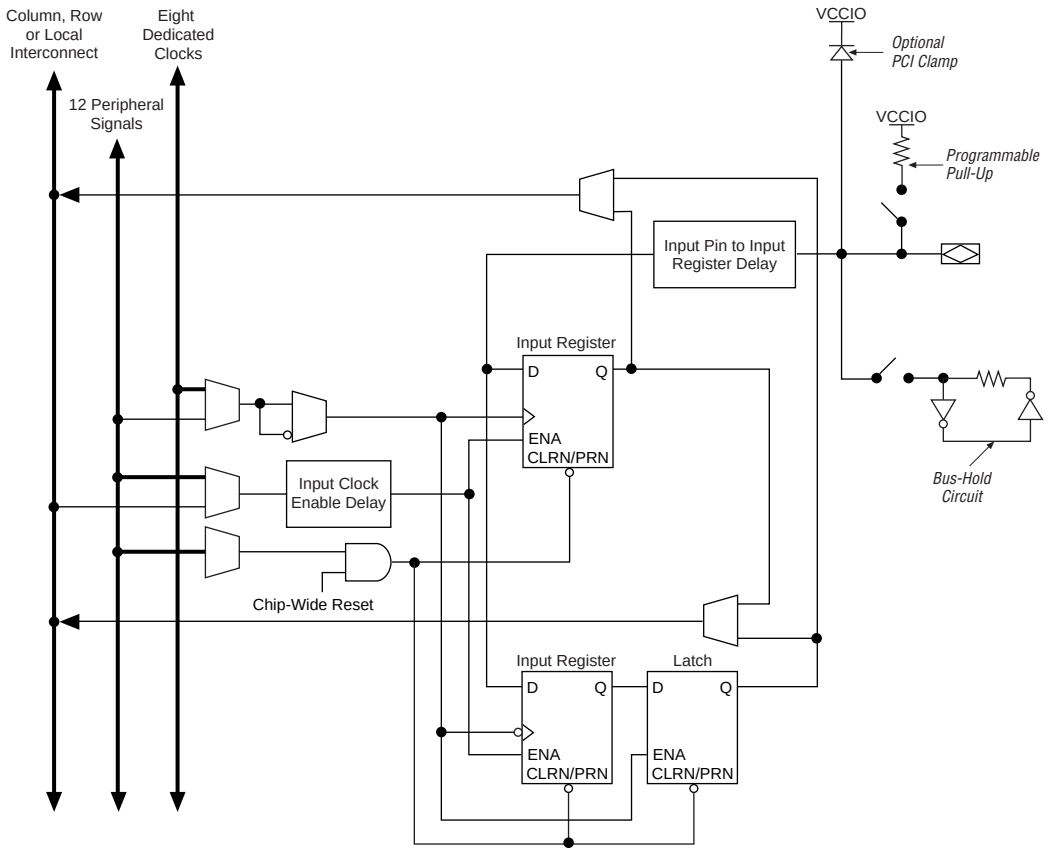
(1) For an unencoded output, the ESB only supports 31 input data bits. One input bit is used by the `select` line to choose one of the two banks of 16 outputs.

(2) If the `select` input is a 1, then CAM outputs odd words between 1 through 15. If the `select` input is a 0, CAM outputs even words between 0 through 14.

In single-match mode, it takes two clock cycles to write into CAM, but only one clock cycle to read from CAM. In this mode, both encoded and unencoded outputs are available without external logic. Single-match mode is better suited for designs without duplicate data in the memory.

When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, APEX II device I/O pins also support interfacing with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) delay ensures that the t_{ZX} is greater than the clock-to-high-impedance time (t_{XZ}). Phase delay control of clocks to the OE/output and input registers using two general-purpose PLLs enable the APEX II device to meet ZBT t_{CO} and t_{SU} times.

Programmable Drive Strength

The output buffer for each APEX II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, 3.3-V GTL+, PCI, and PCI-X support a minimum setting. The minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 9 shows the possible settings for the I/O standards with drive strength control.

Table 10 describes the I/O standards supported by APEX II devices.

Table 10. APEX II Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	N/A	1.5	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
HSTL class I and II	Voltage referenced	0.75	1.5	0.75
SSTL-2 class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage referenced	1.5	3.3	1.5
AGP (1× and 2×)	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Note to Table 10:

(1) Differential HSTL is only supported on the eight dedicated global clock pins and four dedicated high-speed PLL clock pins.

For more information on I/O standards supported by APEX II devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

APEX II devices contain eight I/O banks, as shown in Figure 31. Two blocks within the right I/O banks contain circuitry to support high-speed True-LVDS, LVPECL, PCML, and HyperTransport inputs, and another two blocks within the left I/O banks support high-speed True-LVDS, LVPECL, PCML, and HyperTransport outputs. All other standards are supported by all I/O banks.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

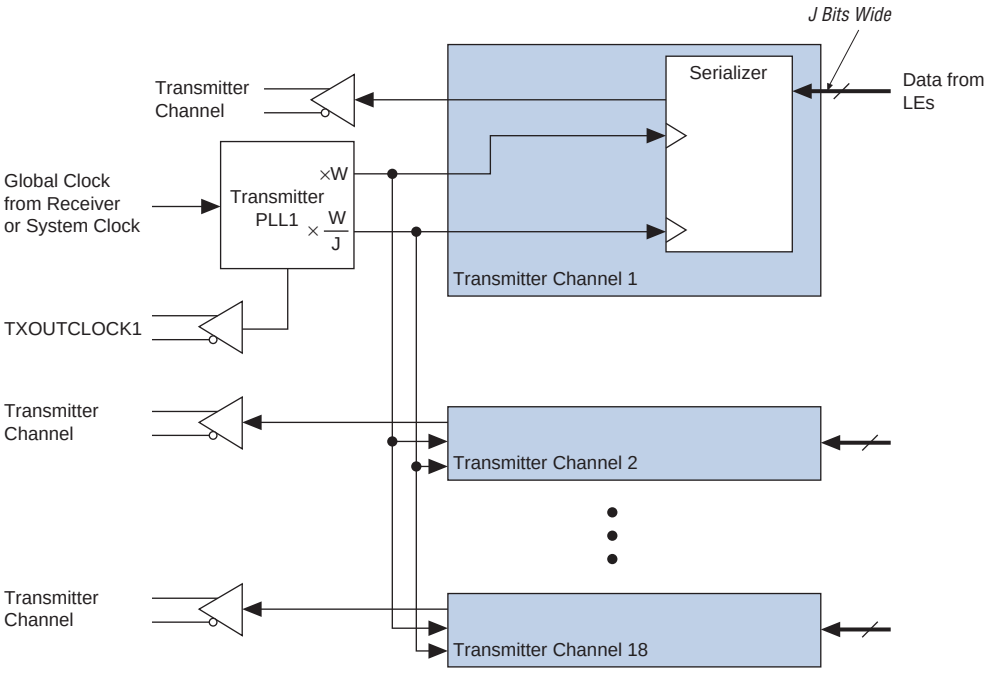
The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Figure 33. True-LVDS Transmitter Diagram *Notes (1), (2)*



Notes to Figure 33:

(1) Two sets of 18 transmitter channels are located in each APEX II device. Each set of 18 channels has one transmitter PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

Clock-Data Synchronization

In addition to dedicated serial-to-parallel converters, APEX II True-LVDS circuitry contains CDS circuitry in every receiver channel. The CDS feature can be turned on or off independently for each receiver channel. There are two modes for the CDS circuitry: single-bit mode, which corrects a fixed clock-to-data skew of up to ±50% of the data bit period, and multi-bit mode, which corrects any fixed clock-to-data skew.

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.
(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.
(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.
(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

Signals can be driven into APEX II devices before and during power-up without damaging the device. In addition, APEX II devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX II devices operate as specified by the user.

General-Purpose PLLs

APEX II devices have ClockLock, ClockBoost, and ClockShift features, which use four general-purpose PLLs (separate from the four dedicated True-LVDS PLLs) to provide clock management and clock-frequency synthesis. These PLLs allow designers to increase performance and provide clock-frequency synthesis. The PLL reduces the clock delay within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The PLLs, which provide programmable multiplication, allow the designer to distribute a low-speed clock and multiply that clock on-device. APEX II devices include a high-speed clock tree: unlike ASICs, the user does not have to design and optimize the clock tree. The PLLs work in conjunction with the APEX II device's high-speed clock to provide significant improvements in system performance and bandwidth.

The PLLs in APEX II devices are enabled through the Quartus II software. External devices are not required to use these features. Table 15 shows the general-purpose PLL features for APEX II devices. Figure 35 shows an APEX II general-purpose PLL.

Table 15. APEX II General-Purpose PLL Features

Number of PLLs	ClockBoost Feature	Number of External Clock Outputs	Number of Feedback Inputs
4	$m/(n \times k, v)$	8	2

Figure 35. APEX II General-Purpose PLL *Note (1)*

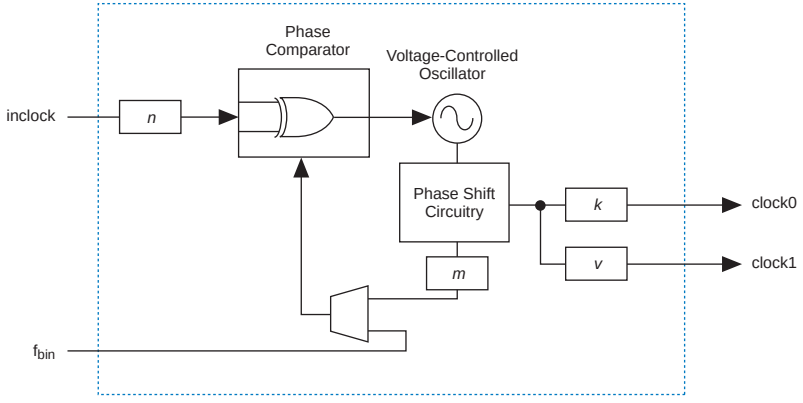


Table 34. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(10)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(10)*			V_{TT} – 0.8	V

Table 35. 3.3-V AGP 2× Specifications

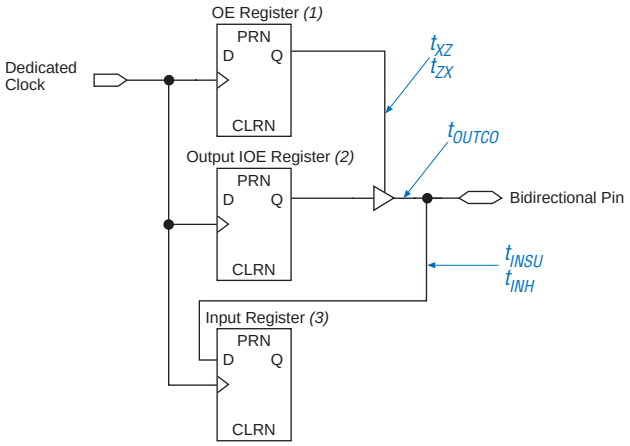
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 36. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Figure 42 shows the timing model for bi-directional, input, and output IOE timing.

Figure 42. Synchronous External TIming Model



Notes to Figure 42:

(1) The output enable register is in the IOE and is controlled by the "Fast Output Enable Register = ON" option in the Quartus II software.

(2) The output register is in the IOE and is controlled by the "Fast Output Register = ON" option in the Quartus II software.

(3) The input register is in the IOE and is controlled by the "Fast Input Register = ON" option in the Quartus II software.

Tables 47 through 50 show APEX II LE, ESB, and routing delays and minimum pulse-width timing parameters for the f_{MAX} timing model.

Table 47. APEX II f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 59. EP2A25 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.50		2.12		ns
t_{CL}	1.00		1.50		2.12		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.50		2.12		ns
t_{ESBCL}	1.00		1.50		2.12		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 60. EP2A40 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.26		0.29		ns
t_{H}	0.22		0.26		0.29		ns
t_{CO}		0.16		0.18		0.21	ns
t_{LUT}		0.48		0.55		0.63	ns

Table 71. EP2A25 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.27		2.45		2.64		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.57	2.00	4.89	2.00	5.24	ns
t_{XZ}		5.87		6.42		7.01	ns
t_{ZX}		5.87		6.42		7.01	ns
$t_{INSUPLL}$	1.23		1.35		1.47		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.89	0.50	3.10	0.50	3.33	ns
t_{XZPLL}		4.18		4.62		5.09	ns
t_{ZXPLL}		4.18		4.62		5.09	ns

Table 72. EP2A40 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.57		1.72		1.88		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.90	2.00	5.24	2.00	5.61	ns
t_{XZ}		6.47		6.98		7.53	ns
t_{ZX}		6.47		6.98		7.53	ns
$t_{INSUPLL}$	1.15		1.26		1.38		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.82	0.50	3.06	ns
t_{XZPLL}		4.17		4.56		4.97	ns
t_{ZXPLL}		4.17		4.56		4.97	ns

Table 76. APEX II Selectable I/O Standards Input Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		0.10		0.11		0.12	ns
1.8 V		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
3.3-V PCI		0.00		0.00		0.00	ns
3.3-V PCI-X		0.00		0.00		0.00	ns
GTL+		– 0.20		– 0.22		– 0.24	ns
SSTL-3 Class I		– 0.17		– 0.19		– 0.20	ns
SSTL-3 Class II		– 0.17		– 0.19		– 0.20	ns
SSTL-2 Class I		– 0.24		– 0.26		– 0.29	ns
SSTL-2 Class II		– 0.24		– 0.26		– 0.29	ns
HSTL Class I		– 0.03		– 0.03		– 0.03	ns
HSTL Class II		– 0.03		– 0.03		– 0.03	ns
LVDS		– 0.23		– 0.26		– 0.28	ns
LVPECL		– 0.23		– 0.26		– 0.28	ns
PCML		– 0.23		– 0.26		– 0.28	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 0.23		– 0.26		– 0.28	ns
Differential HSTL		– 0.23		– 0.26		– 0.28	ns