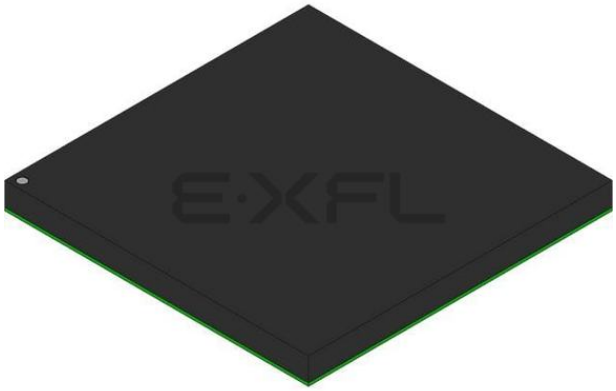


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

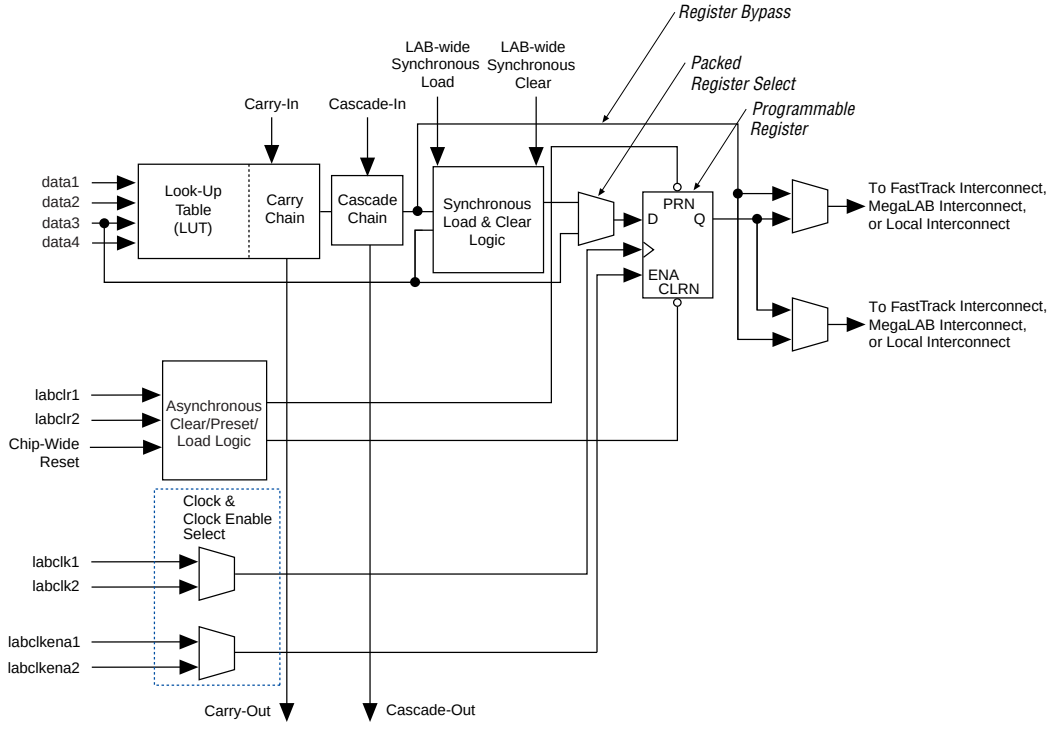
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	655360
Number of I/O	540
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	724-BBGA, FCBGA
Supplier Device Package	724-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a40b724c8

Figure 5. APEX II Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

LE Operating Modes

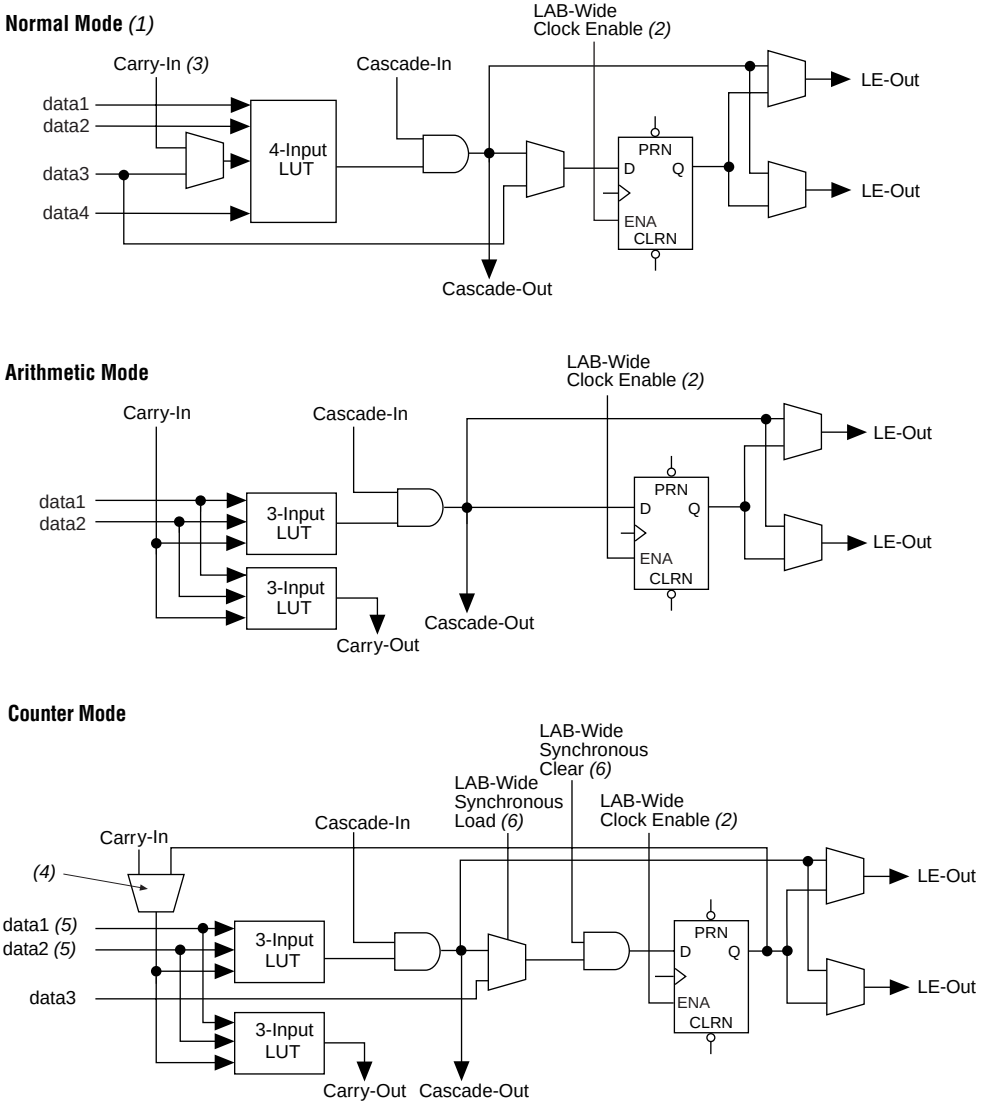
The APEX II LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 8. APEX II LE Operating Modes



Notes to Figure 8:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in a LAB.
(6) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in a LAB.

Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

Arithmetic Mode

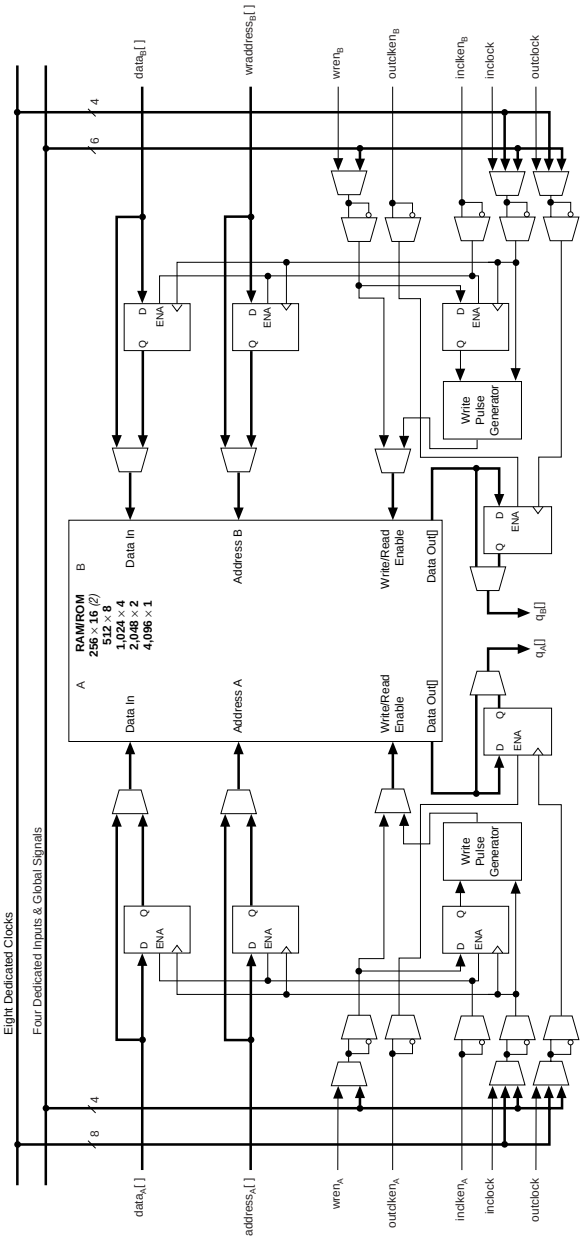
The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

Counter Mode

The counter mode offers clock enable, counter enable, synchronous up / down control, synchronous clear, and synchronous load options. The counter enable and synchronous up / down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 19. ESB in Input/Output Clock Mode *Note (1)*



Notes to Figure 19:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

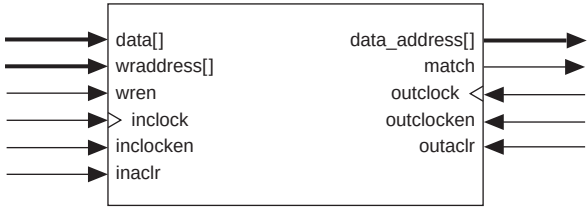
(2) This configuration is not supported for bidirectional dual-port configuration.

Content-Addressable Memory

APEX II devices can implement CAM in ESBs. CAM can be thought of as the inverse of RAM. RAM stores data in a specific location; when the system submits an address, the RAM block provides the data. Conversely, when the system submits data to CAM, the CAM block provides the address where the data is found. For example, if the data FA12 is stored in address 14, the CAM outputs 14 when FA12 is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. CAM is ideally suited for applications such as Ethernet address lookup, data compression, pattern recognition, cache tags, fast routing table lookup, and high-bandwidth address filtering. Figure 21 shows the CAM block diagram.

Figure 21. CAM Block Diagram



The APEX II on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX II device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements a 32-word, 32-bit CAM. Wider or deeper CAM, such as a 32-word, 64-bit or 128-word, 32-bit block, can be implemented by combining multiple CAM blocks with some ancillary logic implemented in LEs. The Quartus II software automatically combines ESBs and LEs to create larger CAM blocks.

CAM supports writing “don’t care” bits into words of the memory. The don’t-care bit can be used as a mask for CAM comparisons; any bit set to don’t-care has no effect on matches.

CAM can generate outputs in three different modes: single-match mode, multiple-match mode, and fast multiple-match mode. In each mode, the ESB outputs the matched data's location as an encoded or unencoded address. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address 12, the ESB output is 12. When unencoded, each ESB port uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address 12, the 12th output line goes high. Figures 21 and 22 show the encoded CAM outputs and unencoded CAM outputs, respectively.

Figure 22. Encoded CAM Address Outputs

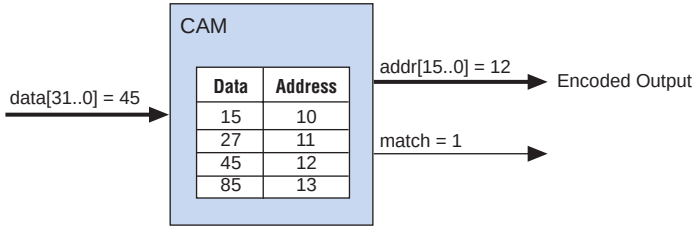
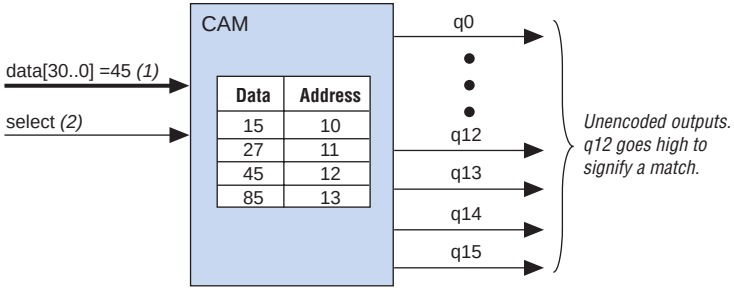


Figure 23. Unencoded CAM Address Outputs



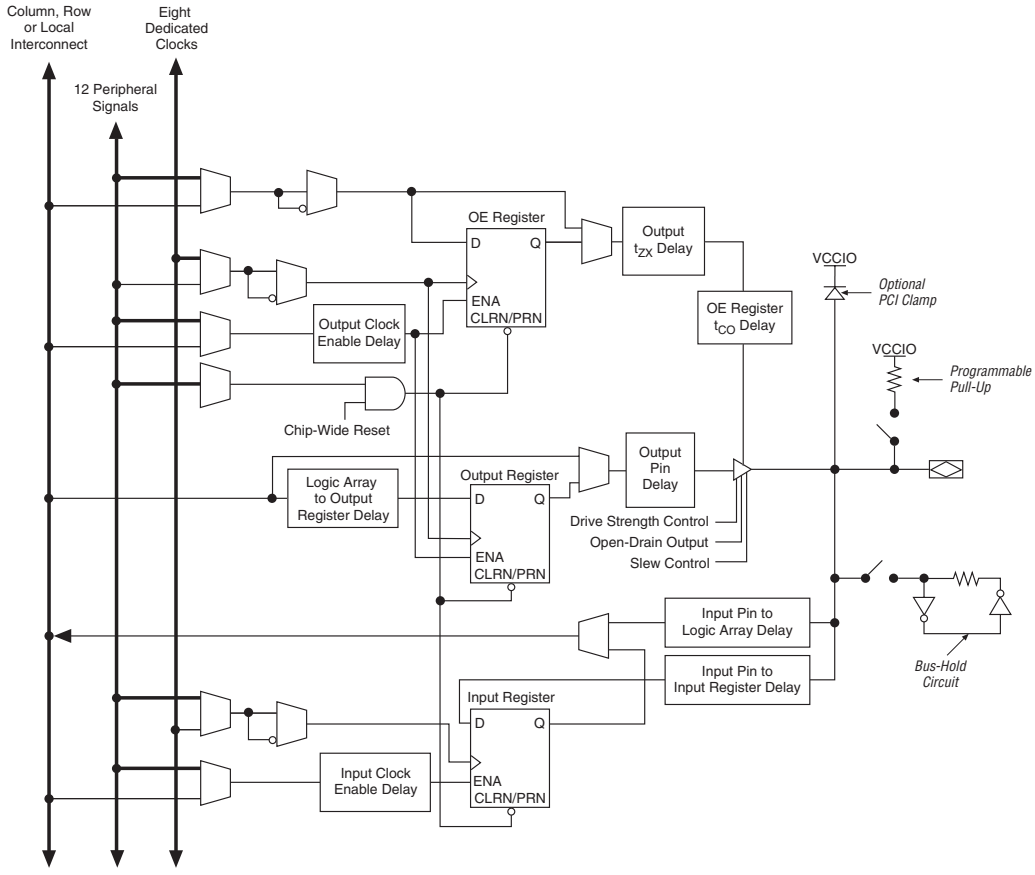
Notes to Figures 22 and 23:

(1) For an unencoded output, the ESB only supports 31 input data bits. One input bit is used by the `select` line to choose one of the two banks of 16 outputs.

(2) If the `select` input is a 1, then CAM outputs odd words between 1 through 15. If the `select` input is a 0, CAM outputs even words between 0 through 14.

In single-match mode, it takes two clock cycles to write into CAM, but only one clock cycle to read from CAM. In this mode, both encoded and unencoded outputs are available without external logic. Single-match mode is better suited for designs without duplicate data in the memory.

Figure 28. APEX II IOE in Bidirectional I/O Configuration



The APEX II IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

Bus Hold

Each APEX II device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signal is present, the bus-hold feature eliminates the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. The bus-hold feature should also be disabled if open-drain outputs are used with the GTL+ I/O standard.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ. Table 41 on page 74 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each APEX II device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the bank that the output pin resides in.

Dedicated Fast I/O Pins

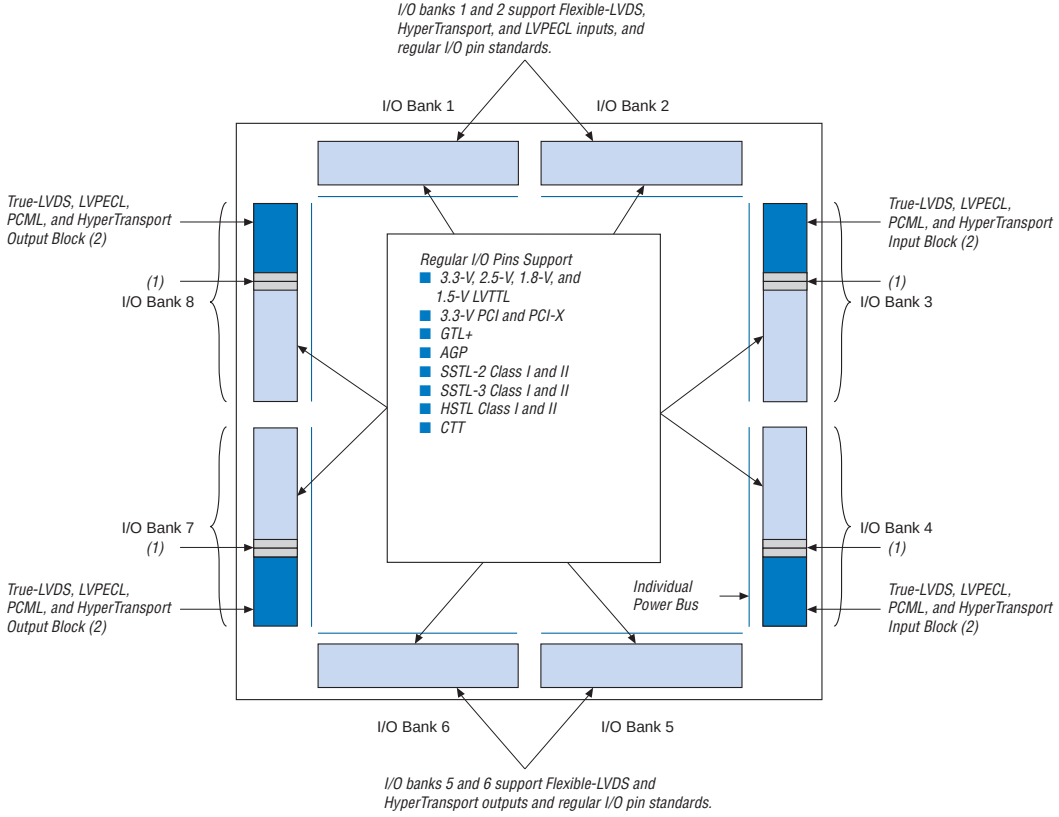
APEX II devices incorporate dedicated bidirectional pins for signals with high internal fanout, such as PCI control signals. These pins are called dedicated fast I/O pins (FAST1, FAST2, FAST3, and FAST4) and can drive the four global fast lines throughout the device, ideal for fast clock, clock enable, preset, clear, or high fanout logic signal distribution. The dedicated fast I/O pins have one output register and one OE register, but they do not have input registers. The dedicated fast lines can also be driven by a LE local interconnect to generate internal global signals.

Advanced I/O Standard Support

APEX II device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5-V
- 1.8-V
- 2.5-V
- 3.3-V PCI
- 3.3-V PCI-X
- 3.3-V AGP (1×, 2×)
- LVDS
- LVPECL
- PCML
- HyperTransport
- GTL+
- HSTL class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- CTT
- Differential HSTL

Figure 31. APEX II I/O Banks



Notes to Figure 31:

(1) For more information on placing I/O pins within LVDS blocks, refer to the "High-Speed Interface Pin Location" section in *Application Note 166 (Using High-Speed I/O Standards in APEX II Devices)*.

(2) If the True-LVDS pins or the Flexible-LVDS pins are not used for high-speed differential signalling, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with V_{CCIO} set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V. However, True-LVDS pins do not support the HSTL Class II output.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate V_{REF} level to support any one of the terminated standards (such as SSTL-3) independently.

Pre-programmed CDS may also be used to resolve clock-to-data skew greater than 50% of the bit period. However, internal logic must be used to implement the byte alignment circuitry for this operation.

Flexible-LVDS I/O Pins

A subset of pins in the top two I/O banks supports interfacing with Flexible-LVDS, LVPECL, and HyperTransport inputs. These Flexible-LVDS input pins include dedicated LVDS, LVPECL, and HyperTransport input buffers. A subset of pins in the bottom two I/O banks supports interfacing with Flexible-LVDS and HyperTransport outputs. These Flexible-LVDS output pins include dedicated LVDS and HyperTransport output buffers. The Flexible-LVDS pins do not require any external components except for 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization/deserialization circuitry; therefore, internal logic is used to perform serialization/deserialization functions.

The EP2A15 and EP2A25 devices support 56 input and 56 output Flexible-LVDS channels. The EP2A40 and larger devices support 88 input and 88 output Flexible-LVDS channels. All APEX II devices support the Flexible-LVDS interface up to 400 Mbps (DDR) per channel. Flexible-LVDS pins along with the True-LVDS pins provide up to 144-Gbps total device bandwidth. Table 13 shows the Flexible-LVDS timing specification.

Table 13. APEX II Flexible-LVDS Timing Specification

Symbol	Timing Parameter Definition	Speed Grade						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Data Rate	Maximum operating speed		400		311		311	Mbps
TCCS	Transmitter channel-to-channel skew		700		900		900	ps
SW	Receiver sampling window	1,100		1,400		1,400		ps

MultiVolt I/O Interface

The APEX II architecture supports the MultiVolt I/O interface feature, which allows APEX II devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

Signals can be driven into APEX II devices before and during power-up without damaging the device. In addition, APEX II devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX II devices operate as specified by the user.

General-Purpose PLLs

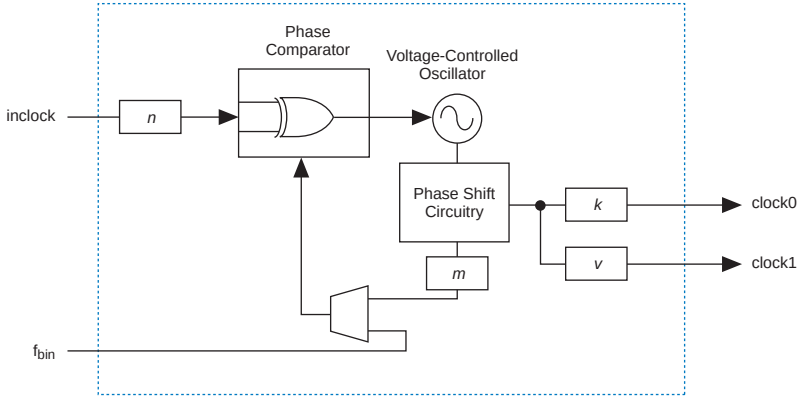
APEX II devices have ClockLock, ClockBoost, and ClockShift features, which use four general-purpose PLLs (separate from the four dedicated True-LVDS PLLs) to provide clock management and clock-frequency synthesis. These PLLs allow designers to increase performance and provide clock-frequency synthesis. The PLL reduces the clock delay within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The PLLs, which provide programmable multiplication, allow the designer to distribute a low-speed clock and multiply that clock on-device. APEX II devices include a high-speed clock tree: unlike ASICs, the user does not have to design and optimize the clock tree. The PLLs work in conjunction with the APEX II device's high-speed clock to provide significant improvements in system performance and bandwidth.

The PLLs in APEX II devices are enabled through the Quartus II software. External devices are not required to use these features. Table 15 shows the general-purpose PLL features for APEX II devices. Figure 35 shows an APEX II general-purpose PLL.

Table 15. APEX II General-Purpose PLL Features

Number of PLLs	ClockBoost Feature	Number of External Clock Outputs	Number of Feedback Inputs
4	$m/(n \times k, v)$	8	2

Figure 35. APEX II General-Purpose PLL *Note (1)*



For more information, see the following documents:

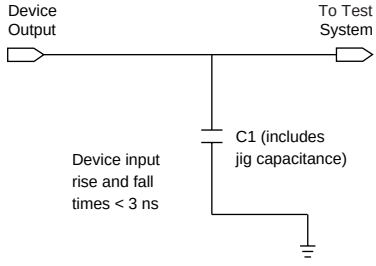
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX II device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX II devices are made under conditions equivalent to those shown in Figure 37. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Figure 37. APEX II AC Test Conditions



Operating Conditions

APEX II devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing structures ensure predictable performance, and accurate simulation and timing analysis. In contrast, the unpredictable performance of FPGAs is caused by their segmented connection scheme.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum drive strength.

Figure 41 shows the f_{MAX} timing model for APEX II devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. However, the Quartus II software timing analysis provides more accurate timing information because the Quartus II software usually has more up-to-date timing information than the data sheet until the timing model is final. Also, the Quartus II software can model delays caused by loading and distance effects more accurately than by using the numbers in this data sheet.

Table 48. APEX II f_{MAX} ESB Timing Parameters	
Symbol	**Parameter**
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Figure shows the dual-port RAM timing microparameter waveform.

Table 61. EP2A40 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		2.28		2.62		3.01	ns
t_{ESBSRC}		2.23		2.56		2.95	ns
t_{ESBAWC}		3.13		3.60		4.13	ns
t_{ESBSWC}		2.76		3.18		3.65	ns
$t_{ESBWASU}$	1.19		1.37		1.57		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.44		1.66		1.91		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	1.88		2.17		2.49		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.60		1.85		2.12		ns
$t_{ESBDATASU}$	0.74		0.85		0.98		ns
$t_{ESBWADDRSU}$	0.82		0.94		1.08		ns
$t_{ESBRADDRSU}$	0.73		0.84		.97		ns
$t_{ESBDATACO1}$		1.09		1.25		1.44	ns
$t_{ESBDATACO2}$		1.73		1.99		2.29	ns
t_{ESBDD}		3.26		3.75		4.32	ns
t_{PD}		1.55		1.78		2.05	ns
$t_{PTERMSU}$	0.99		1.13		1.30		ns
$t_{PTERMCO}$		0.79		0.90		1.04	ns

Table 62. EP2A40 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.17		0.19		0.22		ns
t_{F5-20}	1.12		1.28		1.48		ns
t_{F20+}	1.49		1.72		1.98		ns

Table 71. EP2A25 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.27		2.45		2.64		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.57	2.00	4.89	2.00	5.24	ns
t_{XZ}		5.87		6.42		7.01	ns
t_{ZX}		5.87		6.42		7.01	ns
$t_{INSUPLL}$	1.23		1.35		1.47		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.89	0.50	3.10	0.50	3.33	ns
t_{XZPLL}		4.18		4.62		5.09	ns
t_{ZXPLL}		4.18		4.62		5.09	ns

Table 72. EP2A40 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.57		1.72		1.88		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.90	2.00	5.24	2.00	5.61	ns
t_{XZ}		6.47		6.98		7.53	ns
t_{ZX}		6.47		6.98		7.53	ns
$t_{INSUPLL}$	1.15		1.26		1.38		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.82	0.50	3.06	ns
t_{XZPLL}		4.17		4.56		4.97	ns
t_{ZXPLL}		4.17		4.56		4.97	ns

Table 73. EP2A40 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.00		2.16		2.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.96	2.00	5.29	2.00	5.64	ns
t_{XZ}		7.04		7.59		8.19	ns
t_{ZX}		7.04		7.59		8.19	ns
$t_{INSUPLL}$	1.20		1.31		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.66	0.50	2.87	0.50	3.09	ns
t_{XZPLL}		4.74		5.17		5.64	ns
t_{ZXPLL}		4.74		5.17		5.64	ns

Table 74. EP2A70 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.48		2.68		2.90		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.76	2.00	5.12	2.00	5.51	ns
t_{XZ}		5.68		6.19		6.76	ns
t_{ZX}		5.68		6.19		6.76	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.52	0.50	2.74	0.50	2.98	ns
t_{XZPLL}		3.44		3.82		4.23	ns
t_{ZXPLL}		3.44		3.82		4.23	ns

Table 77. APEX II Selectable I/O Standards Output Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		3.32		3.82		4.20	ns
1.8 V		2.65		3.05		3.36	ns
2.5 V		1.20		1.38		1.52	ns
3.3-V PCI		– 0.68		– 0.78		– 0.85	ns
3.3-V PCI-X		– 0.68		– 0.78		– 0.85	ns
GTL+		– 0.45		– 0.52		– 0.57	ns
SSTL-3 Class I		– 0.52		– 0.60		– 0.66	ns
SSTL-3 Class II		– 0.52		– 0.60		– 0.66	ns
SSTL-2 Class I		– 0.68		– 0.78		– 0.86	ns
SSTL-2 Class II		– 0.81		– 0.93		– 1.02	ns
HSTL Class I		– 0.08		– 0.09		– 0.10	ns
HSTL Class II		– 0.23		– 0.27		– 0.30	ns
LVDS		– 1.41		– 1.62		– 1.79	ns
LVPECL		– 1.38		– 1.58		– 1.74	ns
PCML		– 1.30		– 1.50		– 1.65	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 1.22		– 1.41		– 1.55	ns
Differential HSTL		– 1.41		– 1.62		– 1.79	ns

Power Consumption

Detailed power consumption information for APEX II devices will be released via a future interactive power estimator on the Altera web site.

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.