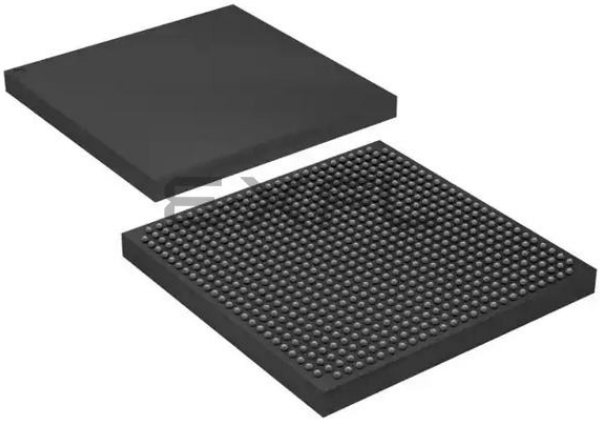


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	655360
Number of I/O	492
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2a40f672c7

Figure 1. APEX II Device Block Diagram

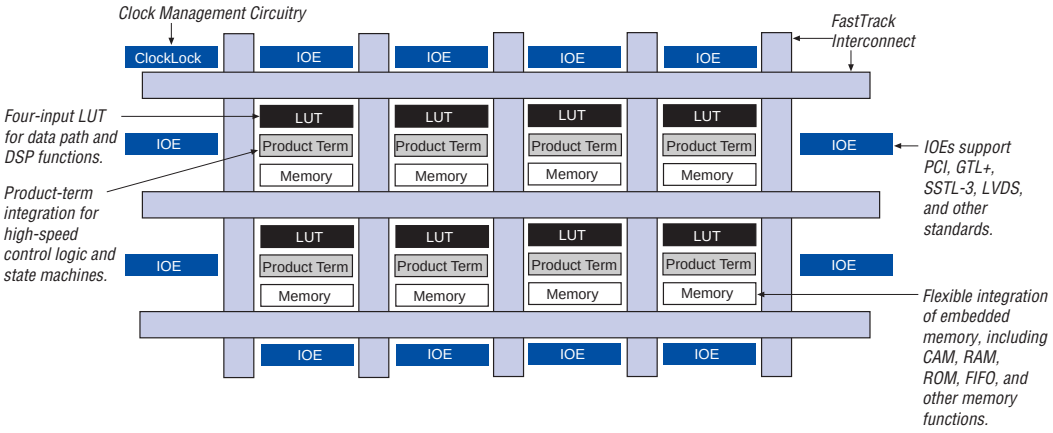


Table 4 lists the resources available in APEX II devices.

Table 4. APEX II Device Resources

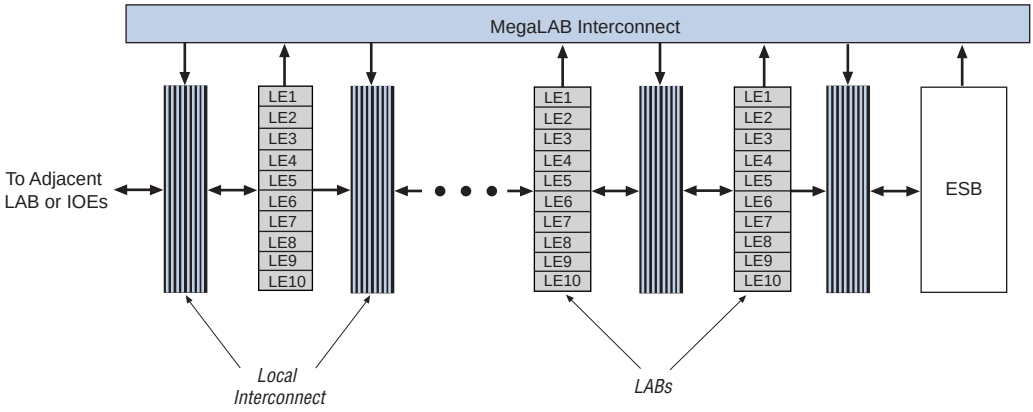
Device	MegaLAB Rows	MegaLAB Columns	ESBs
EP2A15	26	4	104
EP2A25	38	4	152
EP2A40	40	4	160
EP2A70	70	4	280

APEX II devices provide eight dedicated clock input pins and four dedicated fast I/O pins that globally drive register control inputs, including clocks. These signals ensure efficient distribution of high-speed, low-skew control signals. The control signals use dedicated routing channels to provide short delays and low skew. The dedicated fast signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally-generated asynchronous control signal with high fan-out. The dedicated clock and fast I/O pins on APEX II devices can also feed logic. Dedicated clocks can also be used with the APEX II general-purpose PLLs for clock management.

MegaLAB Structure

APEX II devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. EP2A15 and EP2A25 devices have 16 LABs and EP2A40 and EP2A70 devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

Figure 2. MegaLAB Structure



Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs.

The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance.

APEX II devices use an interleaved LAB structure, so that each LAB can drive two local interconnect areas. Every other LE drives to either the left or right local interconnect area, alternating by LE. The local interconnect can drive LEs within the same LAB or adjacent LABs. This feature minimizes the use of the row and column interconnects, providing higher performance and flexibility. Each LAB structure can drive 30 LEs through fast local interconnects.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

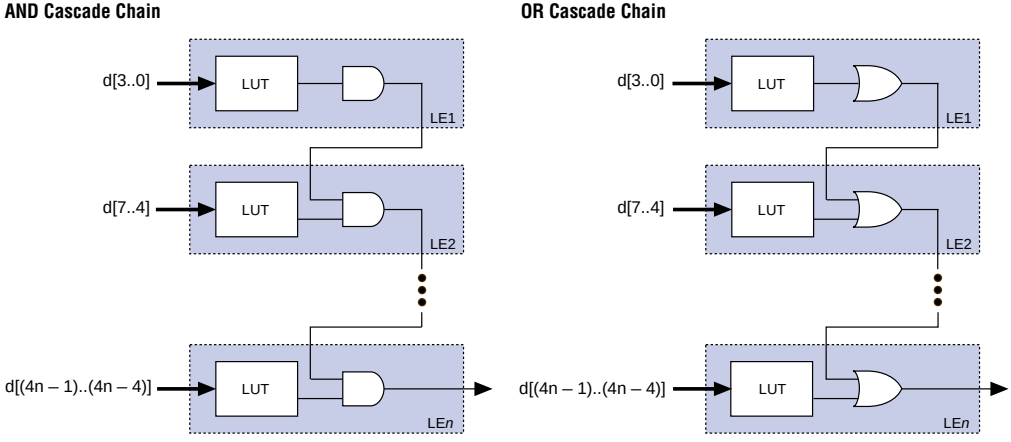
Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Cascade Chain

With the cascade chain, the APEX II architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via DeMorgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. The Quartus II Compiler can create cascade chain logic automatically during the design process, or the designer can create it manually during design entry.

Cascade chains longer than 10 LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

Figure 7. APEX II Cascade Chain



A column line can be directly driven by the LEs, IOEs, or ESBs in that column. Row IOEs can drive a column line on a device's left or right edge. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

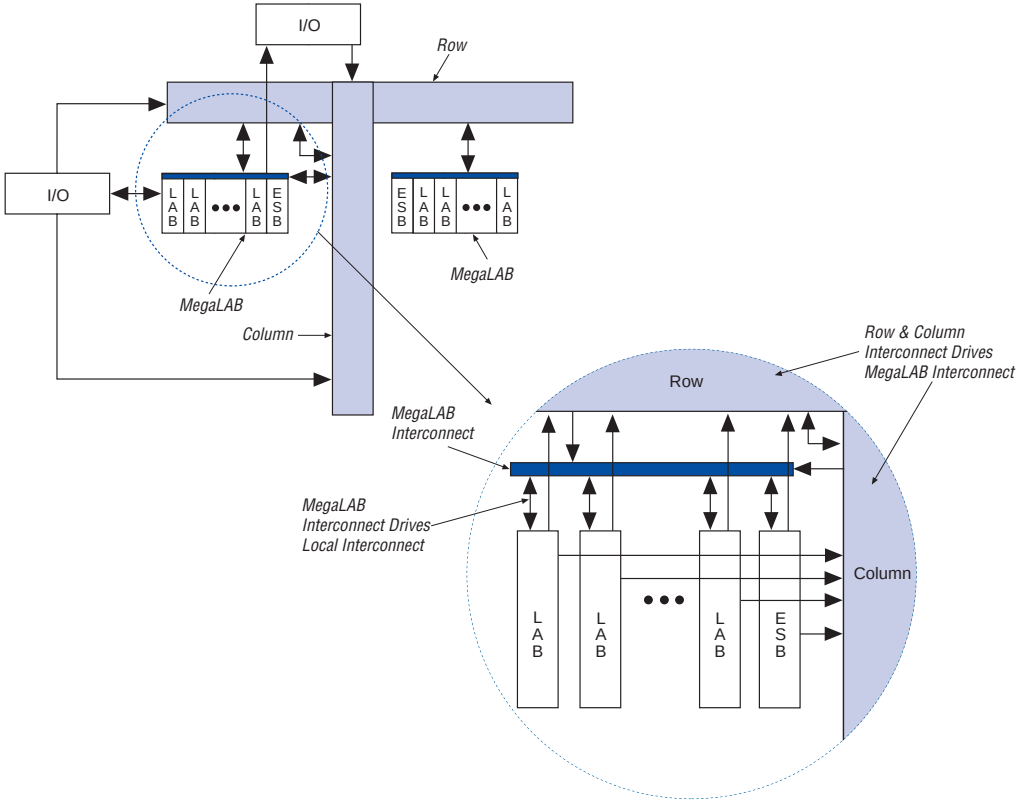


Figure 11 shows the intersection of a row and column interconnect and how these forms of interconnects and LEs drive each other.

By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 256 × 16 RAM blocks can be combined to form a 256 x 32 RAM block, and two 512 × 8 RAM blocks can be combined to form a 512 × 16 RAM block. Memory performance does not degrade for memory blocks up to 4,096 words deep. Each ESB can implement a 4,096-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic that would increase delays. To create a high-speed memory block more than 4,096-words deep, the Quartus II software automatically combines ESBs with LE control logic.

Input/Output Clock Mode

The ESB implements input/output clock mode for both dual-port and bidirectional dual-port memory. An ESB using input/output clock mode can use up to two clocks. On each of the two ports, A or B, one clock controls all registers for inputs into the ESB: data input, WREN, read address, and write address. The other clock controls the ESB data output registers. Each ESB port, A or B, also supports independent read clock enable, write clock enable, and asynchronous clear signals. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 19 shows the ESB in input/output clock mode.

If the same data is written into multiple locations in the memory, a CAM block can be used in multiple-match or fast multiple-match modes. The ESB outputs the matched data's locations as an encoded or unencoded address. In multiple-match mode, it takes two clock cycles to write into a CAM block. For reading, there are 16 outputs from each ESB at each clock cycle. Therefore, it takes two clock cycles to represent the 32 words from a single ESB port. In this mode, encoded and unencoded outputs are available. To implement the encoded version, the Quartus II software adds a priority encoder with LEs. Fast multiple-match is identical to the multiple match mode, however, it only takes one clock cycle to read from a CAM block and generate valid outputs. To do this, the entire ESB is used to represent 16 outputs. In fast multiple-match mode, the ESB can implement a maximum CAM block size of 16 words.

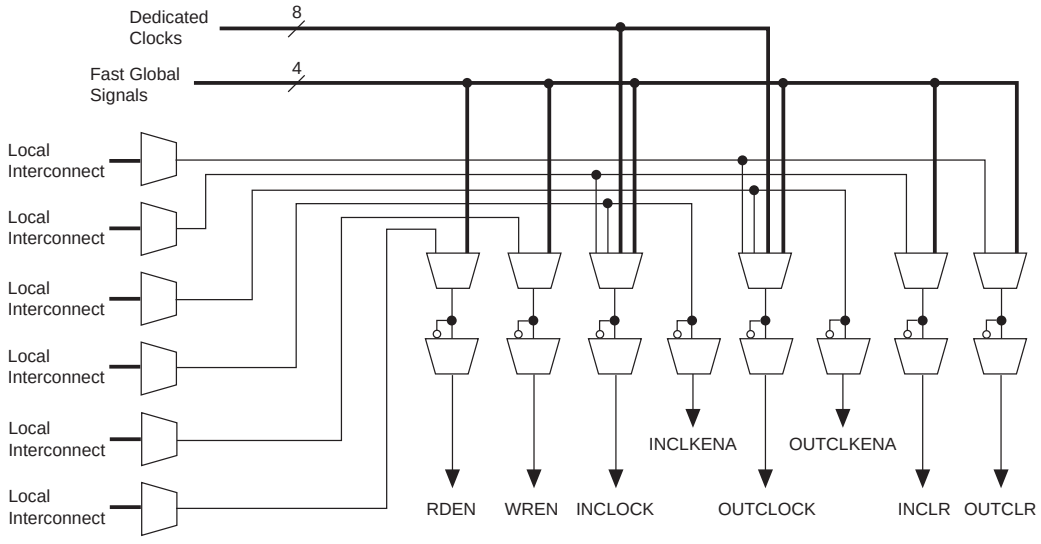
A CAM block can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When don't-care bits are used, a third clock cycle is required.

For more information on CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnects can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and synchronous clear signals. Figure 24 shows the ESB control signal generation logic.

Figure 24. ESB Control Signal Generation

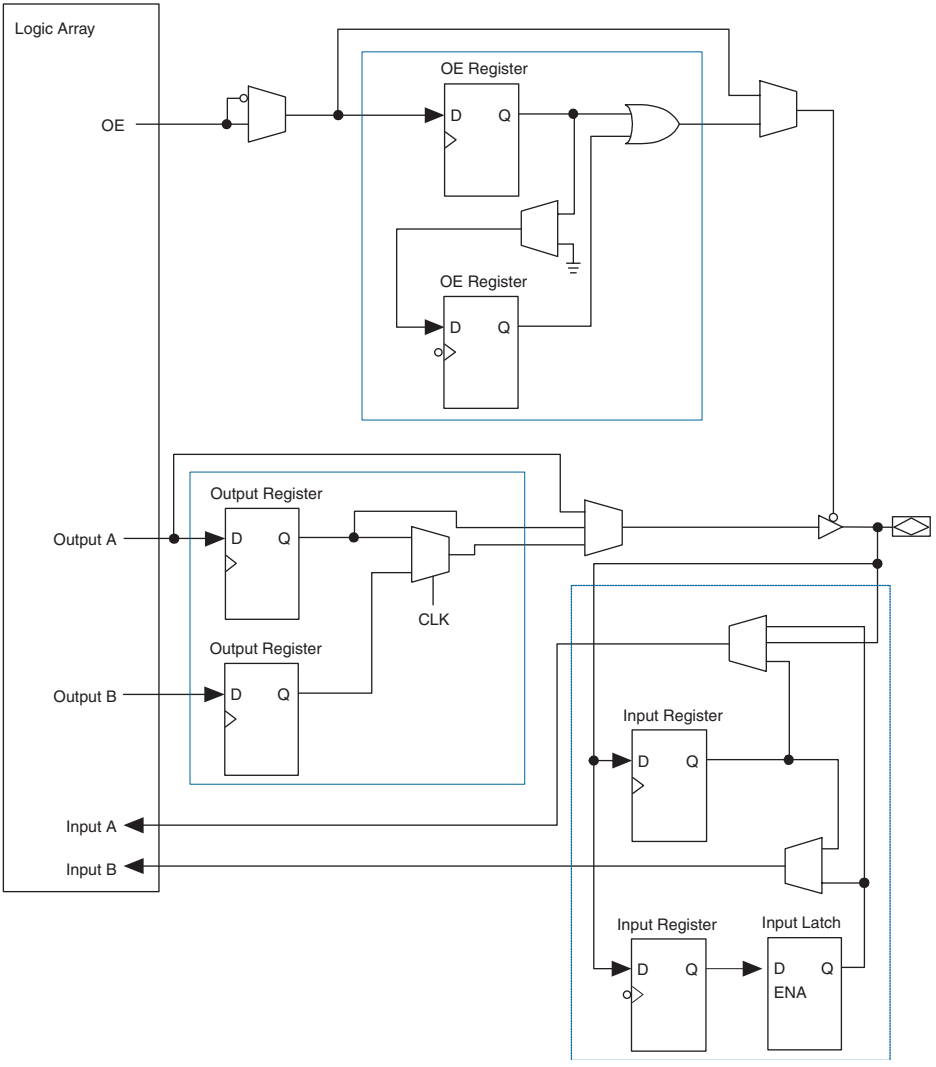


An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

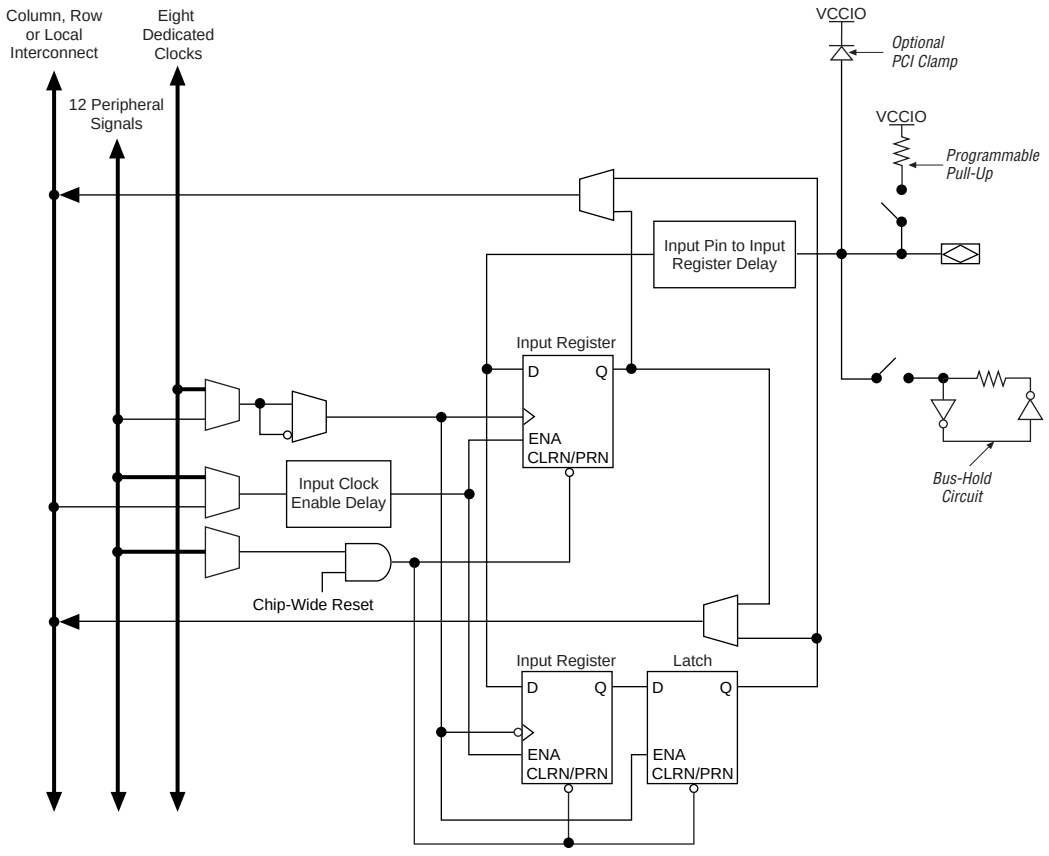
Figure 25. APEX II IOE Structure



The IOEs are located around the periphery of the APEX II device. Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the FastTrack or column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

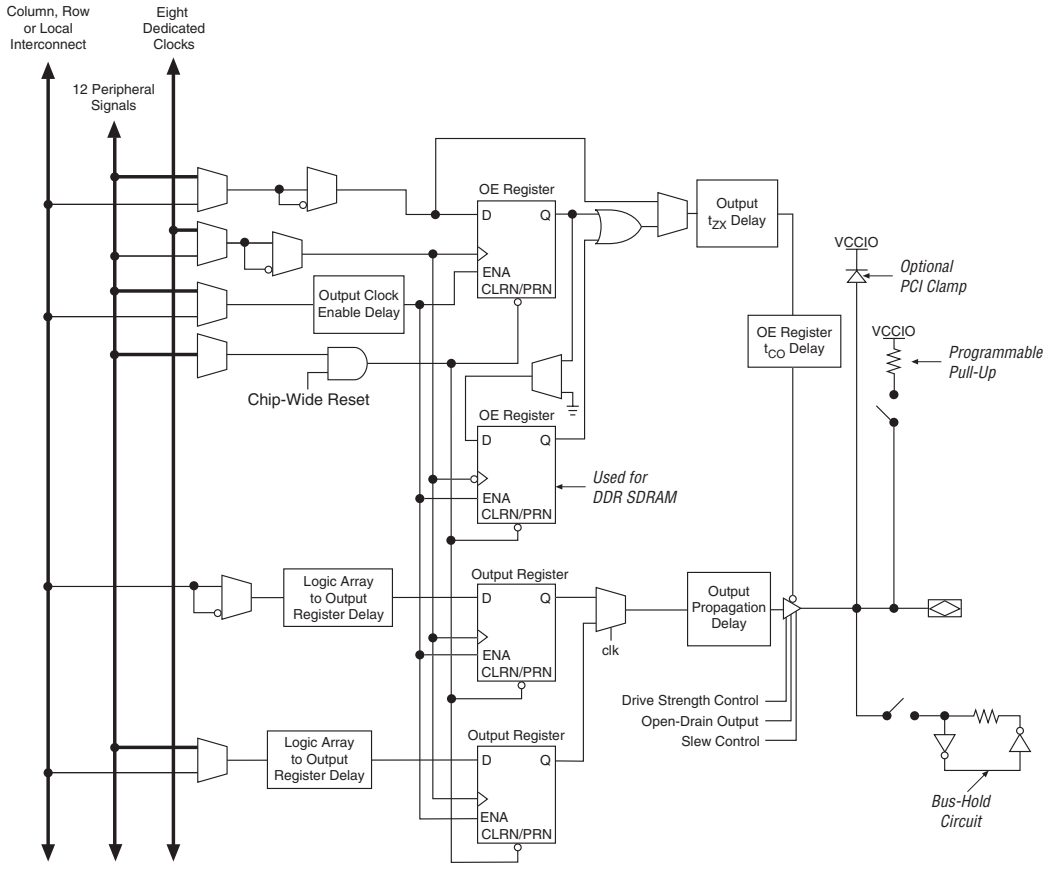
When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Figure 30. APEX II IOE in DDR Output I/O Configuration



The APEX II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations.

APEX II I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM at 167 MHz (334 Mbps). The negative-edge-clocked OE register is used to hold the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements. QDR SRAMs are also supported with DDR I/O pins on separate read and write ports.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

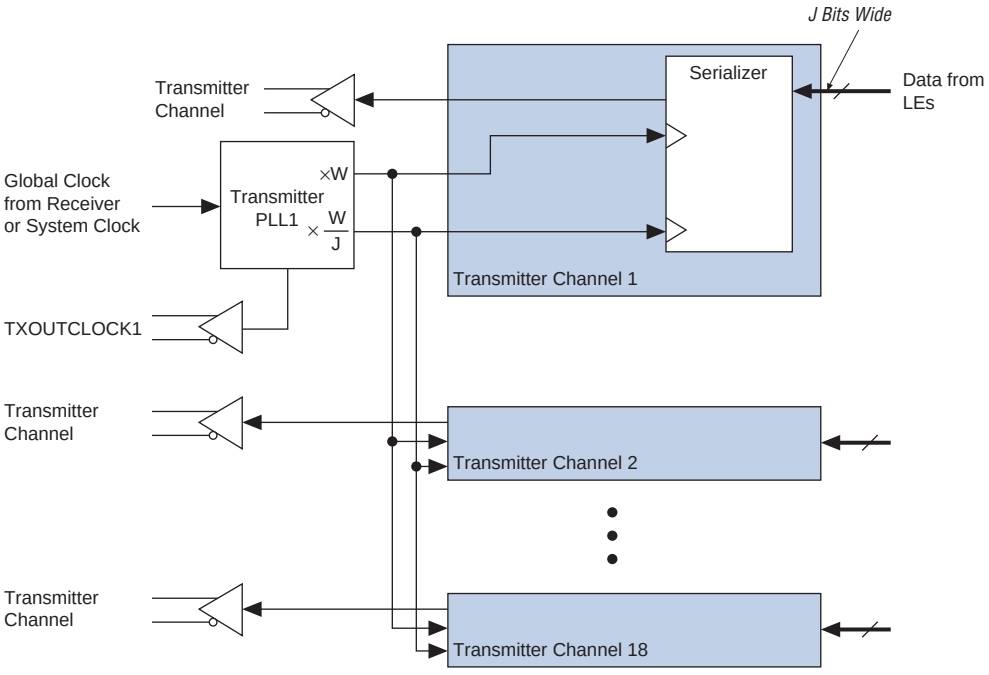
The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Figure 33. True-LVDS Transmitter Diagram *Notes (1), (2)*



Notes to Figure 33:

(1) Two sets of 18 transmitter channels are located in each APEX II device. Each set of 18 channels has one transmitter PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

Clock-Data Synchronization

In addition to dedicated serial-to-parallel converters, APEX II True-LVDS circuitry contains CDS circuitry in every receiver channel. The CDS feature can be turned on or off independently for each receiver channel. There are two modes for the CDS circuitry: single-bit mode, which corrects a fixed clock-to-data skew of up to ±50% of the data bit period, and multi-bit mode, which corrects any fixed clock-to-data skew.

Table 17. APEX II JTAG Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP2A15	1,524
EP2A25	1,884
EP2A40	2,328
EP2A70	3,228

Table 18. 32-Bit APEX II Device IDCODE				
Device	**IDCODE (32 Bits)** *(1)*			
	Version (4 Bits)	**Part Number (16 Bits)**	**Manufacturer Identity (11 Bits)**	**1 (1 Bit)** *(2)*
EP2A15	0000	1100 0100 0000 0000	000 0110 1110	1
EP2A25	0000	1100 0110 0000 0000	000 0110 1110	1
EP2A40	0000	1101 0000 0000 0000	000 0110 1110	1
EP2A70	0000	1110 0000 0000 0000	000 0110 1110	1

Notes to Tables 17 and 18:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

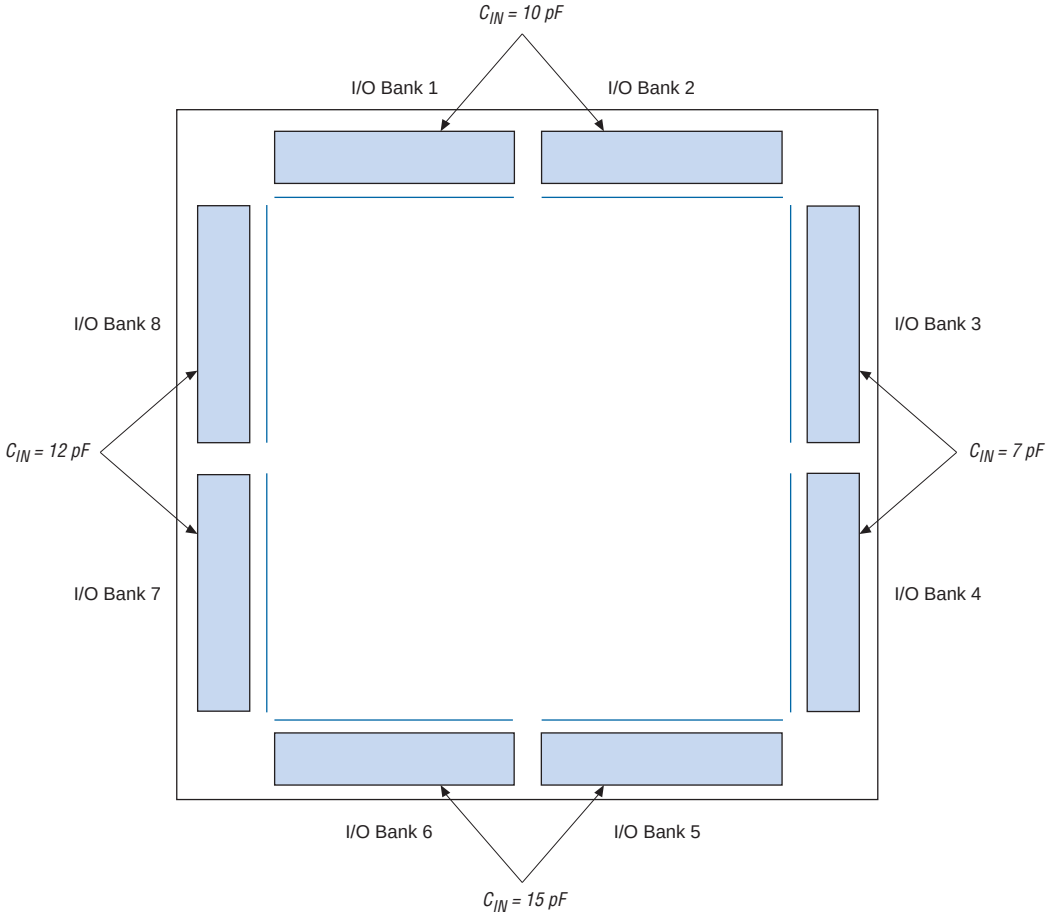
Figure 36 shows the timing requirements for the JTAG signals.

Table 46. APEX II Device Capacitance

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF

Note to Table 46:
(1) See Figure 40.

Figure 40. APEX II Maximum Input & Output Pin Capacitance



Timing Model

The high-performance FastTrack and MegaLAB interconnect routing structures ensure predictable performance, and accurate simulation and timing analysis. In contrast, the unpredictable performance of FPGAs is caused by their segmented connection scheme.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum drive strength.

Figure 41 shows the f_{MAX} timing model for APEX II devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. However, the Quartus II software timing analysis provides more accurate timing information because the Quartus II software usually has more up-to-date timing information than the data sheet until the timing model is final. Also, the Quartus II software can model delays caused by loading and distance effects more accurately than by using the numbers in this data sheet.

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 54. EP2A15 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.64		0.73		0.84		ns
t_{F20+}	1.18		1.35		1.56		ns

Table 55. EP2A15 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.15		1.32		ns
t_{CL}	1.00		1.15		1.32		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.15		1.32		ns
t_{ESBCL}	1.00		1.15		1.32		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 56. EP2A25 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 69. EP2A15 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.16		2.34		2.53		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.36	2.00	4.75	2.00	5.18	ns
t_{XZ}		5.57		6.24		6.97	ns
t_{ZX}		5.57		6.24		6.97	ns
$t_{INSUPLL}$	1.24		1.37		1.52		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.90	0.50	3.16	0.50	3.45	ns
t_{XZPLL}		4.12		4.65		5.23	ns
t_{ZXPLL}		4.12		4.65		5.23	ns

Table 70. EP2A25 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.92		2.08		2.26		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.29	2.00	4.62	2.00	4.98	ns
t_{XZ}		5.24		5.73		6.26	ns
t_{ZX}		5.24		5.73		6.26	ns
$t_{INSUPLL}$	1.17		1.27		1.40		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.61	0.50	2.83	0.50	3.07	ns
t_{XZPLL}		3.55		3.93		4.35	ns
t_{ZXPLL}		3.55		3.93		4.35	ns

Table 75. EP2A70 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.79		2.99		3.22		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.91	2.00	5.24	2.00	5.60	ns
t_{XZ}		6.16		6.71		7.32	ns
t_{ZX}		6.16		6.71		7.32	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.86	0.50	3.08	ns
t_{XZPLL}		3.92		4.34		4.79	ns
t_{ZXPLL}		3.92		4.34		4.79	ns