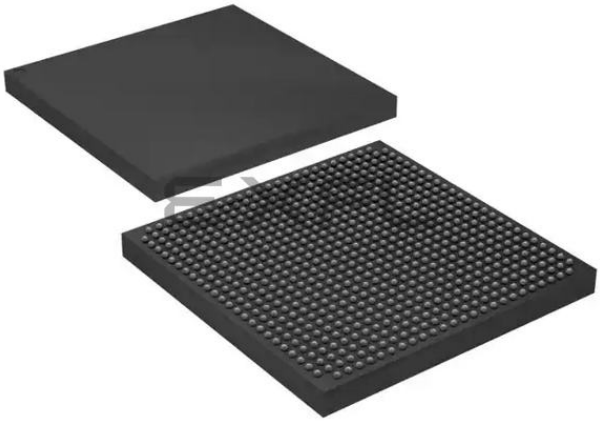

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3840
Number of Logic Elements/Cells	38400
Total RAM Bits	655360
Number of I/O	492
Number of Gates	3000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2a40f672c9

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. APEX II Package Sizes

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Pitch (mm)	1.00	1.27	1.00	1.00
Area (mm^2)	729	1,225	1,089	1,600
Length × Width (mm × mm)	27 × 27	35 × 35	33 × 33	40 × 40

Table 3. APEX II Package Options & I/O Pin Count *Notes (1), (2)*

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2A15	492	492		
EP2A25	492	536		
EP2A40	492	536	735	
EP2A70		536		1,060

Notes to Table 3:

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

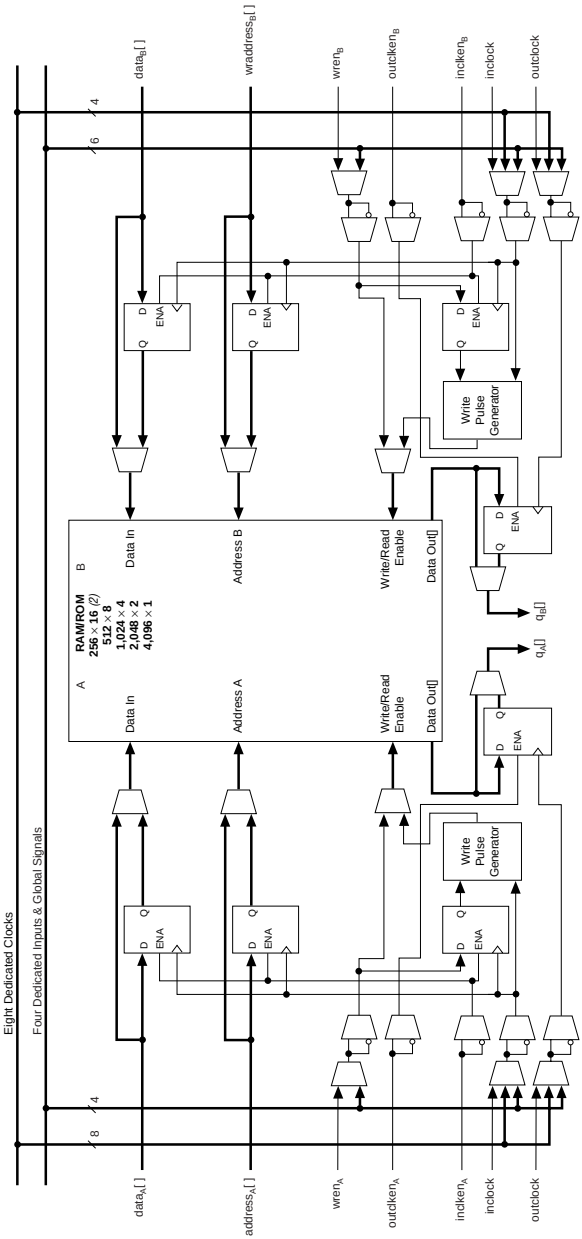
Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 19. ESB in Input/Output Clock Mode *Note (1)*

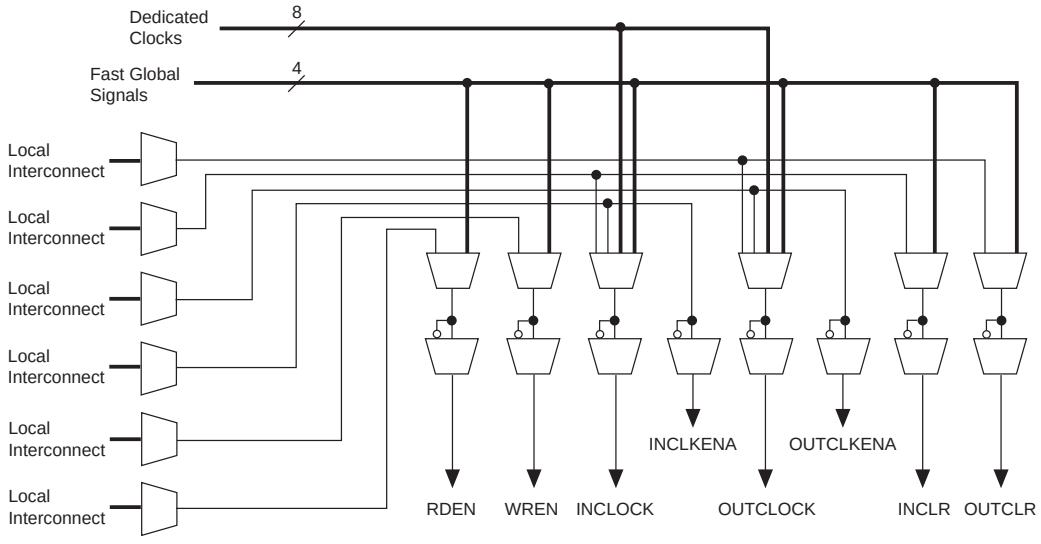


Notes to Figure 19:

(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.

(2) This configuration is not supported for bidirectional dual-port configuration.

Figure 24. ESB Control Signal Generation

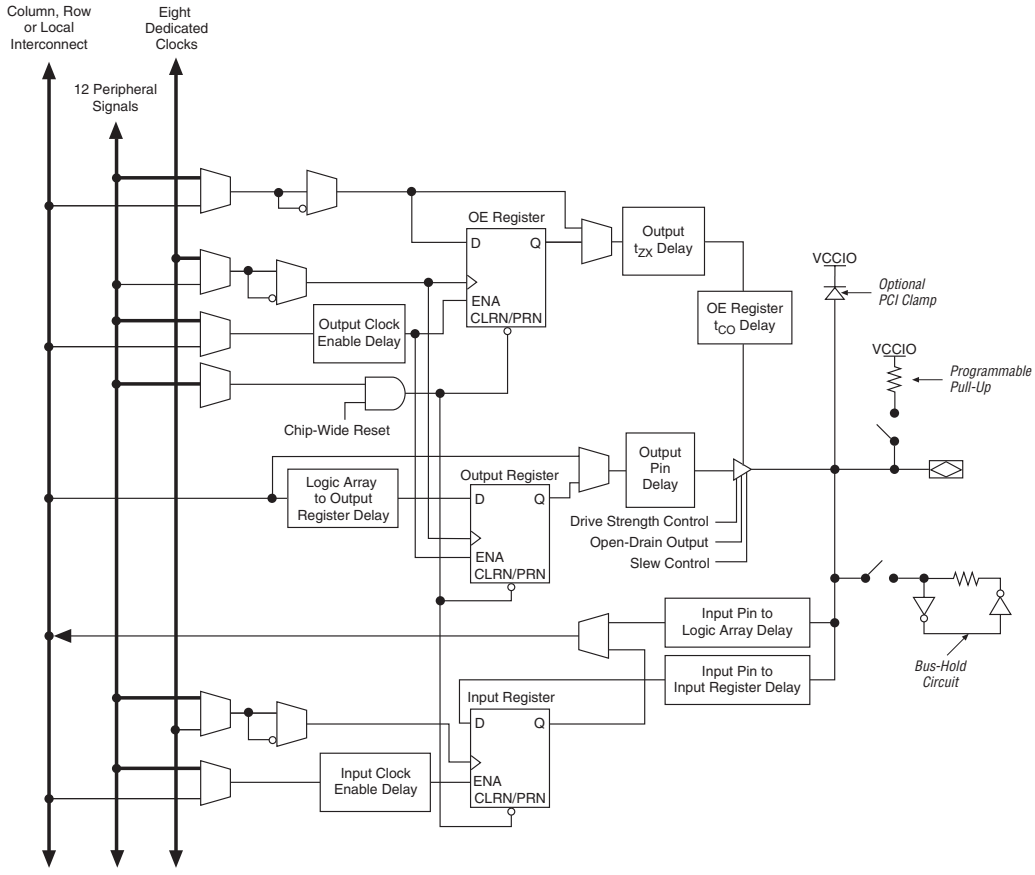


An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

Figure 28. APEX II IOE in Bidirectional I/O Configuration



The APEX II IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

Table 8. APEX II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay *(1)*	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output propagation delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register

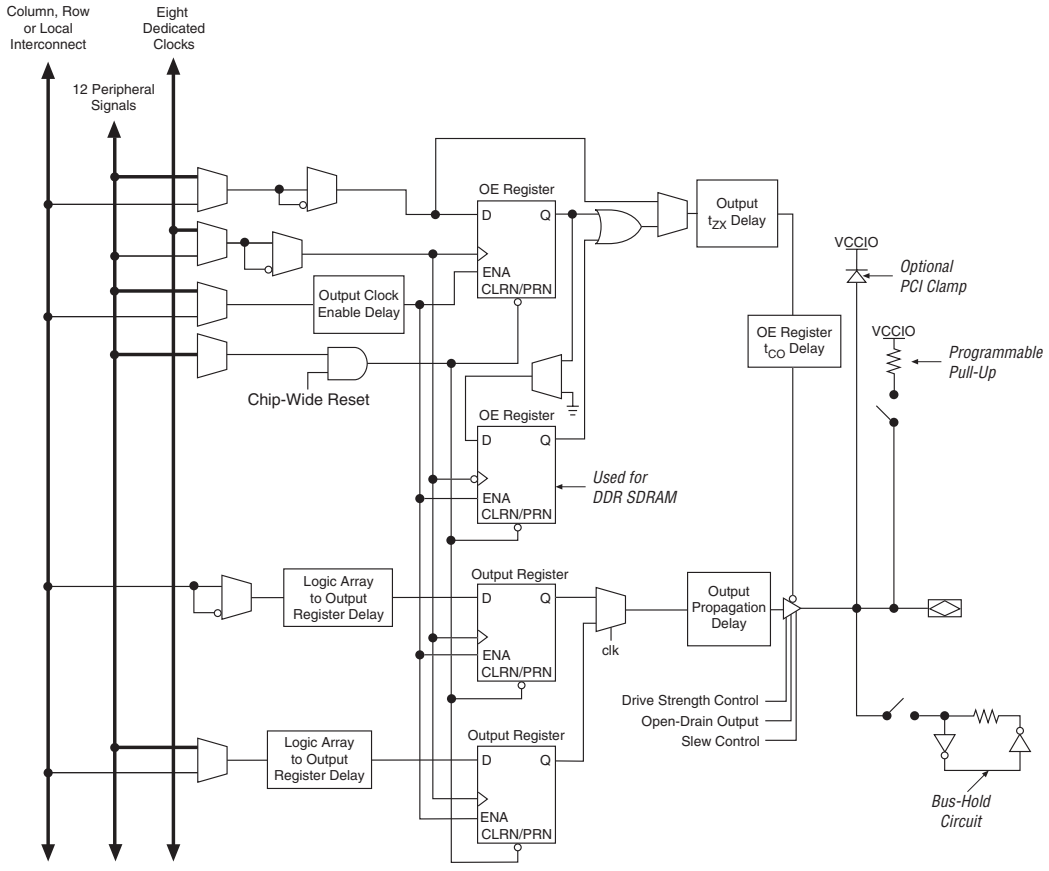
Note to Table 8:
(1) This delay has four settings: off and three levels of delay.

The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

Figure 30. APEX II IOE in DDR Output I/O Configuration



The APEX II IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations.

APEX II I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM at 167 MHz (334 Mbps). The negative-edge-clocked OE register is used to hold the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements. QDR SRAMs are also supported with DDR I/O pins on separate read and write ports.

Zero Bus Turnaround SRAM Interface Support

In addition to DDR SDRAM support, APEX II device I/O pins also support interfacing with ZBT SRAM devices at up to 200 MHz. ZBT SRAM blocks are designed to eliminate dead bus cycles when turning a bidirectional bus around between reads and writes, or writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle.

To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) delay ensures that the t_{ZX} is greater than the clock-to-high-impedance time (t_{XZ}). Phase delay control of clocks to the OE/output and input registers using two general-purpose PLLs enable the APEX II device to meet ZBT t_{CO} and t_{SU} times.

Programmable Drive Strength

The output buffer for each APEX II device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, 3.3-V GTL+, PCI, and PCI-X support a minimum setting. The minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot. Table 9 shows the possible settings for the I/O standards with drive strength control.

The APEX II VCCINT pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.5-V, 1.8-V, 2.5-V or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (i.e., when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 14 summarizes APEX II MultiVolt I/O support.

Table 14. APEX II MultiVolt I/O Support *Note (1)*

V_{CCIO} (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓		✓				
1.8	✓ (2)	✓	✓	✓		✓ (3)	✓			
2.5	✓ (2)	✓ (2)	✓	✓		✓ (4)	✓ (4)	✓		
3.3	✓ (2)	✓ (2)	✓	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓

Notes to Table 14:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}, except for with a 5.0-V input.
(2) These input levels are only allowed if the input standard is set to any V_{REF} standard (i.e., SSTL-3, SSTL-2, HSTL, GTL+, and AGP 2×). The V_{REF} standard inputs are powered by V_{CCINT}. LVTTL, PCI, PCI-X, and AGP 1× standard inputs are powered by V_{CCIO}. As a result, input levels below the V_{CCIO} setting cannot drive these standards.
(3) When V_{CCIO} = 1.8 V, an APEX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
(4) When V_{CCIO} = 2.5 V, an APEX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
(5) APEX II devices can be 5.0-V tolerant with the use of an external series resistor and enabling the PCI clamping diode.
(6) When V_{CCIO} = 3.3 V, an APEX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins with a pull-up resistor to the 5.0-V supply and a series register to the I/O pin can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot Socketing

Because APEX II devices can be used in a mixed-voltage environment, they have been designed specifically for any possible power-up sequence. Therefore, the V_{CCIO} and V_{CCINT} power supplies may be powered in any order.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 25. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA		0.7	V

Table 26. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 27. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 28. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 29. PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
L_{PIN}	Pin inductance				15	nH

Table 30. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(10)*			0.65	V

Figures 38 and 39 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 38. Receiver Input Waveforms for Differential I/O Standards

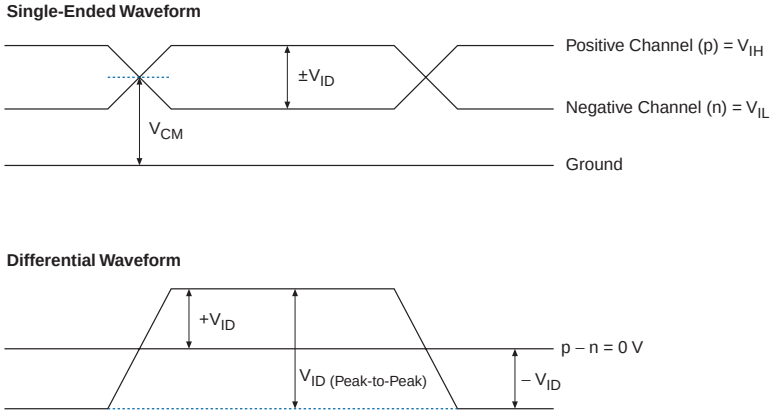
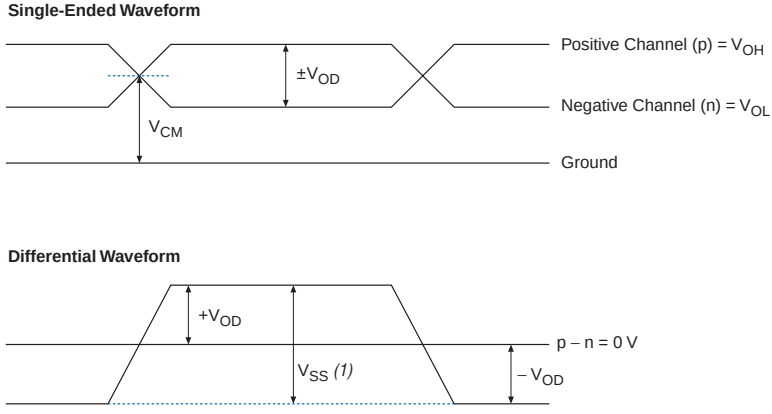


Figure 39. Transmitter Output Waveforms for Differential I/O Standards

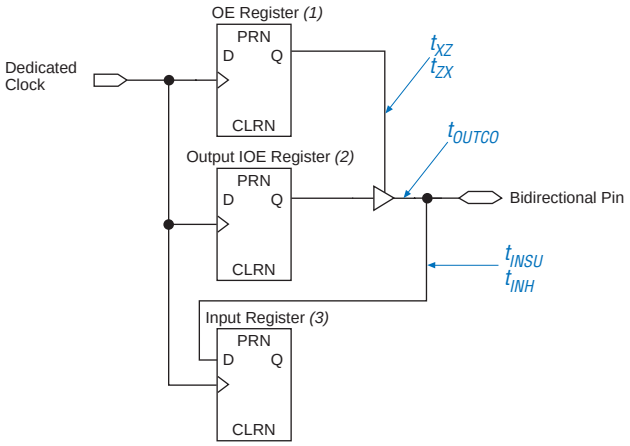


Note to Figure 39:
(1) V_{SS}: steady-state differential output voltage.

Tables 42 through 45 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Figure 42 shows the timing model for bi-directional, input, and output IOE timing.

Figure 42. Synchronous External TIming Model



Notes to Figure 42:

(1) The output enable register is in the IOE and is controlled by the "Fast Output Enable Register = ON" option in the Quartus II software.

(2) The output register is in the IOE and is controlled by the "Fast Output Register = ON" option in the Quartus II software.

(3) The input register is in the IOE and is controlled by the "Fast Input Register = ON" option in the Quartus II software.

Tables 47 through 50 show APEX II LE, ESB, and routing delays and minimum pulse-width timing parameters for the f_{MAX} timing model.

Table 47. APEX II f_{MAX} LE Timing Parameters

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time before clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LUT delay for data-in to data-out

Table 50. APEX II Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Table 51. APEX II External Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
t_{XZ}	Clock-to-output buffer disable delay	
t_{ZX}	Clock-to-output buffer enable delay	Slow slew rate = OFF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF
t_{XZPLL}	PLL clock-to-output buffer disable delay	
t_{ZXPLL}	PLL clock-to-output buffer enable delay	Slow slew rate = OFF

Note to Table 51:

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

Table 57. EP2A25 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	0.07		0.07		0.09		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 58. EP2A25 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.65		0.75		0.86		ns
t_{F20+}	1.11		1.27		1.46		ns

Table 59. EP2A25 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.50		2.12		ns
t_{CL}	1.00		1.50		2.12		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.50		2.12		ns
t_{ESBCL}	1.00		1.50		2.12		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 60. EP2A40 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.22		0.26		0.29		ns
t_{H}	0.22		0.26		0.29		ns
t_{CO}		0.16		0.18		0.21	ns
t_{LUT}		0.48		0.55		0.63	ns

Table 75. EP2A70 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.79		2.99		3.22		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.91	2.00	5.24	2.00	5.60	ns
t_{XZ}		6.16		6.71		7.32	ns
t_{ZX}		6.16		6.71		7.32	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.67	0.50	2.86	0.50	3.08	ns
t_{XZPLL}		3.92		4.34		4.79	ns
t_{ZXPLL}		3.92		4.34		4.79	ns

Table 77. APEX II Selectable I/O Standards Output Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		3.32		3.82		4.20	ns
1.8 V		2.65		3.05		3.36	ns
2.5 V		1.20		1.38		1.52	ns
3.3-V PCI		– 0.68		– 0.78		– 0.85	ns
3.3-V PCI-X		– 0.68		– 0.78		– 0.85	ns
GTL+		– 0.45		– 0.52		– 0.57	ns
SSTL-3 Class I		– 0.52		– 0.60		– 0.66	ns
SSTL-3 Class II		– 0.52		– 0.60		– 0.66	ns
SSTL-2 Class I		– 0.68		– 0.78		– 0.86	ns
SSTL-2 Class II		– 0.81		– 0.93		– 1.02	ns
HSTL Class I		– 0.08		– 0.09		– 0.10	ns
HSTL Class II		– 0.23		– 0.27		– 0.30	ns
LVDS		– 1.41		– 1.62		– 1.79	ns
LVPECL		– 1.38		– 1.58		– 1.74	ns
PCML		– 1.30		– 1.50		– 1.65	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 1.22		– 1.41		– 1.55	ns
Differential HSTL		– 1.41		– 1.62		– 1.79	ns

Power Consumption

Detailed power consumption information for APEX II devices will be released via a future interactive power estimator on the Altera web site.

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the ***Altera Digital Library*** for pin-out information.

Revision History

The information contained in the *APEX II Programmable Logic Device Family Data Sheet* version 3.0 supersedes information published in previous versions. The following changes were made to the *APEX II Programmable Logic Device Family Data Sheet* version 3.0:

- Changed the value from 624 to 400 Mbps throughout the document.
- Deleted the pin count (612) for the EP2A25 device in the 1,020-pin FineLine BGA package (see Table 3).
- Added Table 13.
- Changed the maximum value of 3.6 to 2.4 in Table 20.
- Updated Tables 60 through 67 and Tables 72 through 75.
- Updated Figures 25, 28, and 30.
- Added *Note (1)* to Figure 13.
- Added Figure 43.

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