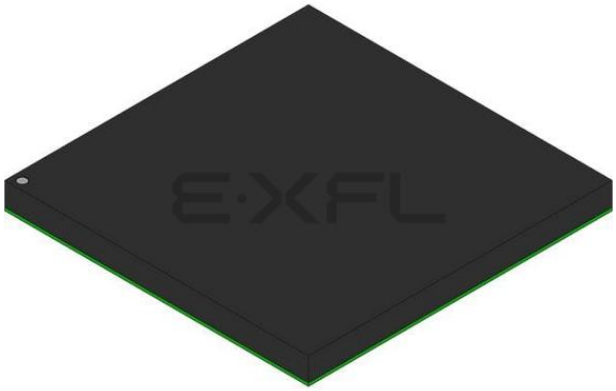

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6720
Number of Logic Elements/Cells	67200
Total RAM Bits	1146880
Number of I/O	540
Number of Gates	5250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	724-BBGA, FCBGA
Supplier Device Package	724-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a70b724c8

Each I/O pin is fed by an IOE located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and six registers that can be used for registering input, output, and output-enable signals. When used with a dedicated clock pin, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM and ZBT and QDR SRAM devices.

IOEs provide a variety of features such as: 3.3-V, 64-bit, 66-MHz PCI compliance, 3.3-V, 64-bit, 133-MHz PCI-X compliance, Joint Test Action Group (JTAG) boundary-scan test (BST) support, output drive strength control, slew-rate control, tri-state buffers, bus-hold circuitry, programmable pull-up resistors, programmable input and output delays, and open-drain outputs.

APEX II devices offer enhanced I/O support, including support for 1.5 V, 1.8 V, 2.5 V, 3.3 V, LVCMOS, LVTTL, HSTL, LVDS, LVPECL, HyperTransport, PCML, 3.3-V PCI, PCI-X, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. High-speed (up to 1.0 Gbps) differential transfers are supported with True-LVDS circuitry for LVDS, LVPECL, HyperTransport, and PCML I/O standards. The optional CDS feature corrects any clock-to-data skew at the True-LVDS receiver channels, allowing for flexible board topologies. Up to 88 Flexible-LVDS channels support differential transfer at up to 400 Mbps (DDR) for LVDS and HyperTransport I/O standards.

An ESB can implement many types of memory, including Dual-Port+ RAM, CAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. The abundance of cascadable ESBs ensures that the APEX II device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX II device.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 6. APEX II Carry Chain

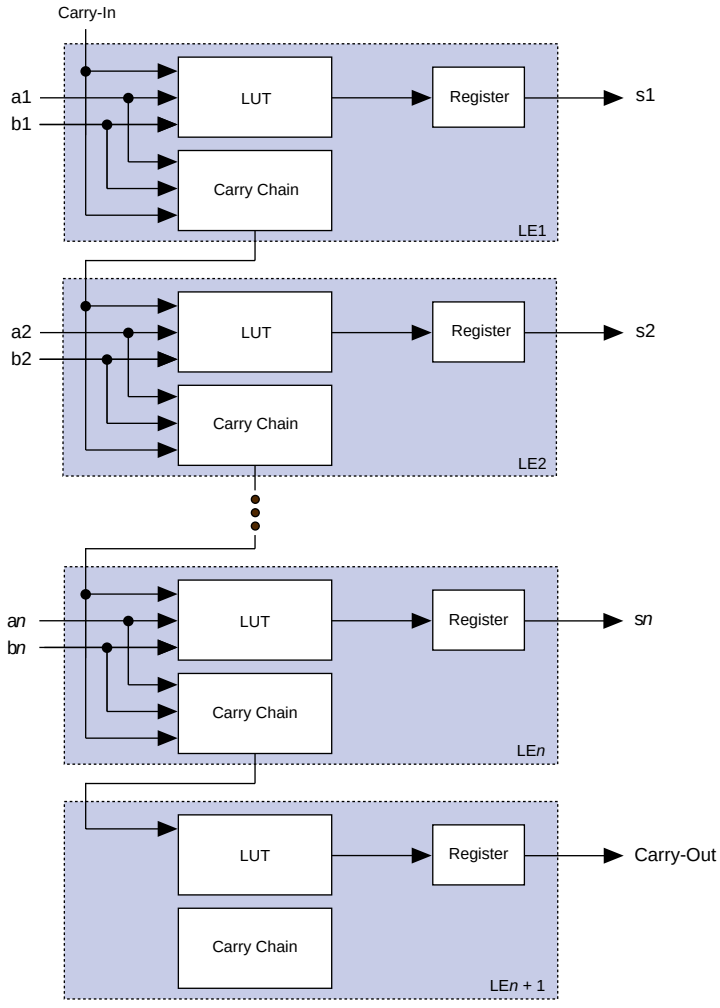
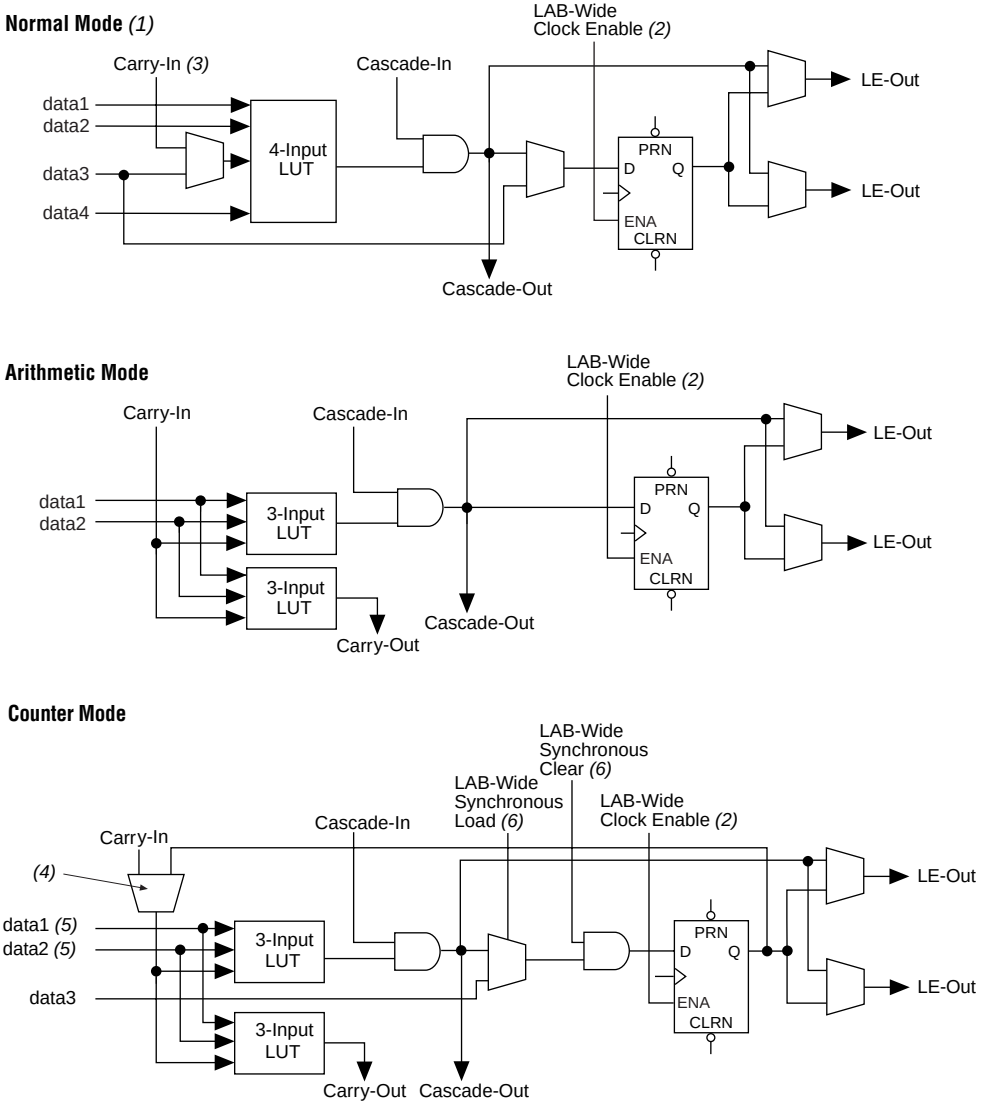


Figure 8. APEX II LE Operating Modes



Notes to Figure 8:

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in a LAB.
(6) The LAB-wide synchronous clear and LAB-wide synchronous load affect all registers in a LAB.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

Clear & Preset Logic Control

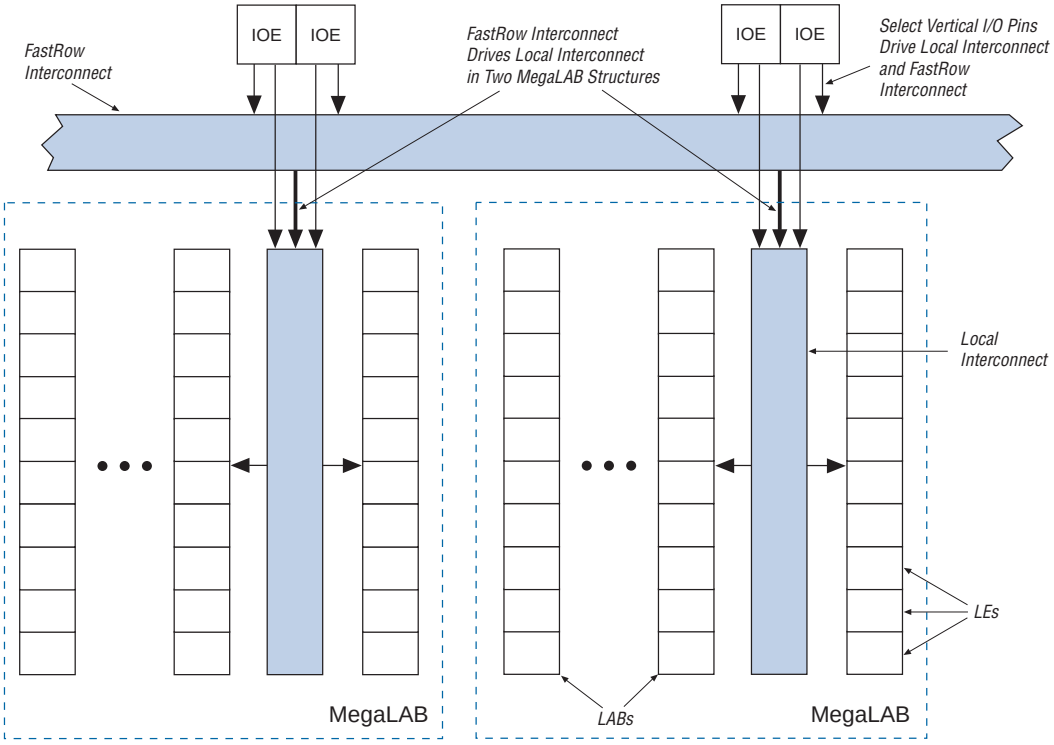
Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

In addition to the two clear and preset modes, APEX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

FastTrack Interconnect

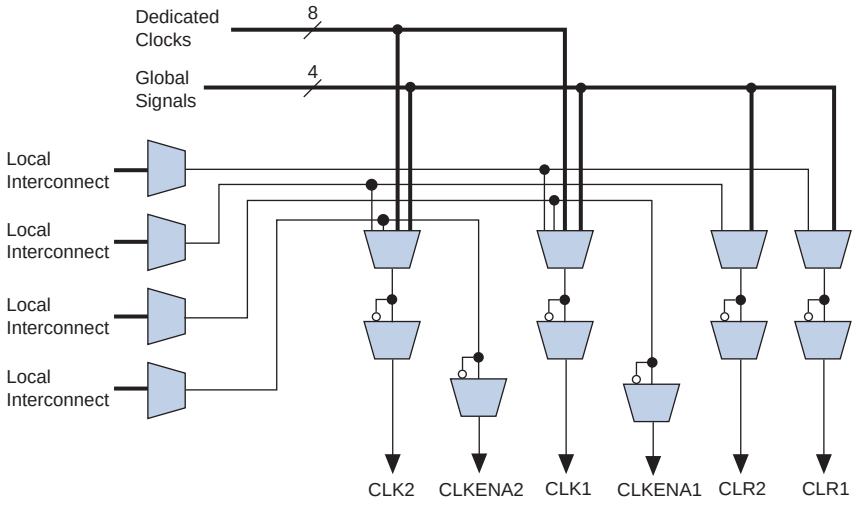
In the APEX II architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack interconnect. The FastTrack interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

Figure 12. APEX II FastRow Interconnect



The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

Figure 15. ESB Product-Term Mode Control Logic

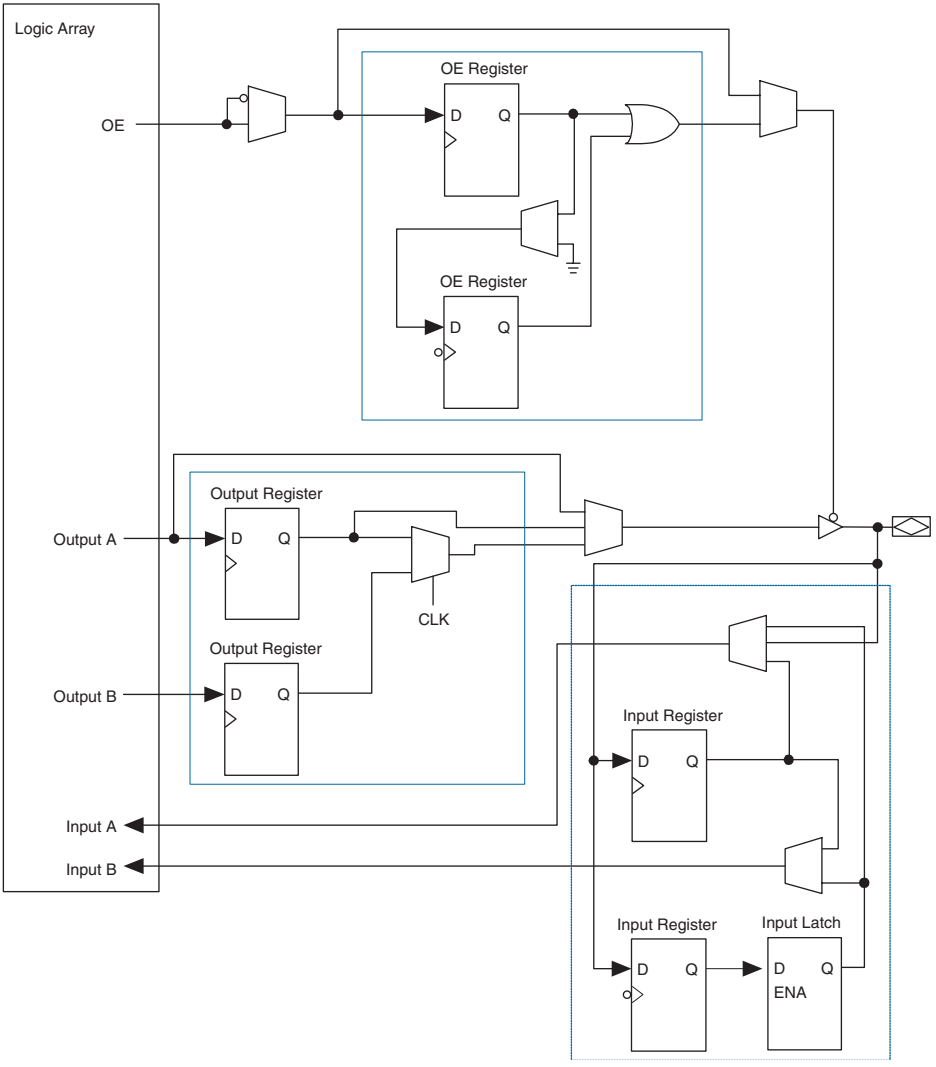


Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

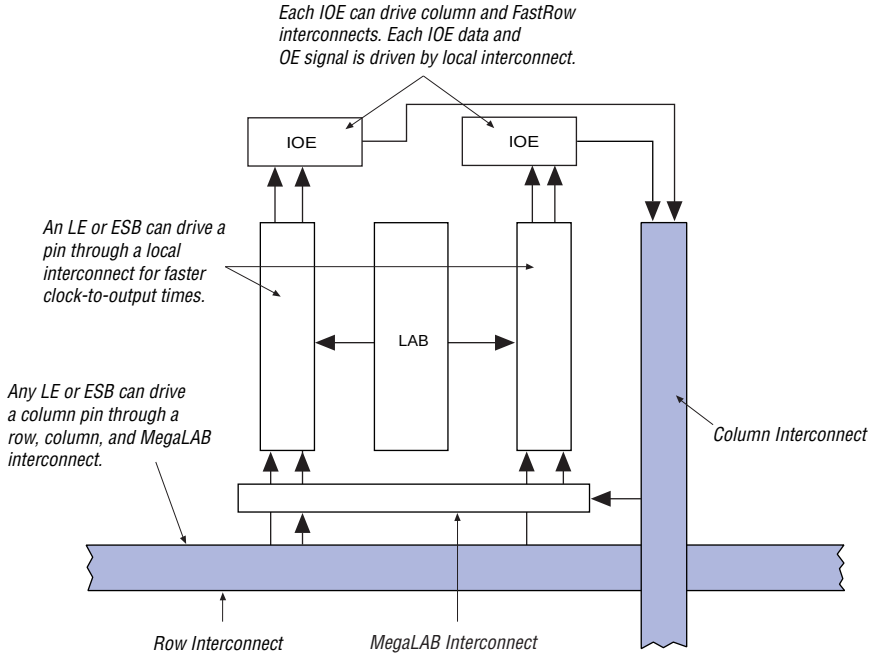
The Quartus II Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX II parallel expanders.

Figure 25. APEX II IOE Structure



The IOEs are located around the periphery of the APEX II device. Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the FastTrack or column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

Figure 27. Column IOE Connection to the Interconnect



FastRow interconnects connect a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing.

APEX II devices have a peripheral control bus made up of 12 signals that drive the IOE control signals. The peripheral bus is composed of six output enables, `OE[5:0]` and six clock enables, `CE[5:0]`. These twelve signals can be driven from internal logic or from the Fast I/O signals. Table 7 lists the peripheral control signal destinations.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

Table 8. APEX II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay *(1)*	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output propagation delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register

Note to Table 8:
(1) This delay has four settings: off and three levels of delay.

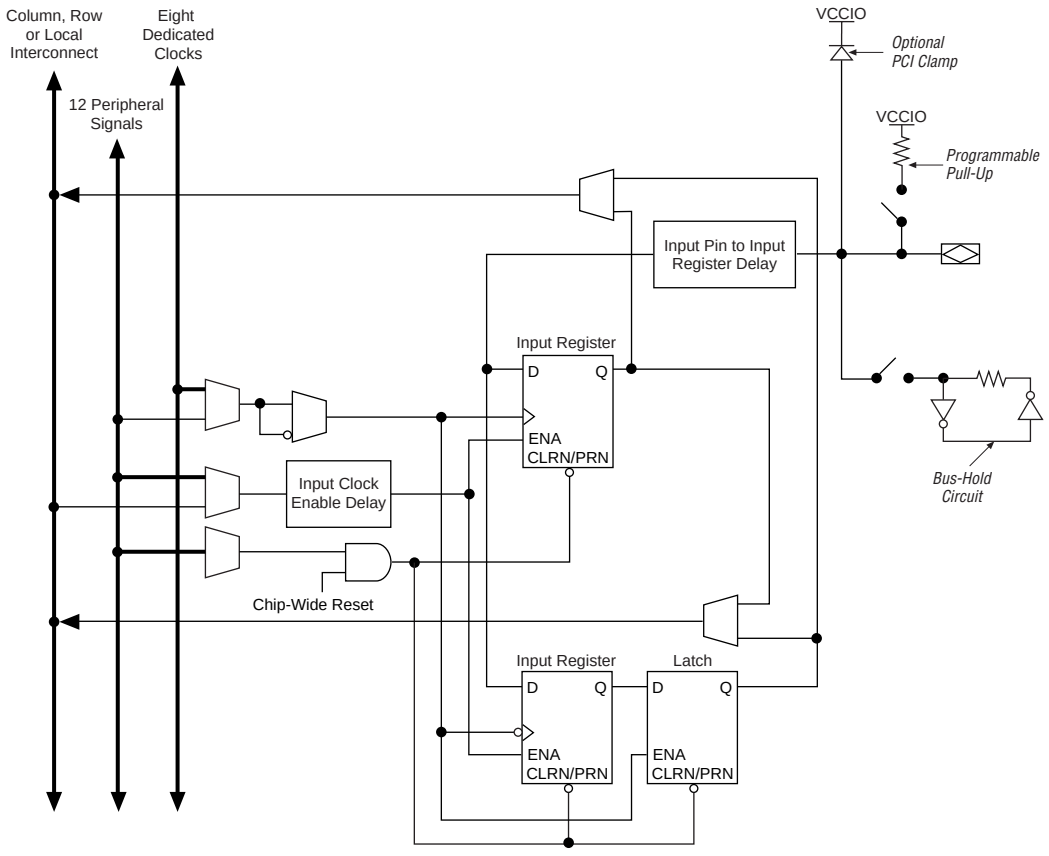
The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers are used to clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous to the same clock edge (either rising or falling). Figure 29 shows an IOE configured for DDR input.

Figure 29. APEX II IOE in DDR Input I/O Configuration



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These register outputs are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 30 shows the IOE configured for DDR output.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

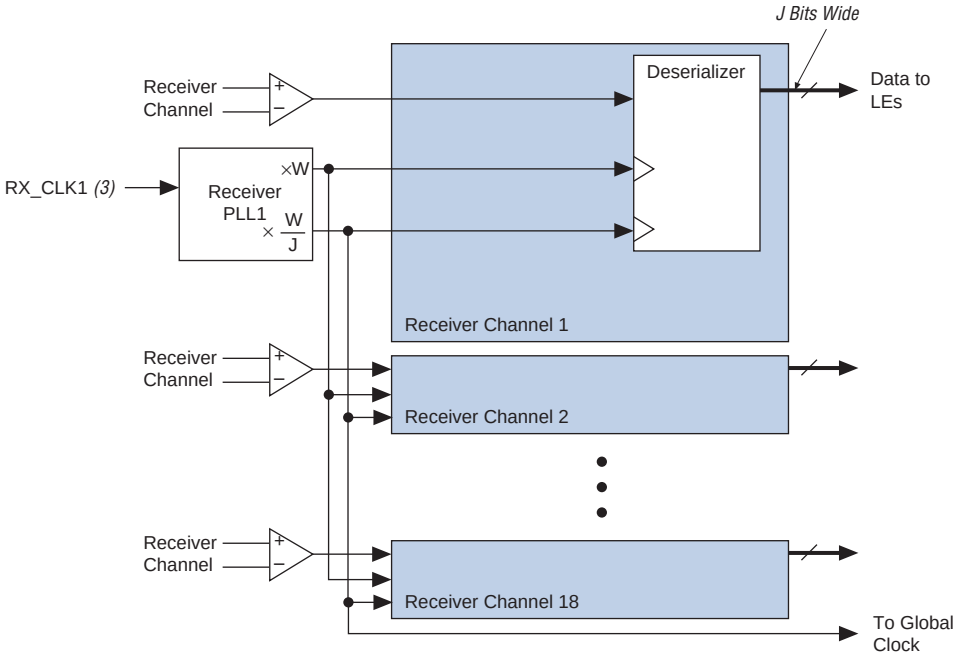
The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Figure 32. True-LVDS Receiver Diagram *Notes (1), (2)*



Notes to Figure 32:

(1) Two sets of 18 receiver channels are located in each APEX II device. Each set of 18 channels has one receiver PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

(3) These clock pins drive receiver PLLs only. They do not drive directly to the logic array. However, the receiver PLL can drive the logic array via a global clock line.

Note to Figure 35:

(1) *n* represents the prescale divider for the PLL input. *m* represents the multiplier. *k* and *v* represent the different post scale dividers for the two possible PLL outputs. *m* and *k* are integers that range from 1 to 160. *n* and *v* are integers that range from 1 to 16.

Advanced ClockBoost Multiplication & Division

APEX II PLLs include circuitry that provides clock synthesis for eight internal outputs and two external outputs using $m / (n \times$ output divider) scaling. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. The closed loop equation for Figure 35 gives an output frequency $f_{clock0} = (m / (n \times k))f_{IN}$ and $f_{clock1} = (m / (n \times v))f_{IN}$. These equations allow the multiplication or division of clocks by a programmable number. The Quartus II software automatically chooses the appropriate scaling factors according to the frequency, multiplication, and division values entered.

A single PLL in an APEX II device allows for multiple user-defined multiplication and division ratios that are not possible even with multiple delay-locked loops (DLLs). For example, if a frequency scaling factor of 3.75 is needed for a given input clock, a multiplication factor of 15 and a division factor of 4 can be entered. This advanced multiplication scaling can be performed with a single PLL, making it unnecessary to cascade PLL outputs.

External Clock Outputs

APEX II devices have two low-jitter external clocks available for external clock sources. Other devices on the board can use these outputs as clock sources.

There are three modes for external clock outputs.

- Zero Delay Buffer: The external clock output pin is phase aligned with the clock input pin for zero delay. Multiplication, programmable phase shift, and time delay shift are not allowed in this configuration. The MegaWizard interface for `altclklock` should be used to verify possible clock settings.
- External Feedback: The external feedback input pin is phase aligned with clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. This mode has the same restrictions as zero delay buffer mode.
- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

Table 28. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.3 × V_{CCIO}	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V

Table 29. PCI-X Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.35 × V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 × V_{CCIO}			V
I_{IL}	Input leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 × V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 × V_{CCIO}	V
L_{PIN}	Pin inductance				15	nH

Table 30. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		V_{REF} + 0.1			V
V_{IL}	Low-level input voltage				V_{REF} – 0.1	V
V_{OL}	Low-level output voltage	I_{OL} = 36 mA *(10)*			0.65	V

Table 31. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(10)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(10)*			V_{TT} – 0.57	V

Table 32. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(10)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(10)*			V_{TT} – 0.76	V

Table 33. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(10)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(10)*			V_{TT} – 0.6	V

Figures 38 and 39 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 38. Receiver Input Waveforms for Differential I/O Standards

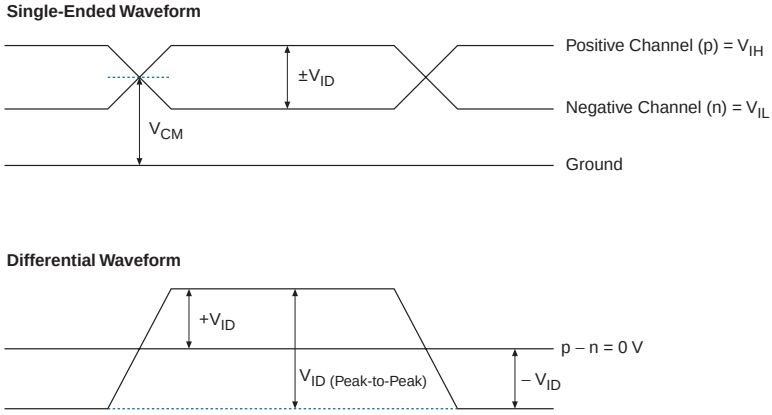
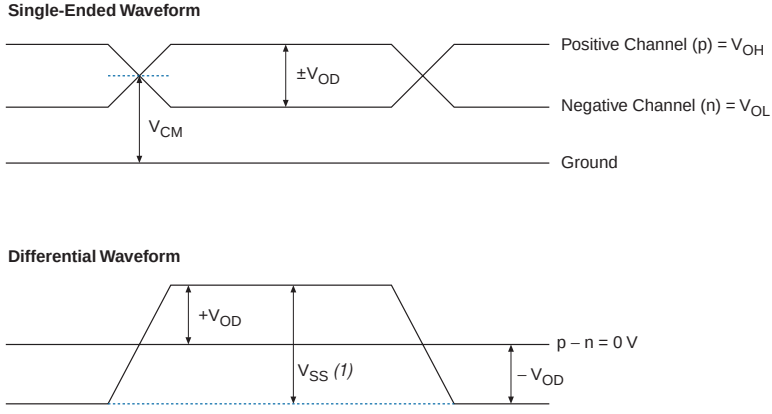


Figure 39. Transmitter Output Waveforms for Differential I/O Standards



Note to Figure 39:
(1) V_{SS}: steady-state differential output voltage.

Tables 42 through 45 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 50. APEX II Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Table 51. APEX II External Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
t_{XZ}	Clock-to-output buffer disable delay	
t_{ZX}	Clock-to-output buffer enable delay	Slow slew rate = OFF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF
t_{XZPLL}	PLL clock-to-output buffer disable delay	
t_{ZXPLL}	PLL clock-to-output buffer enable delay	Slow slew rate = OFF

Note to Table 51:

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

Table 57. EP2A25 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	0.07		0.07		0.09		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 58. EP2A25 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.65		0.75		0.86		ns
t_{F20+}	1.11		1.27		1.46		ns

Table 73. EP2A40 External Timing Parameters for Column I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.00		2.16		2.33		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.96	2.00	5.29	2.00	5.64	ns
t_{XZ}		7.04		7.59		8.19	ns
t_{ZX}		7.04		7.59		8.19	ns
$t_{INSUPLL}$	1.20		1.31		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.66	0.50	2.87	0.50	3.09	ns
t_{XZPLL}		4.74		5.17		5.64	ns
t_{ZXPLL}		4.74		5.17		5.64	ns

Table 74. EP2A70 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.48		2.68		2.90		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.76	2.00	5.12	2.00	5.51	ns
t_{XZ}		5.68		6.19		6.76	ns
t_{ZX}		5.68		6.19		6.76	ns
$t_{INSUPLL}$	1.19		1.30		1.43		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.52	0.50	2.74	0.50	2.98	ns
t_{XZPLL}		3.44		3.82		4.23	ns
t_{ZXPLL}		3.44		3.82		4.23	ns