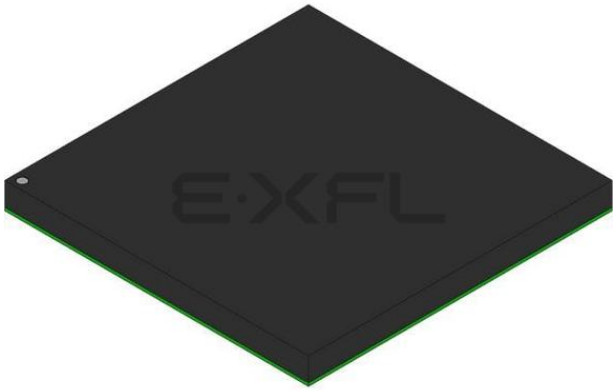

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6720
Number of Logic Elements/Cells	67200
Total RAM Bits	1146880
Number of I/O	540
Number of Gates	5250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	724-BBGA, FCBGA
Supplier Device Package	724-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a70b724c9

- LogicLock™ incremental design for intellectual property (IP) integration and team-based design
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Support for popular revision-control software packages, including PVCS, RCS, and SCCS

Tables 2 and 3 show the APEX II ball-grid array (BGA) and FineLine BGA™ device package sizes, options, and I/O pin counts.

Table 2. APEX II Package Sizes

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
Pitch (mm)	1.00	1.27	1.00	1.00
Area (mm^2)	729	1,225	1,089	1,600
Length × Width (mm × mm)	27 × 27	35 × 35	33 × 33	40 × 40

Table 3. APEX II Package Options & I/O Pin Count *Notes (1), (2)*

Feature	672-Pin FineLine BGA	724-Pin BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2A15	492	492		
EP2A25	492	536		
EP2A40	492	536	735	
EP2A70		536		1,060

Notes to Table 3:

(1) All APEX II devices support vertical migration within the same package (e.g., the designer can migrate between the EP2A15, EP2A25, and EP2A40 devices in the 672-pin FineLine BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, LVDS pins, and power pins are the same for a given package across device densities. Migration of I/O pins across densities requires the designer to cross reference the available I/O pins using the device pin-outs. This must be done for all planned densities for a given package type to identify which I/O pins are migratable.

(2) I/O pin counts include dedicated clock and fast I/O pins.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output. The APEX II architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

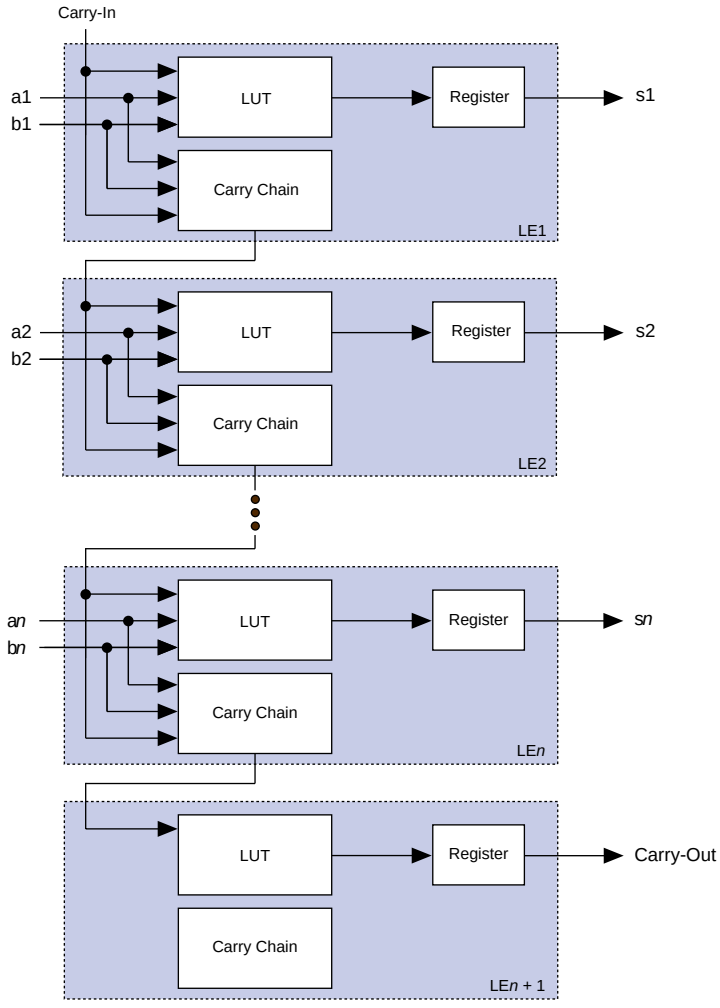
Carry Chain

The carry chain provides a fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX II architecture to implement high-speed counters, adders, and comparators of arbitrary width. The Quartus II Compiler can create carry chain logic automatically during the design process, or the designer can create it manually during design entry. Parameterized functions such as DesignWare functions from Synopsys and library of parameterized modules (LPM) functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack interconnect routing structures.

Figure 6. APEX II Carry Chain



LE Operating Modes

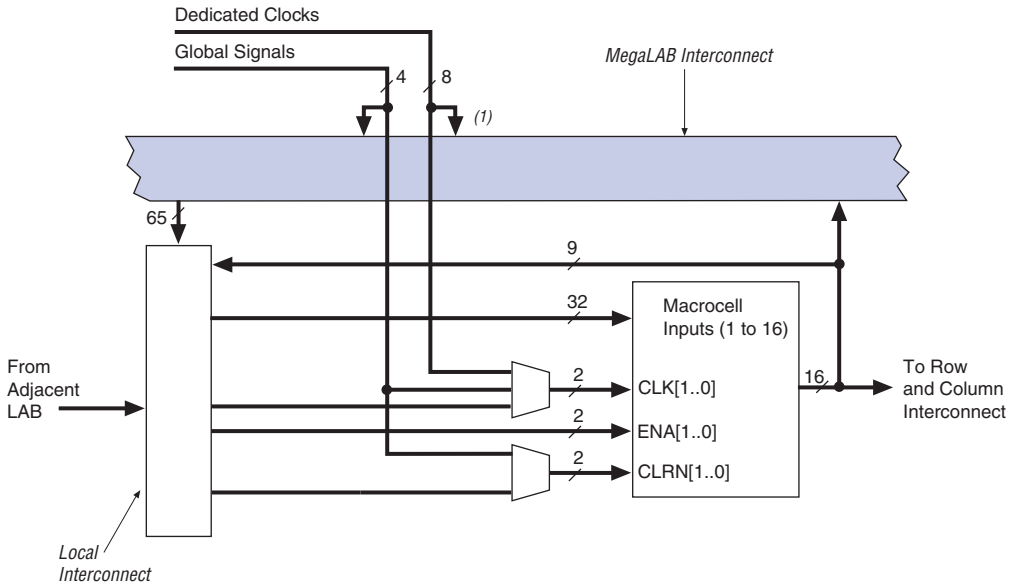
The APEX II LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

Figure 13. Product-Term Logic in ESB



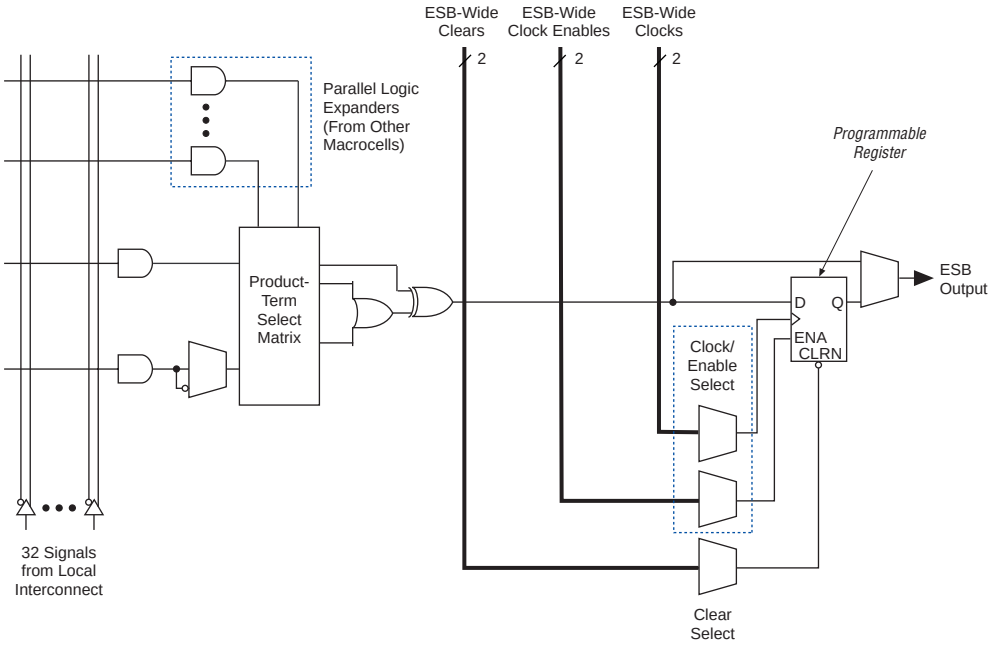
Note ot Figure 13:
(1) PLL outputs cannot drive data input ports.

Macrocells

APEX II macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX II macrocell.

Figure 14. APEX II Macrocell

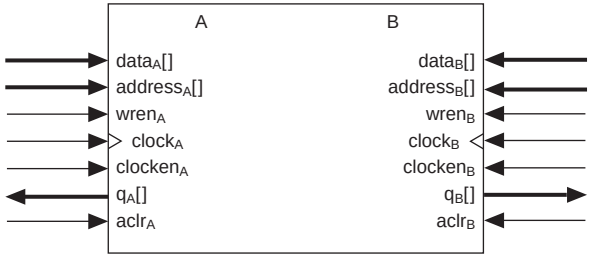


For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

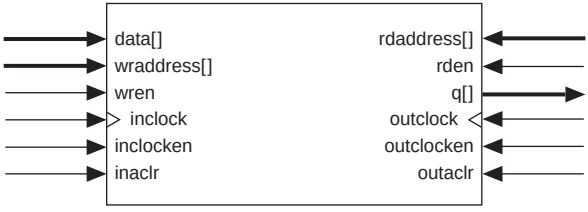
Figure 17. Bidirectional Dual-Port Memory Configuration



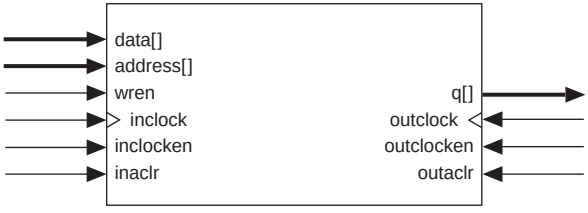
In addition to bidirectional dual-port memory, the ESB also supports dual-port, and single-port RAM. Dual-port memory supports a simultaneous read and write. Single-port memory supports independent read and write. Figure 18 shows these different RAM memory port configurations for an ESB.

Figure 18. Dual- & Single-Port Memory Configurations

Dual-Port Memory



Single-Port Memory *(1)*



Note to Figure 18:

(1) Two single-port memory blocks can be implemented in a single ESB.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

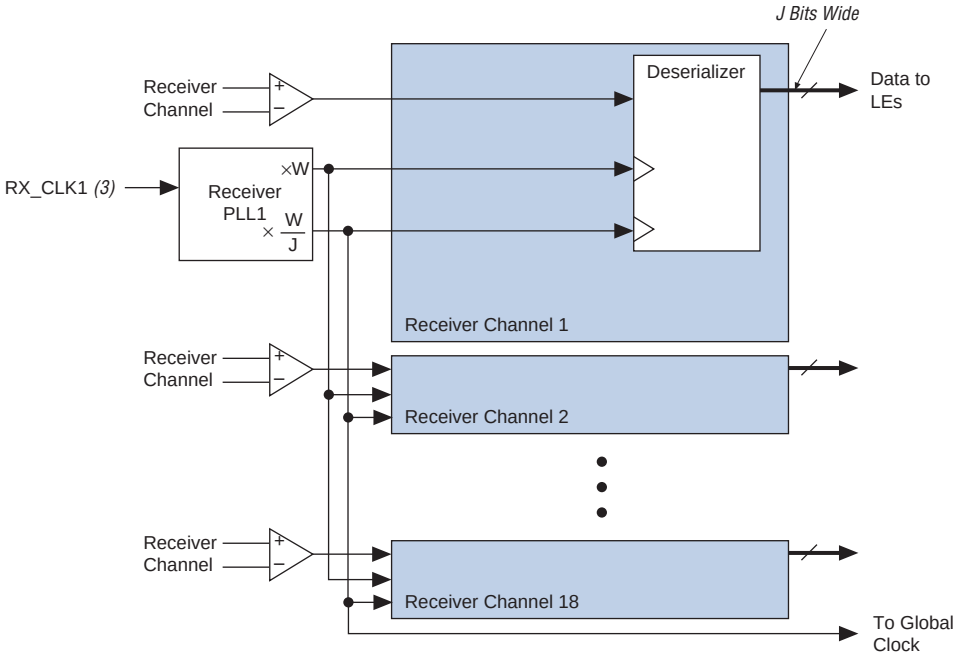
The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Figure 32. True-LVDS Receiver Diagram *Notes (1), (2)*



Notes to Figure 32:

(1) Two sets of 18 receiver channels are located in each APEX II device. Each set of 18 channels has one receiver PLL.

(2) *W* = 1, 2, 4 to 10
J = 1, 2, 4 to 10
W does not have to equal *J*. When *J* = 1 or 2, the deserializer is bypassed. When *J* = 2, DDR I/O registers are used.

(3) These clock pins drive receiver PLLs only. They do not drive directly to the logic array. However, the receiver PLL can drive the logic array via a global clock line.

Single-Bit Mode

Single-bit CDS corrects a fixed clock-to-data skew of up to ±50% of the data bit period, which allows receiver input skew margin (RSKM) to increase by 50% of the data period. To use single-bit CDS, the deserialization factor, *J*, must be equal to the multiplication factor, *W*. The combination of allowable *W* / *J* factors and the associated CDS training patterns automatically determine byte alignment (see Table 11).

Table 11. Single-Bit CDS Training Patterns

W/J Factor	Single-Bit CDS Pattern
10	0000011111
9	000001111
8	00001111
7	0000111
6	000111
5	00011
4	0011

Multi-Bit Mode

Multi-bit CDS corrects any fixed clock-to-data skew. This feature enables flexible board topologies, such as an N:1 topology (see Figure 34), a switch topology, or a matrix topology. Multi-bit CDS corrects for the skews inherent with these topologies, making them possible to use.

Note to Figure 35:

(1) *n* represents the prescale divider for the PLL input. *m* represents the multiplier. *k* and *v* represent the different post scale dividers for the two possible PLL outputs. *m* and *k* are integers that range from 1 to 160. *n* and *v* are integers that range from 1 to 16.

Advanced ClockBoost Multiplication & Division

APEX II PLLs include circuitry that provides clock synthesis for eight internal outputs and two external outputs using $m / (n \times$ output divider) scaling. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. The closed loop equation for Figure 35 gives an output frequency $f_{clock0} = (m / (n \times k))f_{IN}$ and $f_{clock1} = (m / (n \times v))f_{IN}$. These equations allow the multiplication or division of clocks by a programmable number. The Quartus II software automatically chooses the appropriate scaling factors according to the frequency, multiplication, and division values entered.

A single PLL in an APEX II device allows for multiple user-defined multiplication and division ratios that are not possible even with multiple delay-locked loops (DLLs). For example, if a frequency scaling factor of 3.75 is needed for a given input clock, a multiplication factor of 15 and a division factor of 4 can be entered. This advanced multiplication scaling can be performed with a single PLL, making it unnecessary to cascade PLL outputs.

External Clock Outputs

APEX II devices have two low-jitter external clocks available for external clock sources. Other devices on the board can use these outputs as clock sources.

There are three modes for external clock outputs.

- Zero Delay Buffer: The external clock output pin is phase aligned with the clock input pin for zero delay. Multiplication, programmable phase shift, and time delay shift are not allowed in this configuration. The MegaWizard interface for `altclklock` should be used to verify possible clock settings.
- External Feedback: The external feedback input pin is phase aligned with clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. This mode has the same restrictions as zero delay buffer mode.
- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX II devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX II devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX II devices support the JTAG instructions shown in Table 16.

Table 16. APEX II JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring an APEX II device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 16:

(1) Bus hold and weak pull-up features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The APEX II device instruction register length is 10 bits. The APEX II device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for APEX II devices.

For more information, see the following documents:

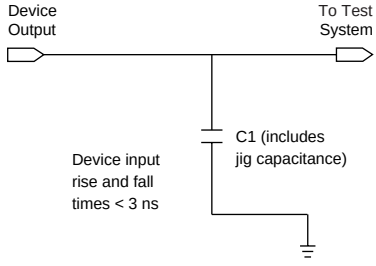
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

Generic Testing

Each APEX II device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX II devices are made under conditions equivalent to those shown in Figure 37. Multiple test patterns can be used to configure devices during all stages of the production flow. AC test criteria include:

- Power supply transients can affect AC measurements.
- Simultaneous transitions of multiple outputs should be avoided for accurate measurement.
- Threshold tests must not be performed under AC conditions.
- Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

Figure 37. APEX II AC Test Conditions



Operating Conditions

APEX II devices are offered in both commercial and industrial grades. However, industrial-grade devices may have limited speed-grade availability.

Tables 20 through 41 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 20. APEX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 21. APEX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 22. APEX II Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 23. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–5	5	µA
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 24. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 31. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		3.0	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –7.6 mA *(10)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 7.6 mA *(10)*			V_{TT} – 0.57	V

Table 32. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		2.3	2.5	2.7	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
V_{IH}	High-level input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.18	V
V_{OH}	High-level output voltage	I_{OH} = –15.2 mA *(10)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 15.2 mA *(10)*			V_{TT} – 0.76	V

Table 33. SSTL-3 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(10)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(10)*			V_{TT} – 0.6	V

Table 46. APEX II Device Capacitance

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF
C_{INCLK}	Input capacitance on dedicated clock pin	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{IN} = 0 V, f = 1.0 MHz		*(1)*	pF

Note to Table 46:
(1) See Figure 40.

Figure 40. APEX II Maximum Input & Output Pin Capacitance

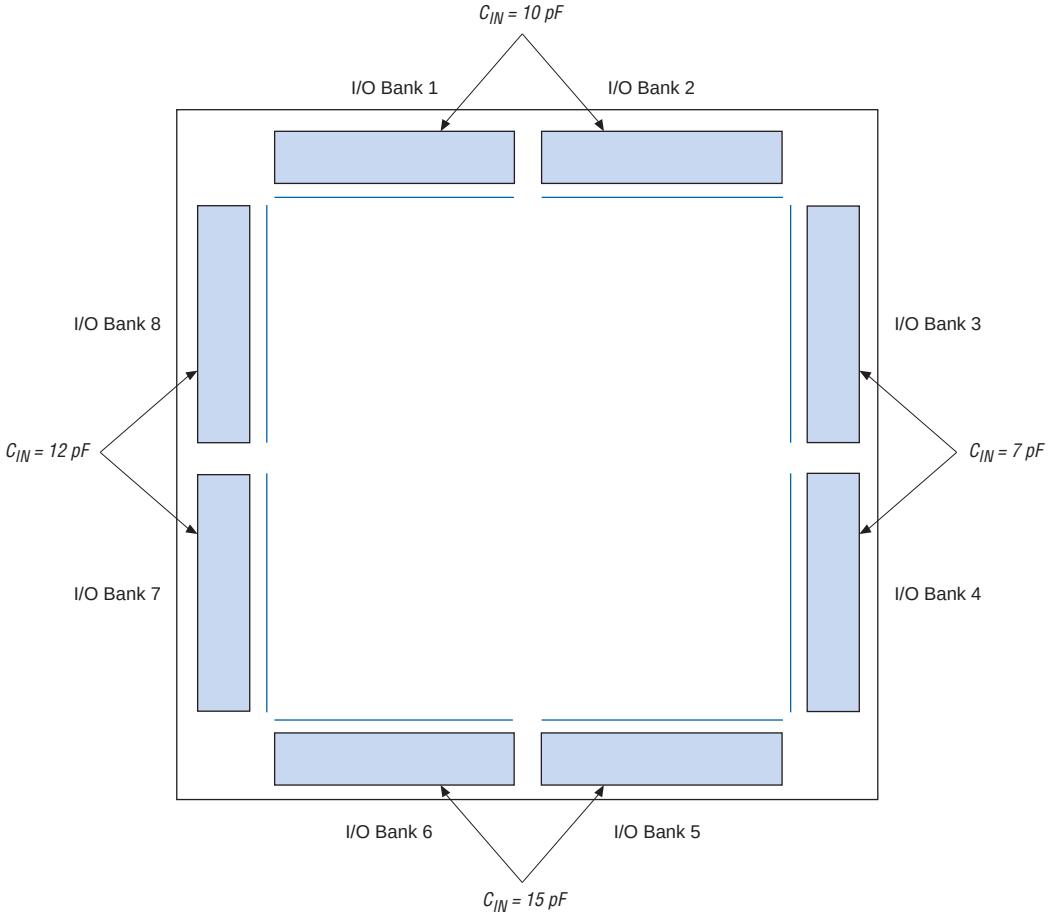


Table 50. APEX II Minimum Pulse Width Timing Parameters	
Symbol	**Parameter**
t_{CH}	Minimum clock high time from clock pin
t_{CL}	Minimum clock low time from clock pin
t_{CLRP}	LE clear pulse width
t_{PREP}	LE preset pulse width
t_{ESBCH}	Clock high time
t_{ESBCL}	Clock low time
t_{ESBWP}	Write pulse width
t_{ESBRP}	Read pulse width

Table 51. APEX II External Timing Parameters Note (1)		
Symbol	**Parameter**	**Conditions**
t_{INSU}	Setup time with global clock at IOE input register	
t_{INH}	Hold time with global clock at IOE input register	
t_{OUTCO}	Clock-to-output delay with global clock at IOE output register	C1 = 35 pF
t_{XZ}	Clock-to-output buffer disable delay	
t_{ZX}	Clock-to-output buffer enable delay	Slow slew rate = OFF
$t_{INSUPLL}$	Setup time with PLL clock at IOE input register	
t_{INHPLL}	Hold time with PLL clock at IOE input register	
$t_{OUTCOPLL}$	Clock-to-output delay with PLL clock at IOE output register	C1 = 35 pF
t_{XZPLL}	PLL clock-to-output buffer disable delay	
t_{ZXPLL}	PLL clock-to-output buffer enable delay	Slow slew rate = OFF

Note to Table 51:

(1) External timing parameters are factory tested, worst-case values specified by Altera. These timing parameters are sample-tested only.

Table 76. APEX II Selectable I/O Standards Input Adder Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
LVCMOS		0.00		0.00		0.00	ns
LVTTL		0.00		0.00		0.00	ns
1.5 V		0.10		0.11		0.12	ns
1.8 V		0.00		0.00		0.00	ns
2.5 V		0.00		0.00		0.00	ns
3.3-V PCI		0.00		0.00		0.00	ns
3.3-V PCI-X		0.00		0.00		0.00	ns
GTL+		– 0.20		– 0.22		– 0.24	ns
SSTL-3 Class I		– 0.17		– 0.19		– 0.20	ns
SSTL-3 Class II		– 0.17		– 0.19		– 0.20	ns
SSTL-2 Class I		– 0.24		– 0.26		– 0.29	ns
SSTL-2 Class II		– 0.24		– 0.26		– 0.29	ns
HSTL Class I		– 0.03		– 0.03		– 0.03	ns
HSTL Class II		– 0.03		– 0.03		– 0.03	ns
LVDS		– 0.23		– 0.26		– 0.28	ns
LVPECL		– 0.23		– 0.26		– 0.28	ns
PCML		– 0.23		– 0.26		– 0.28	ns
CTT		0.00		0.00		0.00	ns
3.3-V AGP 1×		0.00		0.00		0.00	ns
3.3-V AGP 2×		0.00		0.00		0.00	ns
HyperTransport		– 0.23		– 0.26		– 0.28	ns
Differential HSTL		– 0.23		– 0.26		– 0.28	ns