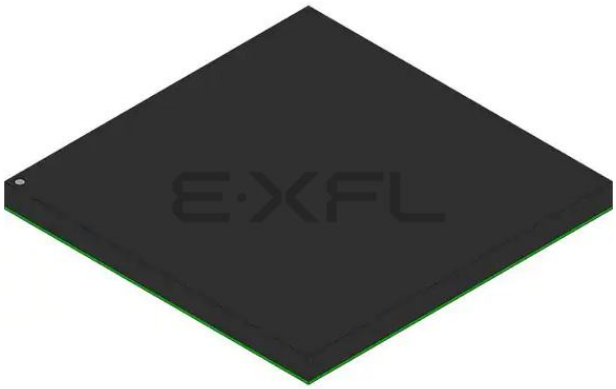


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6720
Number of Logic Elements/Cells	67200
Total RAM Bits	1146880
Number of I/O	1060
Number of Gates	5250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a70f1508c7

Table 1. APEX II Device Features

Feature	EP2A15	EP2A25	EP2A40	EP2A70
Maximum gates	1,900,000	2,750,000	3,000,000	5,250,000
Typical gates	600,000	900,000	1,500,000	3,000,000
LEs	16,640	24,320	38,400	67,200
RAM ESBs	104	152	160	280
Maximum RAM bits	425,984	622,592	655,360	1,146,880
True-LVDS channels	36 *(1)*	36 *(1)*	36 *(1)*	36 *(1)*
Flexible-LVDS™ channels *(2)*	56	56	88	88
True-LVDS PLLs *(3)*	4	4	4	4
General-purpose PLL outputs *(4)*	8	8	8	8
Maximum user I/O pins	492	612	735	1,060

Notes to Table 1:

(1) Each device has 36 input channels and 36 output channels.
(2) EP2A15 and EP2A25 devices have 56 input and 56 output channels; EP2A40 and EP2A70 devices have 88 input and 88 output channels.
(3) PLL: phase-locked loop. True-LVDS PLLs are dedicated to implement True-LVDS functionality.
(4) Two internal outputs per PLL are available. Additionally, the device has one external output per PLL pair (two external outputs per device).

…and More Features

- I/O features
  - Up to 380 Gbps of I/O capability
  - 1-Gbps True-LVDS, LVPECL, PCML, and HyperTransport support on 36 input and 36 output channels that feature clock synchronization circuitry and independent clock multiplication and serialization/deserialization factors
  - Common networking and communications bus I/O standards such as RapidIO, CSIX, Utopia IV, and POS-PHY Level 4 enabled
  - 400-megabits per second (Mbps) Flexible-LVDS and HyperTransport support on up to 88 input and 88 output channels (input channels also support LVPECL)
  - Support for high-speed external memories, including ZBT, QDR, and DDR SRAM, and SDR and DDR SDRAM
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Compliant with 133-MHz PCI-X specifications
  - Support for other advanced I/O standards, including AGP, CTT, SSTL-3 and SSTL-2 Class I and II, GTL+, and HSTL Class I and II
  - Six dedicated registers in each I/O element (IOE): two input registers, two output registers, and two output-enable registers
  - Programmable bus hold feature
  - Programmable pull-up resistor on I/O pins available during user mode

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

Each I/O pin is fed by an IOE located at the end of each row and column of the FastTrack interconnect. Each IOE contains a bidirectional I/O buffer and six registers that can be used for registering input, output, and output-enable signals. When used with a dedicated clock pin, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM and ZBT and QDR SRAM devices.

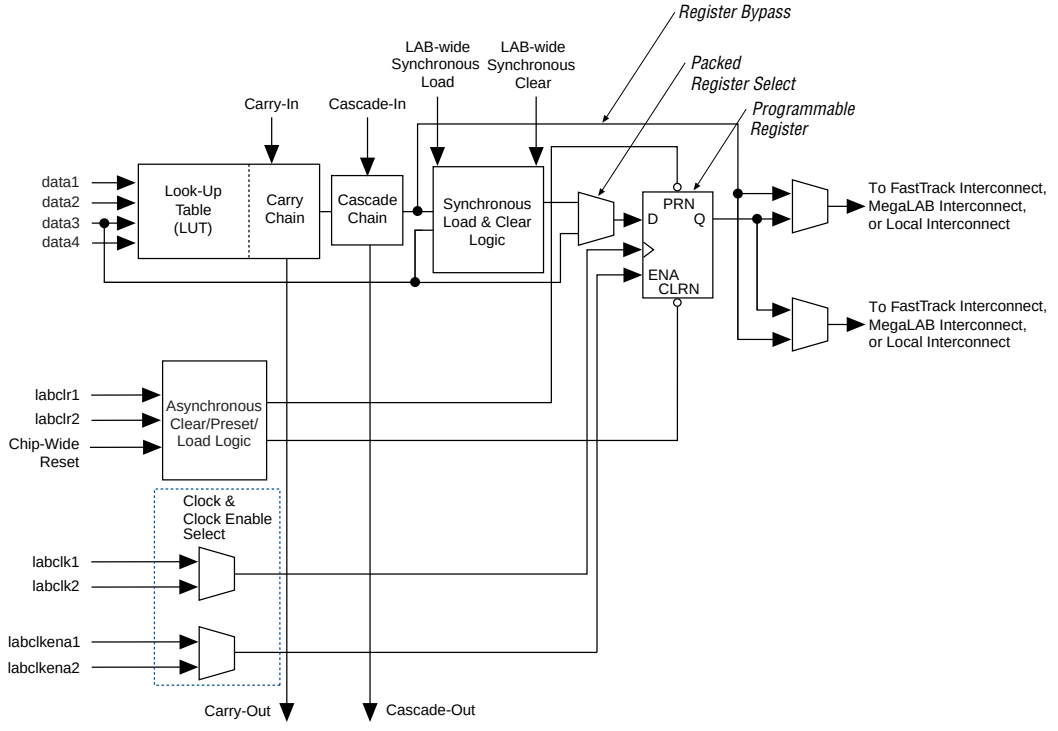
IOEs provide a variety of features such as: 3.3-V, 64-bit, 66-MHz PCI compliance, 3.3-V, 64-bit, 133-MHz PCI-X compliance, Joint Test Action Group (JTAG) boundary-scan test (BST) support, output drive strength control, slew-rate control, tri-state buffers, bus-hold circuitry, programmable pull-up resistors, programmable input and output delays, and open-drain outputs.

APEX II devices offer enhanced I/O support, including support for 1.5 V, 1.8 V, 2.5 V, 3.3 V, LVCMOS, LVTTL, HSTL, LVDS, LVPECL, HyperTransport, PCML, 3.3-V PCI, PCI-X, GTL+, SSTL-2, SSTL-3, CTT, and 3.3-V AGP I/O standards. High-speed (up to 1.0 Gbps) differential transfers are supported with True-LVDS circuitry for LVDS, LVPECL, HyperTransport, and PCML I/O standards. The optional CDS feature corrects any clock-to-data skew at the True-LVDS receiver channels, allowing for flexible board topologies. Up to 88 Flexible-LVDS channels support differential transfer at up to 400 Mbps (DDR) for LVDS and HyperTransport I/O standards.

An ESB can implement many types of memory, including Dual-Port+ RAM, CAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. The abundance of cascadable ESBs ensures that the APEX II device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs, in conjunction with the ability for one ESB to implement two separate memory blocks, ensures that designers can create as many different-sized memory blocks as the system requires.

Figure 1 shows an overview of the APEX II device.

Figure 5. APEX II Logic Element



Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

LE Operating Modes

The APEX II LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

A column line can be directly driven by the LEs, IOEs, or ESBs in that column. Row IOEs can drive a column line on a device's left or right edge. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack interconnect uses the local interconnect to drive LEs within MegaLAB structures.

Figure 10. FastTrack Connection to Local Interconnect

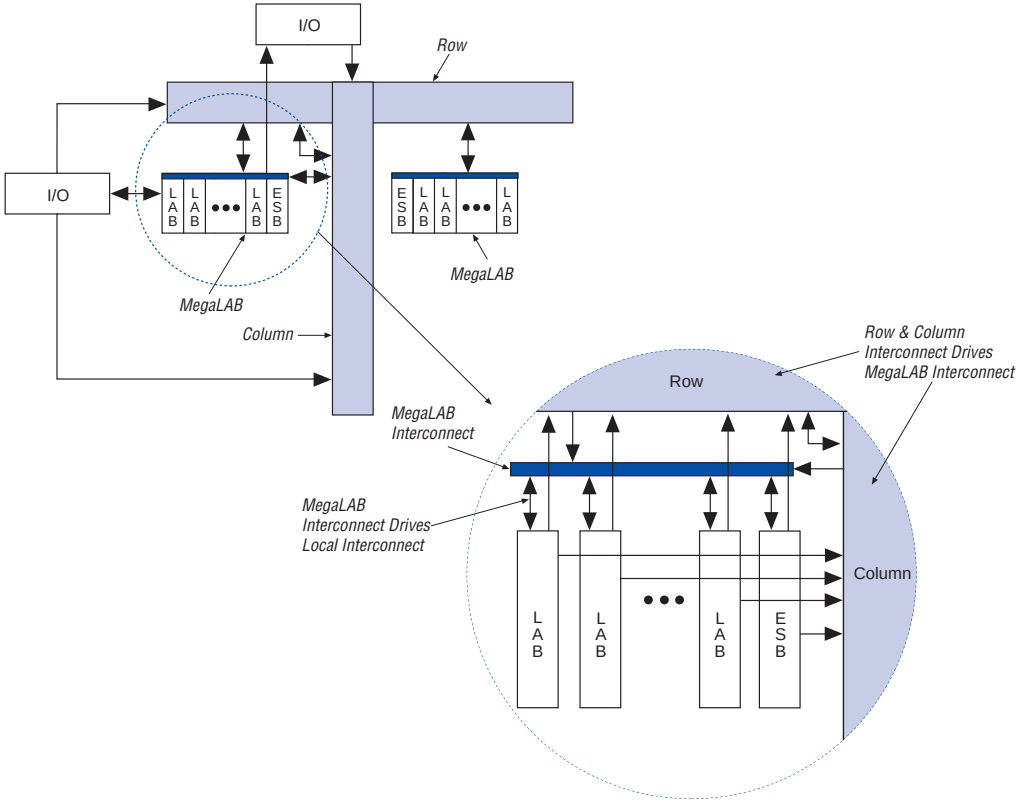
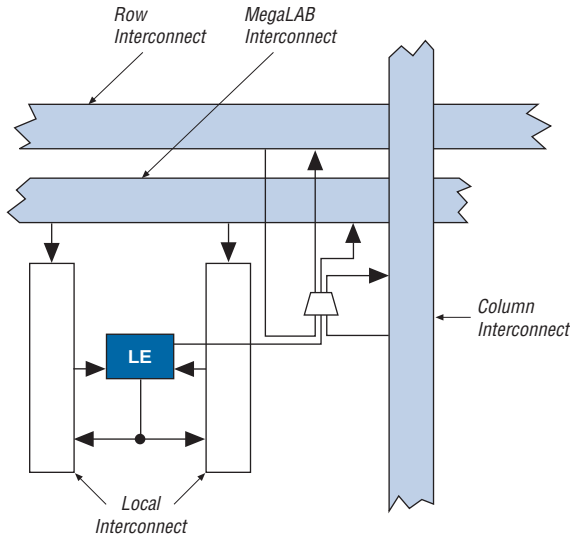


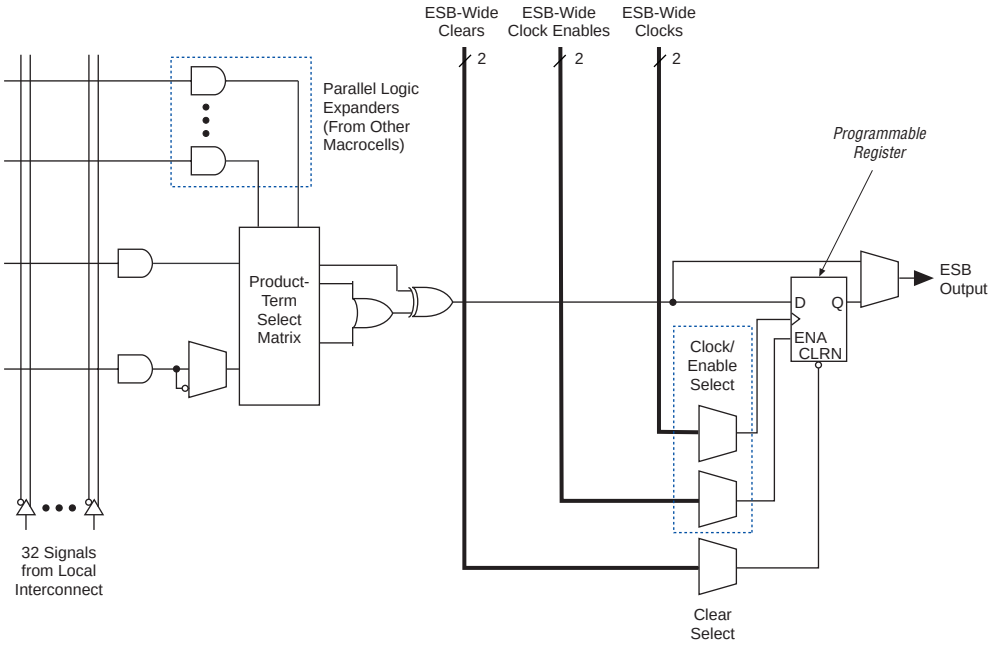
Figure 11 shows the intersection of a row and column interconnect and how these forms of interconnects and LEs drive each other.

Figure 11. Driving the FastTrack Interconnect



APEX II devices feature FastRow™ lines for quickly routing input signals with high fan-out. Column I/O pins can drive the FastRow interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. The FastRow interconnect drives the four MegaLABs in the top row and the four MegaLABs in the bottom row of the device. The FastRow interconnect drives all local interconnects in the appropriate MegaLABs. Column pins using the FastRow interconnect achieve a faster set-up time, because the signal does not need to use a MegaLab interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

Figure 14. APEX II Macrocell



For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The ESB also enables variable width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the ESB can be written in 1× mode at port A while being read in 16× mode from port B. Table 6 lists the supported variable width configurations for an ESB in dual-port mode.

Table 6. Variable Width Configurations for Dual-Port RAM

Read Port Width	Write Port Width
1 bit	2 bits, 4 bits, 8 bits, or 16 bits
2 bits, 4 bits, 8 bits, or 16 bits	1 bit

ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM only need to meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack interconnects. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack interconnects and the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 512 × 8, 1,024 × 4, 2,048 × 2, or 4,096 × 1. For dual-port and single-port modes, the ESB can be configured for 256 × 16 in addition to the list above.

The ESB can also be split in half and used for two independent 2,048-bit single-port RAM blocks. The two independent RAM blocks must have identical configurations with a maximum width of 256 × 8. For example, one half of the ESB can be used as a 256 × 8 single-port memory while the other half is also used for a 256 × 8 single-port memory. This effectively doubles the number of RAM blocks an APEX II device can implement for its given number of ESBs. The Quartus II software automatically merges two logical memory functions in a design into an ESB; the designer does not need to merge the functions manually.

Pre-programmed CDS may also be used to resolve clock-to-data skew greater than 50% of the bit period. However, internal logic must be used to implement the byte alignment circuitry for this operation.

Flexible-LVDS I/O Pins

A subset of pins in the top two I/O banks supports interfacing with Flexible-LVDS, LVPECL, and HyperTransport inputs. These Flexible-LVDS input pins include dedicated LVDS, LVPECL, and HyperTransport input buffers. A subset of pins in the bottom two I/O banks supports interfacing with Flexible-LVDS and HyperTransport outputs. These Flexible-LVDS output pins include dedicated LVDS and HyperTransport output buffers. The Flexible-LVDS pins do not require any external components except for 100-Ω termination resistors on receiver channels. These pins do not contain dedicated serialization/deserialization circuitry; therefore, internal logic is used to perform serialization/deserialization functions.

The EP2A15 and EP2A25 devices support 56 input and 56 output Flexible-LVDS channels. The EP2A40 and larger devices support 88 input and 88 output Flexible-LVDS channels. All APEX II devices support the Flexible-LVDS interface up to 400 Mbps (DDR) per channel. Flexible-LVDS pins along with the True-LVDS pins provide up to 144-Gbps total device bandwidth. Table 13 shows the Flexible-LVDS timing specification.

Table 13. APEX II Flexible-LVDS Timing Specification

Symbol	Timing Parameter Definition	Speed Grade						Unit
		-7		-8		-9		
		Min	Max	Min	Max	Min	Max	
Data Rate	Maximum operating speed		400		311		311	Mbps
TCCS	Transmitter channel-to-channel skew		700		900		900	ps
SW	Receiver sampling window	1,100		1,400		1,400		ps

MultiVolt I/O Interface

The APEX II architecture supports the MultiVolt I/O interface feature, which allows APEX II devices in all packages to interface with systems of different supply voltages. The devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX II devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX II devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam™ Standard Test and Programming Language (STAPL) Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX II devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX II devices support the JTAG instructions shown in Table 16.

Table 16. APEX II JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer.
EXTEST *(1)*	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	Used when configuring an APEX II device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor.
SignalTap instructions	Monitors internal device operation with the SignalTap embedded logic analyzer.

Note to Table 16:

(1) Bus hold and weak pull-up features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The APEX II device instruction register length is 10 bits. The APEX II device USERCODE register length is 32 bits. Tables 17 and 18 show the boundary-scan register length and device IDCODE information for APEX II devices.

Tables 20 through 41 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 20. APEX II Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground *(3)*	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	BGA packages under bias		135	° C

Table 21. APEX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(4)*	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(4)*, *(5)*	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	*(4)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	*(4)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	*(4)*	1.4	1.6	V
V_I	Input voltage	*(3)*, *(6)*	–0.5	4.1	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 25. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA		0.7	V

Table 26. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 27. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 37. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –8 mA *(10)*			0.4	V

Table 38. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(10)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = –16 mA *(10)*			0.4	V

Table 39. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Timing Model

The high-performance FastTrack and MegaLAB interconnect routing structures ensure predictable performance, and accurate simulation and timing analysis. In contrast, the unpredictable performance of FPGAs is caused by their segmented connection scheme.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum drive strength.

Figure 41 shows the f_{MAX} timing model for APEX II devices. These parameters can be used to estimate f_{MAX} for multiple levels of logic. However, the Quartus II software timing analysis provides more accurate timing information because the Quartus II software usually has more up-to-date timing information than the data sheet until the timing model is final. Also, the Quartus II software can model delays caused by loading and distance effects more accurately than by using the numbers in this data sheet.

Table 48. APEX II f_{MAX} ESB Timing Parameters	
Symbol	**Parameter**
t_{ESBARC}	ESB asynchronous read cycle time
t_{ESBSRC}	ESB synchronous read cycle time
t_{ESBAWC}	ESB asynchronous write cycle time
t_{ESBSWC}	ESB synchronous write cycle time
$t_{ESBWASU}$	ESB write address setup time with respect to WE
t_{ESBWAH}	ESB write address hold time with respect to WE
$t_{ESBWDSU}$	ESB data setup time with respect to WE
t_{ESBWDH}	ESB data hold time with respect to WE
$t_{ESBRASU}$	ESB read address setup time with respect to RE
t_{ESBRAH}	ESB read address hold time with respect to RE
$t_{ESBWESU}$	ESB WE setup time before clock when using input register
$t_{ESBDATASU}$	ESB data setup time before clock when using input register
$t_{ESBWADDRSU}$	ESB write address setup time before clock when using input registers
$t_{ESBRADDRSU}$	ESB read address setup time before clock when using input registers
$t_{ESBDATACO1}$	ESB clock-to-output delay when using output registers
$t_{ESBDATACO2}$	ESB clock-to-output delay without output registers
t_{ESBDD}	ESB data-in to data-out delay for RAM mode
t_{PD}	ESB macrocell input to non-registered output
$t_{PTERMSU}$	ESB macrocell register setup time before clock
$t_{PTERMCO}$	ESB macrocell register clock-to-output delay

Figure shows the dual-port RAM timing microparameter waveform.

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns

Table 54. EP2A15 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.19		0.21		0.25		ns
t_{F5-20}	0.64		0.73		0.84		ns
t_{F20+}	1.18		1.35		1.56		ns

Table 55. EP2A15 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.00		1.15		1.32		ns
t_{CL}	1.00		1.15		1.32		ns
t_{CLRP}	0.13		0.15		0.17		ns
t_{PREP}	0.13		0.15		0.17		ns
t_{ESBCH}	1.00		1.15		1.32		ns
t_{ESBCL}	1.00		1.15		1.32		ns
t_{ESBWP}	1.12		1.28		1.48		ns
t_{ESBRP}	0.88		1.02		1.17		ns

Table 56. EP2A25 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 65. EP2A70 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		3.12		3.58		4.12	ns
t_{ESBSRC}		3.11		3.58		4.11	ns
t_{ESBAWC}		4.41		5.07		5.83	ns
t_{ESBSWC}		3.82		4.39		5.05	ns
$t_{ESBWASU}$	1.73		1.99		2.28		ns
t_{ESBWAH}	0.00		0.00		0.00		ns
$t_{ESBWDSU}$	1.87		2.15		2.47		ns
t_{ESBWDH}	0.00		0.00		0.00		ns
$t_{ESBRASU}$	2.76		3.17		3.65		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	1.98		2.27		2.61		ns
$t_{ESBDATASU}$	1.06		1.22		1.40		ns
$t_{ESBWADDRSU}$	1.17		1.34		1.54		ns
$t_{ESBRADDRSU}$	1.02		1.17		1.35		ns
$t_{ESBDATACO1}$		1.52		1.75		2.01	ns
$t_{ESBDATACO2}$		2.35		2.71		3.11	ns
t_{ESBDD}		4.43		5.10		5.87	ns
t_{PD}		2.17		2.49		2.87	ns
$t_{PTERMSU}$	1.40		1.62		1.86		ns
$t_{PTERMCO}$		1.08		1.24		1.42	ns

Table 66. EP2A70 f_{MAX} Routing Delays

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{F1-4}	0.15		0.18		0.20		ns
t_{F5-20}	1.21		1.39		1.60		ns
t_{F20+}	1.87		2.15		2.55		ns

Table 67. EP2A70 Minimum Pulse Width Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CH}	1.19		1.78		2.53		ns
t_{CL}	1.19		1.78		2.53		ns
t_{CLRP}	0.16		0.19		0.21		ns
t_{PREP}	0.16		0.19		0.21		ns
t_{ESBCH}	1.19		1.78		2.53		ns
t_{ESBCL}	1.19		1.78		2.53		ns
t_{ESBWP}	1.35		1.56		1.79		ns
t_{ESBRP}	1.13		1.30		1.50		ns

Tables 68 through 77 show the IOE external timing parameter values for APEX II devices.

Table 68. EP2A15 External Timing Parameters for Row I/O Pins

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.06		2.25		2.46		ns
t_{INH}	0.00		0.00		0.00		ns
t_{OUTCO}	2.00	4.05	2.00	4.45	2.00	4.90	ns
t_{XZ}		4.98		5.59		6.26	ns
t_{ZX}		4.98		5.59		6.26	ns
$t_{INSUPLL}$	1.15		1.28		1.42		ns
t_{INHPLL}	0.00		0.00		0.00		ns
$t_{OUTCOPLL}$	0.50	2.60	0.50	2.87	0.50	3.16	ns
t_{XZPLL}		3.53		4.00		4.52	ns
t_{ZXPLL}		3.53		4.00		4.52	ns