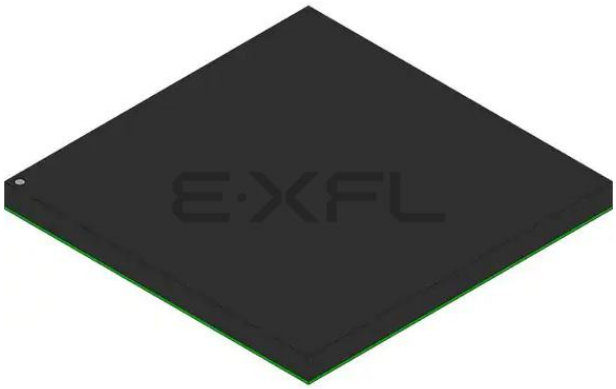


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6720
Number of Logic Elements/Cells	67200
Total RAM Bits	1146880
Number of I/O	1060
Number of Gates	5250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2a70f1508c8

  - Programmable output drive for 3.3-V LVTTL at 4 mA, 12 mA, 24 mA, or I/O standard levels
  - Programmable output slew-rate control reduces switching noise
  - Hot-socketing operation supported
  - Pull-up resistor on I/O pins before and during configuration
- Enhanced internal memory structure
  - High-density 4,096-bit ESBs
  - Dual-Port+ RAM with bidirectional read and write ports
  - Support for many other memory functions, including CAM, FIFO, and ROM
  - ESB packing mode partitions one ESB into two 2,048-bit blocks
- Device configuration
  - Fast byte-wide synchronous configuration minimizes in-circuit reconfiguration time
  - Device configuration supports multiple voltages (either 3.3 V and 2.5 V or 1.8 V)
- Flexible clock management circuitry with eight general-purpose PLL outputs
  - Four general-purpose PLLs with two outputs per PLL
  - Built-in low-skew clock tree
  - Eight global clock signals
  - ClockLock™ feature reducing clock delay and skew
  - ClockBoost™ feature providing clock multiplication (by 1 to 160) and division (by 1 to 256)
  - ClockShift™ feature providing programmable clock phase and delay shifting with coarse (90°, 180°, or 270°) and fine (0.5 to 1.0 ns) resolution
- Advanced interconnect structure
  - All-layer copper interconnect for high performance
  - Four-level hierarchical FastTrack® interconnect structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allowing one LE to drive 29 other LEs through the fast local interconnect
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus™ II development system for Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
  - Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions optimized for APEX II architecture

After an APEX II device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Software

APEX II devices are supported by the Altera Quartus II development system: a single, integrated package that offers hardware description language (HDL) and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software includes the LogicLock incremental design feature. The LogicLock feature allows the designer to make pin and timing assignments, verify functionality and performance, and then set constraints to lock down the placement and performance of a specific block of logic using LogicLock constraints. Constraints set by the LogicLock function guarantee repeatable placement when implementing a block of logic in a current project or exporting the block to another project. The constraints set by the LogicLock feature can lock down logic to a fixed location in the device. The LogicLock feature can also lock the logic down to a floating location, and the Quartus II software determines the best relative placement of the block to meet design requirements. Adding additional logic to a project will not affect the performance of blocks locked down with LogicLock constraints.

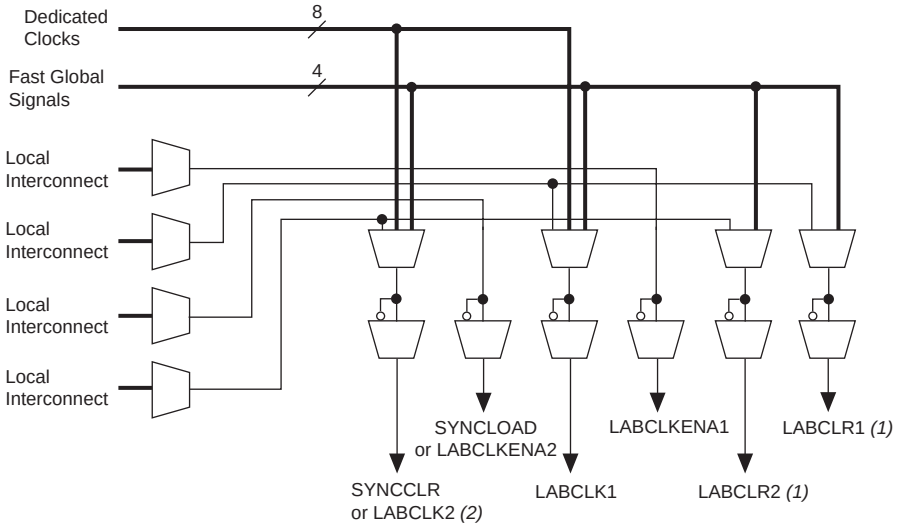
The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can open the Quartus II software from within third-party design tools. The Quartus II software also contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX II devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX II architecture.

Functional Description

APEX II devices incorporate LUT-based logic, product-term-based logic, memory, and high-speed I/O standards into one device. Signal interconnections within APEX II devices (as well as to and from device pins) are provided by the FastTrack interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

Figure 4. LAB Control Signal Generation



Notes to Figure 4:

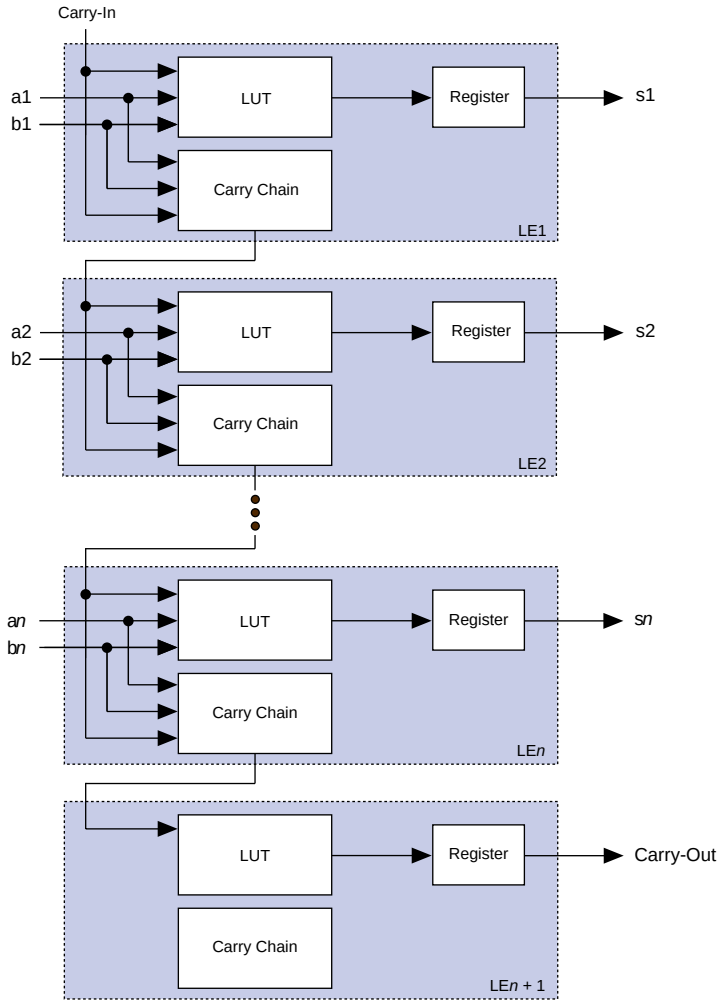
(1) The LABCLR1 and LABCLR2 signals also control asynchronous load and asynchronous preset for LEs within the LAB.

(2) The SYNCCLR signal can be generated by the local interconnect or global signals.

Logic Element

The LE is the smallest unit of logic in the APEX II architecture. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack interconnect routing structures. See Figure 5.

Figure 6. APEX II Carry Chain



LE Operating Modes

The APEX II LE can operate in one of the following three modes:

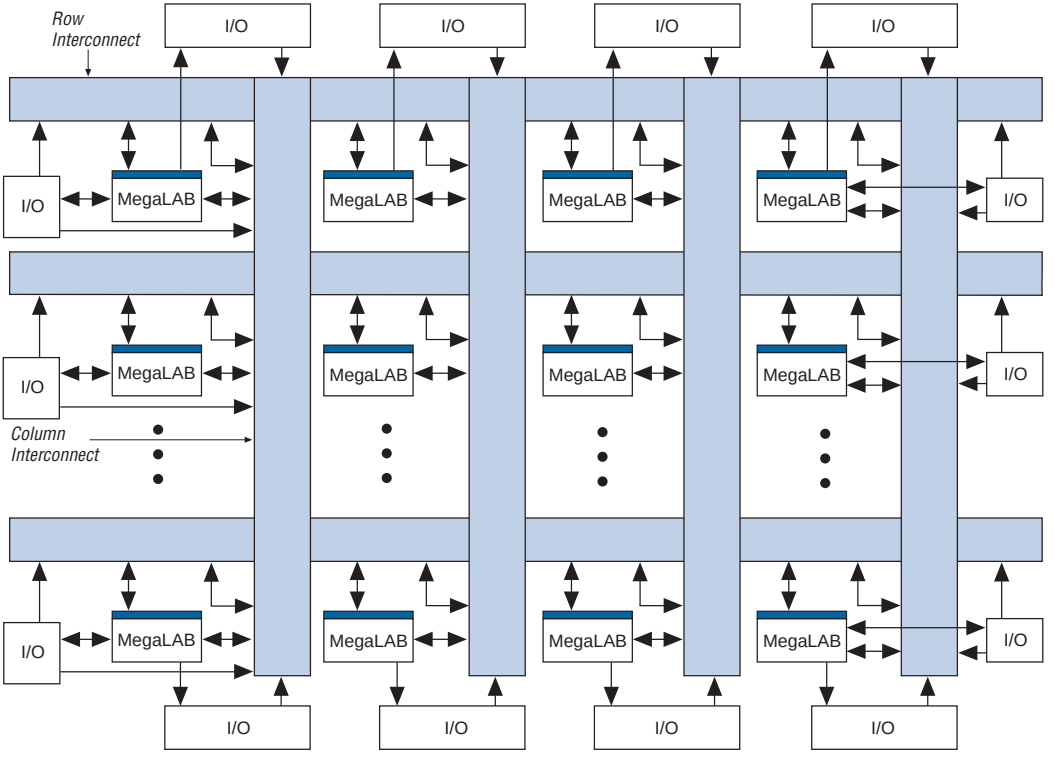
- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

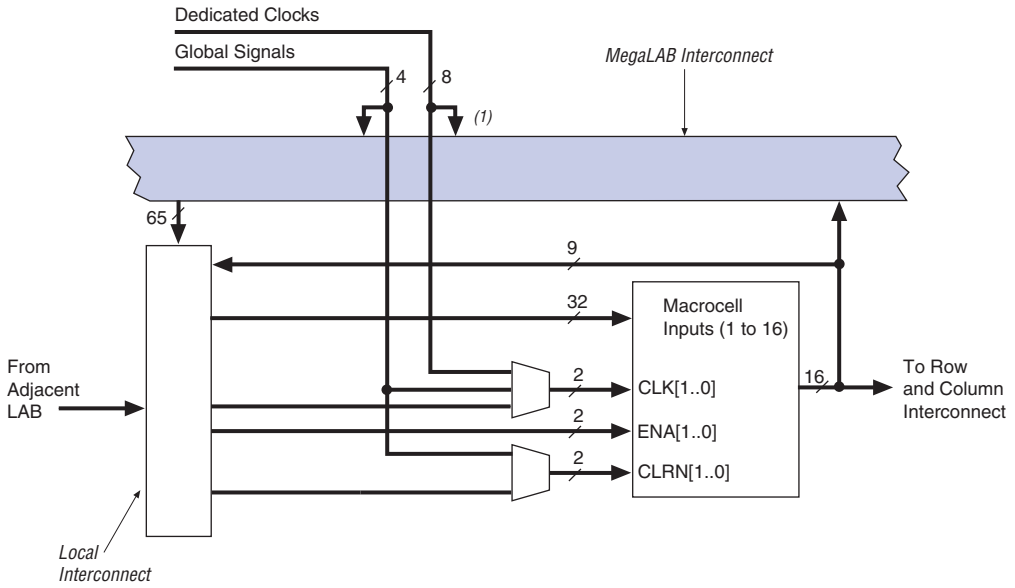
The FastTrack interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

Figure 9. APEX II Interconnect Structure



A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

Figure 13. Product-Term Logic in ESB



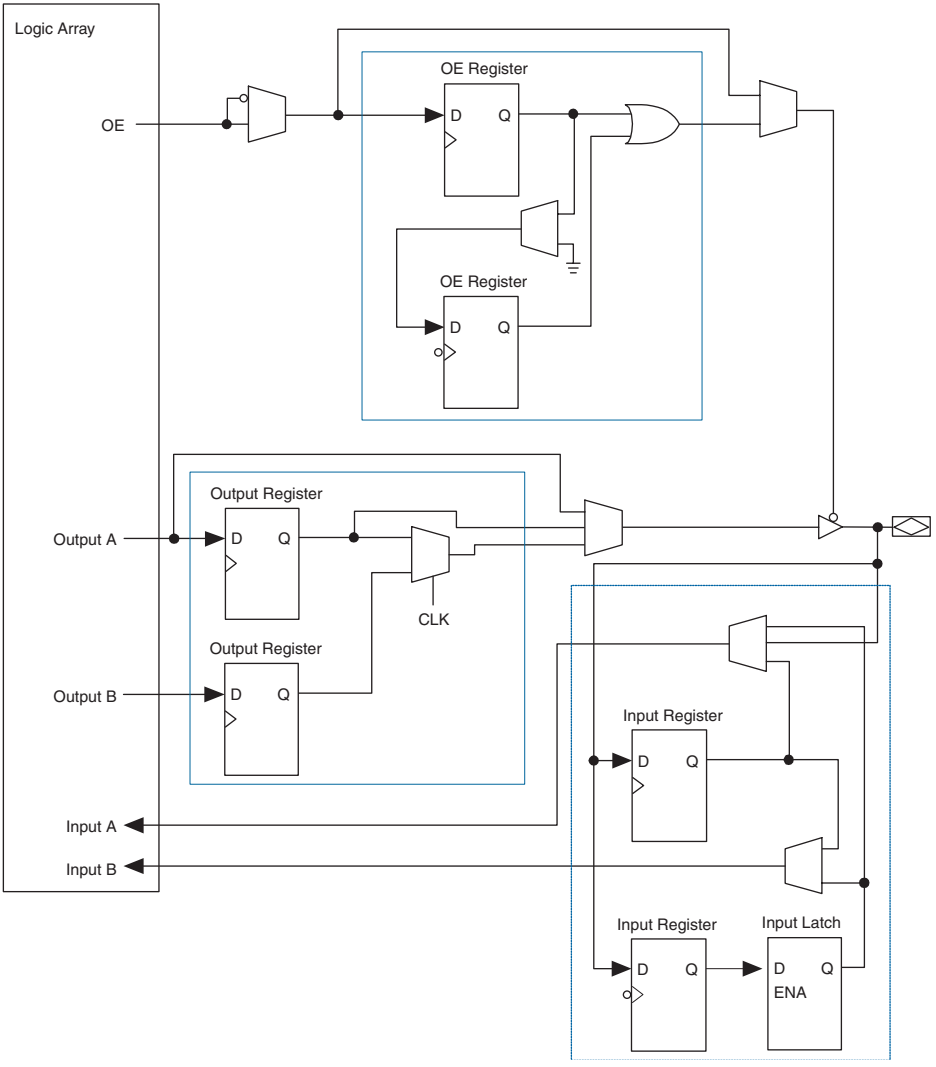
Note ot Figure 13:
(1) PLL outputs cannot drive data input ports.

Macrocells

APEX II macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX II macrocell.

Figure 25. APEX II IOE Structure



The IOEs are located around the periphery of the APEX II device. Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the FastTrack or column interconnect. Figure 26 shows how a row IOE connects to the interconnect.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input pin to logic array and IOE input register delays. The Quartus II Compiler can program these delays automatically to minimize setup time while providing a zero hold time. Delays are also programmable for increasing the register to pin delays for output and / or output enable registers. A programmable delay exists for increasing the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 8 shows the programmable delays for APEX II devices.

Table 8. APEX II Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay *(1)*	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output propagation delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register

Note to Table 8:
(1) This delay has four settings: off and three levels of delay.

The IOE registers in APEX II devices share the same source for clear or preset. The designer can program preset and clear for each individual IOE. The registers can be programmed to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that preset or clear signal.

Double Data Rate I/O

APEX II devices have six-register IOEs which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in APEX II devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

Each bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same V_{CCIO} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs. When the True-LVDS banks are not used for LVDS I/O pins, they support all of the other I/O standards except HSTL Class II output.

True-LVDS Interface

APEX II devices contain dedicated circuitry for supporting differential standards at speeds up to 1.0 Gbps. APEX II devices have dedicated differential buffers and circuitry to support LVDS, LVPECL, HyperTransport, and PCML I/O standards. Four dedicated high-speed PLLs (separate from the general-purpose PLLs) multiply reference clocks and drive high-speed differential serializer/deserializer channels. In addition, CDS circuitry at each receiver channel corrects any fixed clock-to-data skew. All APEX II devices support 36 input channels, 36 output channels, two dedicated receiver PLLs, and two dedicated transmitter PLLs.

The True-LVDS circuitry supports the following standards and applications:

- RapidIO
- POS-PHY Level 4
- Utopia IV
- HyperTransport

APEX II devices support source-synchronous interfacing with LVDS, LVPECL,PCML, or HyperTransport signaling at up to 1 Gbps. Serial channels are transmitted and received along with a low-speed clock. The receiving device then multiplies the clock by a factor of 1, 2, or 4 to 10. The serialization/deserialization rate can be any number from 1, 2, or 4 to 10 and does not have to equal the clock multiplication value.

For example, an 840-Mbps LVDS channel can be received along with an 84-MHz clock. The 84-MHz clock is multiplied by 10 to drive the serial shift register, but the register can be clocked out in parallel at 8- or 10-bits wide at 84 or 105 MHz. See Figures 32 and 33.

Single-Bit Mode

Single-bit CDS corrects a fixed clock-to-data skew of up to ±50% of the data bit period, which allows receiver input skew margin (RSKM) to increase by 50% of the data period. To use single-bit CDS, the deserialization factor, *J*, must be equal to the multiplication factor, *W*. The combination of allowable *W* / *J* factors and the associated CDS training patterns automatically determine byte alignment (see Table 11).

Table 11. Single-Bit CDS Training Patterns

W/J Factor	Single-Bit CDS Pattern
10	0000011111
9	000001111
8	00001111
7	0000111
6	000111
5	00011
4	0011

Multi-Bit Mode

Multi-bit CDS corrects any fixed clock-to-data skew. This feature enables flexible board topologies, such as an N:1 topology (see Figure 34), a switch topology, or a matrix topology. Multi-bit CDS corrects for the skews inherent with these topologies, making them possible to use.

Note to Figure 35:

(1) *n* represents the prescale divider for the PLL input. *m* represents the multiplier. *k* and *v* represent the different post scale dividers for the two possible PLL outputs. *m* and *k* are integers that range from 1 to 160. *n* and *v* are integers that range from 1 to 16.

Advanced ClockBoost Multiplication & Division

APEX II PLLs include circuitry that provides clock synthesis for eight internal outputs and two external outputs using $m / (n \times$ output divider) scaling. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. The closed loop equation for Figure 35 gives an output frequency $f_{clock0} = (m / (n \times k))f_{IN}$ and $f_{clock1} = (m / (n \times v))f_{IN}$. These equations allow the multiplication or division of clocks by a programmable number. The Quartus II software automatically chooses the appropriate scaling factors according to the frequency, multiplication, and division values entered.

A single PLL in an APEX II device allows for multiple user-defined multiplication and division ratios that are not possible even with multiple delay-locked loops (DLLs). For example, if a frequency scaling factor of 3.75 is needed for a given input clock, a multiplication factor of 15 and a division factor of 4 can be entered. This advanced multiplication scaling can be performed with a single PLL, making it unnecessary to cascade PLL outputs.

External Clock Outputs

APEX II devices have two low-jitter external clocks available for external clock sources. Other devices on the board can use these outputs as clock sources.

There are three modes for external clock outputs.

- Zero Delay Buffer: The external clock output pin is phase aligned with the clock input pin for zero delay. Multiplication, programmable phase shift, and time delay shift are not allowed in this configuration. The MegaWizard interface for `altclklock` should be used to verify possible clock settings.
- External Feedback: The external feedback input pin is phase aligned with clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. This mode has the same restrictions as zero delay buffer mode.
- Normal Mode: The external clock output pin will have phase delay relative to the clock input pin. If an internal clock is used in this mode, the IOE register clock will be phase aligned to the input clock pin. Multiplication is allowed with the normal mode.

ClockShift Circuitry

General-purpose PLLs in APEX II devices have ClockShift circuitry that provides programmable phase shift. Users can enter a phase shift (in degrees or time units) that affects all PLL outputs. Phase shifts of 90°, 180°, and 270° can be implemented exactly. Other values of phase shifting, or delay shifting in time units, are allowed with a resolution range of 0.5 ns to 1.0 ns. This resolution varies with frequency input and the user-entered multiplication and division factors. The phase shift ability is only possible on a multiplied or divided clock if the input and output frequency have an integer multiple relationship (i.e., f_{IN}/f_{OUT} or f_{OUT}/f_{IN} must be an integer).

Clock Enable Signal

APEX II PLLs have a CLKLK_ENA pin for enabling/disabling all device PLLs. When the CLKLK_ENA pin is high, the PLL drives a clock to all its output ports. When the CLKLK_ENA pin is low, the clock0, clock1, and extclock ports are driven by GND and all of the PLLs go out of lock. When the CLKLK_ENA pin goes high again, the PLL relocks.

The individual enable port for each PLL is programmable. If more than one PLL is instantiated, each one does not have to use the clock enable. To enable/disable the device PLLs with the CLKLK_ENA pin, the inclocken port on the altclklock instance must be connected to the CLKLK_ENA input pin.

Lock Signals

The APEX II device PLL circuits support individual LOCK signals. The LOCK signal drives high when the PLL has locked onto the input clock. LOCK remains high as long as the input remains within specification. It will go low if the input is out of specification. A LOCK pin is optional for each PLL used in the APEX II devices; when not used, they are I/O pins. This signal is not available internally; if it is used in the logic array, it must be fed back in with an input pin.

SignalTap Embedded Logic Analyzer

APEX II devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX II device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

Table 22. APEX II Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All ESBs in power-down mode)	V_I = ground, no load, no toggling inputs, -7 speed grade		10		mA
		V_I = ground, no load, no toggling inputs, -8, -9 speed grades		5		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 23. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–5	5	µA
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 24. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 25. 2.5-V I/O Specifications *Note (10)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA		0.7	V

Table 26. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 27. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	4.1	V
V_{IL}	Low-level input voltage		–0.5	$0.35 \times V_{CCIO}$	V
I_I	Input pin leakage current	V_{IN} = 0 V or V_{CCIO}	–10	10	µA
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Table 34. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
V_{IH}	High-level input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(10)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(10)*			V_{TT} – 0.8	V

Table 35. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		$0.39 \times V_{CCIO}$		$0.41 \times V_{CCIO}$	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Table 36. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(11)*		$0.5 \times V_{CCIO}$		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(11)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OUT} = –20 µA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 20 µA			$0.1 \times V_{CCIO}$	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA

Figures 38 and 39 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 38. Receiver Input Waveforms for Differential I/O Standards

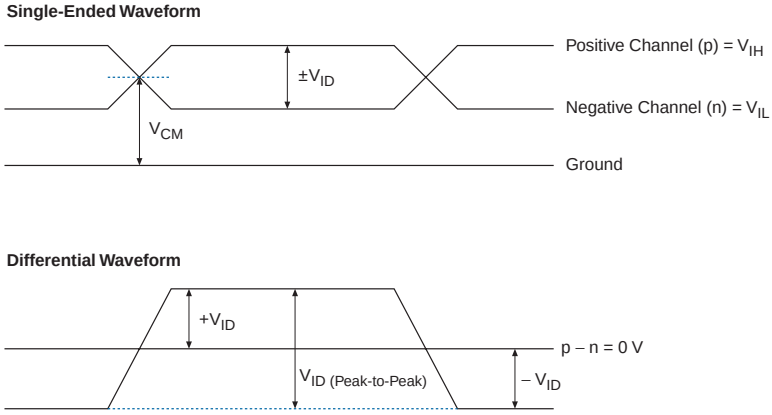
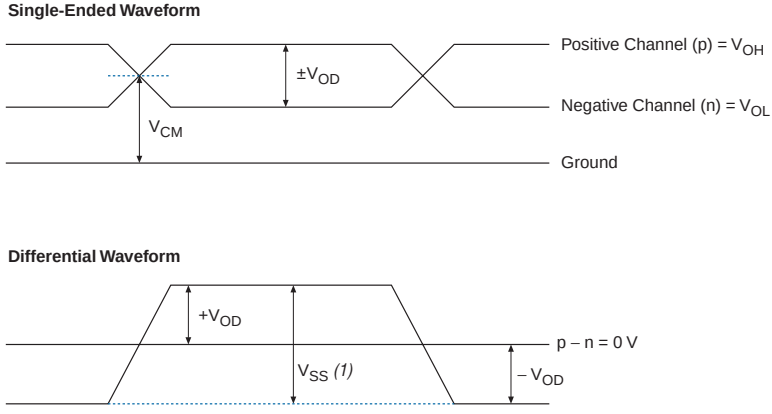


Figure 39. Transmitter Output Waveforms for Differential I/O Standards



Note to Figure 39:
(1) V_{SS}: steady-state differential output voltage.

Tables 42 through 45 provide information on absolute maximum ratings, recommended operating conditions, and DC operating conditions for 1.5-V APEX II devices.

Table 42. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{OD}	Differential output voltage	R_L = 100 Ω	250		850 *(1)*	mV
ΔV_{OD}	Change in V_{OD} between high and low	R_L = 100 Ω			50	mV
V_{OS}	Output Offset voltage	R_L = 100 Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between high and low	R_L = 100 Ω			50	mV
V_{TH}	Differential input threshold	V_{CM} = 1.2 V	–100		100	mV
V_{IN}	Receiver input voltage range		0.0		2.4	V
R_L	Receiver differential input resistor (external to APEX II devices)		90	100	110	Ω

Table 43. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{IL}	Low-level input voltage				V_{CCIO} – 0.3	V
V_{IH}	High-level input voltage		V_{CCIO}			V
V_{OL}	Low-level output voltage		V_{CCIO} – 0.6		V_{CCIO} – 0.3	V
V_{OH}	High-level output voltage		V_{CCIO}		V_{CCIO} – 0.3	V
V_T	Output termination voltage			V_{CCIO}		V
V_{OD}	Differential output voltage		300	450	600	mV
t_R	Rise time (20 to 80%)		85		325	ps
t_F	Fall time (20 to 80%)		85		325	ps
R_O	Output load			100		Ω
R_L	Receiver differential input resistor		45	50	55	Ω

Figure 43. Dual-Port RAM Timing Microparameter Waveform

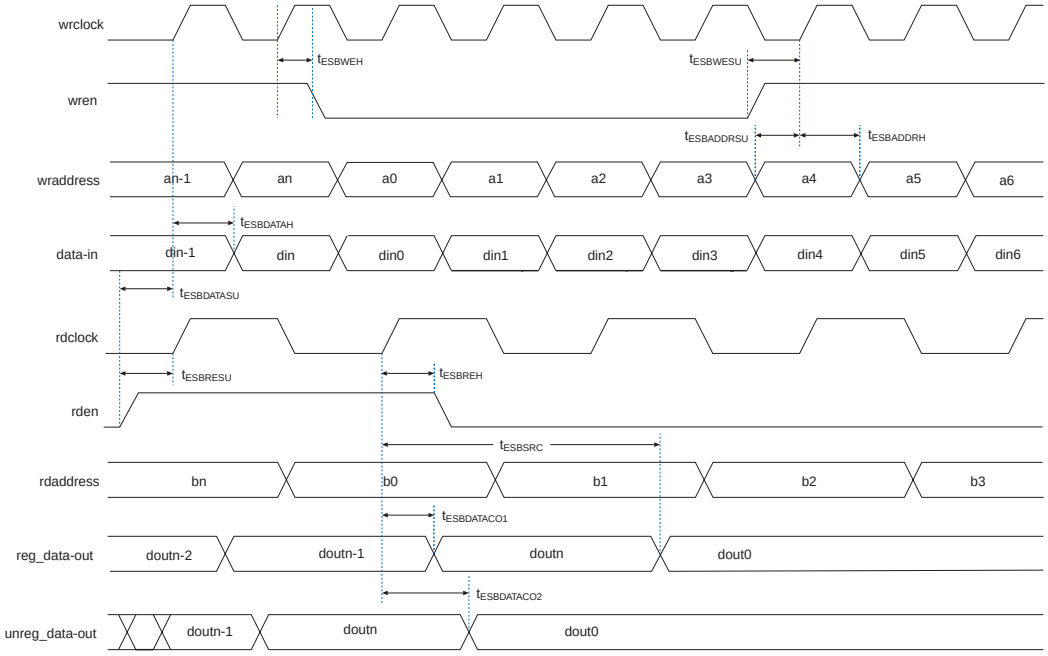


Table 49. APEX II f_{MAX} Routing Delays	
Symbol	**Parameter**
t_{F1-4}	Fan-out delay estimate using local interconnect; use to estimate routing delay for a signal with fan-out of 1 to 4
t_{F5-20}	Fan-out delay estimate using MegaLab interconnect; use to estimate routing delay for a signal with fan-out of 5 to 20
t_{F20+}	Fan-out delay estimate using FastTrack interconnect; use to estimate routing delay for a signal with fan-out greater than 20

Tables 52 through 67 show the APEX II device f_{MAX} and functional timing parameters.

Table 52. EP2A15 f_{MAX} LE Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{SU}	0.25		0.29		0.33		ns
t_{H}	0.25		0.29		0.33		ns
t_{CO}		0.18		0.20		0.23	ns
t_{LUT}		0.53		0.61		0.70	ns

Table 53. EP2A15 f_{MAX} ESB Timing Parameters

Symbol	-7 Speed Grade		-8 Speed Grade		-9 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ESBARC}		1.28		1.47		1.69	ns
t_{ESBSRC}		2.49		2.86		3.29	ns
t_{ESBAWC}		2.20		2.53		2.91	ns
t_{ESBSWC}		3.02		3.47		3.99	ns
$t_{ESBWASU}$	– 0.55		– 0.64		– 0.73		ns
t_{ESBWAH}	0.15		0.18		0.20		ns
$t_{ESBWDSU}$	0.37		0.43		0.49		ns
t_{ESBWDH}	0.16		0.18		0.21		ns
$t_{ESBRASU}$	0.84		0.96		1.11		ns
t_{ESBRAH}	0.00		0.00		0.00		ns
$t_{ESBWESU}$	0.14		0.16		0.19		ns
$t_{ESBDATASU}$	– 0.02		– 0.03		– 0.03		ns
$t_{ESBWADDRSU}$	– 0.40		– 0.46		– 0.53		ns
$t_{ESBRADDRSU}$	– 0.38		– 0.44		– 0.51		ns
$t_{ESBDATACO1}$		1.30		1.50		1.72	ns
$t_{ESBDATACO2}$		1.84		2.12		2.44	ns
t_{ESBDD}		2.42		2.78		3.19	ns
t_{PD}		1.69		1.94		2.23	ns
$t_{PTERMSU}$	1.10		1.26		1.45		ns
$t_{PTERMCO}$		0.82		0.94		1.08	ns