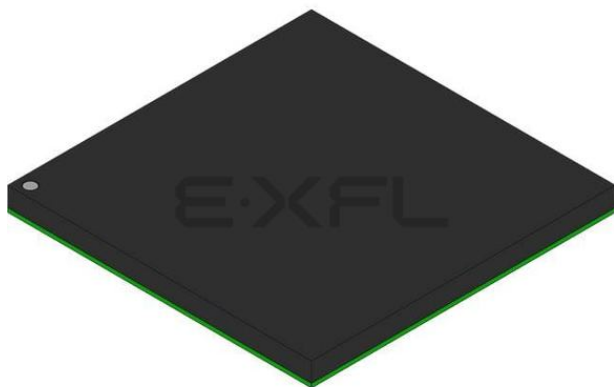




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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mxlcvp15

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
UART1_RTS	Request to Send
UART1_CTS	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
UART2_RTS	Request to Send
UART2_CTS	Clear to Send
UART2_DSR	Data Set Ready
UART2_RI	Ring Indicator
UART2_DCD	Data Carrier Detect
UART2_DTR	Data Terminal Ready
Serial Audio Port – SSI (configurable to I²S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I²C	
I2C_SCL	I ² C Clock
I2C_SDA	I ² C Data

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	N11	T9	DQM2	O									
NVDD1	P11	N9	DQM1	O									
NVDD1	N12	R10	DQM0	O									
NVDD1	P12	M9	RAS	O									
NVDD1	R13	L8	CAS	O									
NVDD1	R14	T10	SDWE	O									
NVDD1	N13	R11	SDCKE0	O									
NVDD1	P13	P10	SDCKE1	O									
NVDD1	P15	N10	RESET_SF	O									
NVDD1	P14	T11	CLKO	O									
AVDD1	R15	T12	AVDD1	Static									
QVDD2	M13	R15	QVDD2	Static									
AVDD1	N15	P13	TRST	I	69K								
AVDD1	N14	T13	TRISTATE ₁	I									
AVDD1	M15	T14	EXTAL16M	I									
AVDD1	L14	T15	XTAL16M	O									
AVDD1	L15	R16	EXTAL32K	I									
AVDD1	K15	P16	XTAL32K	O									
AVDD1	M14	M10	RESET_I _N ²	I	69K								
AVDD1	K14	N11	RESET_O _{UT}	O									
AVDD1	L12	R12	POR ²	I									
AVDD1	K13	M11	BIG_ENDI _{AN} ³	I									
AVDD1	M12	P11	BOOT3 ³	I									
AVDD1	K11	N12	BOOT2 ³	I									
AVDD1	J14	R13	BOOT1 ³	I									
AVDD1	J15	P12	BOOT0 ³	I									
NVDD2	J13	R14	TDO ⁴	O									
NVDD2	H15	N15	TMS	I	69K								
NVDD2	J12	L9	TCK	I	69K								
NVDD2	K12	N16	TDI	I	69K								
NVDD2	J11	P14	I2C_SCL	O				PA16	69K				PA16
NVDD2	H14	P15	I2C_SDA	I/O				PA15	69K				PA15

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD2	D11	G14	LP/HSYN C	O				PD13	69K				PD13
NVDD2	E11	G13	ACD/OE	O				PD12	69K				PD12
NVDD2	C10	G12	CONTRA ST	O				PD11	69K				PD11
NVDD2	B11	F16	SPL_SPR	O		UART2_D SR	O	PD10	69K	SPI2_TXD			PD10
NVDD2	A12	H10	PS	O		UART2_RI	O	PD9	69K			SPI2_RXD_1	PD9
NVDD2	F10	G11	CLS	O		UART2_D CD	O	PD8	69K	SPI2_SS			PD8
NVDD2	A11	F12	REV	O		UART2_D TR	I	PD7	69K	SPI2_SCLK			PD7
NVDD2	B10	F15	LSCLK	O				PD6	69K				PD6
NVDD3	D10	G9	SPI1_MO SI	I/O				PC17	69K				PC17
NVDD3	E10	F9	SPI1_MIS O	I/O				PC16	69K				PC16
NVDD3	B9	E9	SPI1_SS	I/O				PC15	69K				PC15
NVDD3	A10	B9	SPI1_SCL K	I/O				PC14	69K				PC14
NVDD3	A9	D9	SPI1_SPI_RDY	I/O				PC13	69K			DMA_REQ	PC13
NVDD3	E8	A9	UART1_R XD	I				PC12	69K				PC12
NVDD3	B8	C9	UART1_T XD	O				PC11	69K				PC11
NVDD3	C9	A8	UART1_R TS	I				PC10	69K				PC10
NVDD3	E9	G8	UART1_C TS	O				PC9	69K				PC9
NVDD3	A8	B8	SSI_TXCL K	I/O				PC8	69K				PC8
NVDD3	C8	F8	SSI_TXFS	I/O				PC7	69K				PC7
NVDD3	F9	E8	SSI_TXDA T	O				PC6	69K				PC6
NVDD3	B7	D8	SSI_RXD AT	I				PC5	69K				PC5
NVDD3	F8	B7	SSI_RXCL K	I				PC4	69K				PC4
NVDD3	A7	C8	SSI_RXFS	I				PC3	69K				PC3
NVDD4	C7	C7	UART2_R XD	I				PB31	69K				PB31

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXL.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

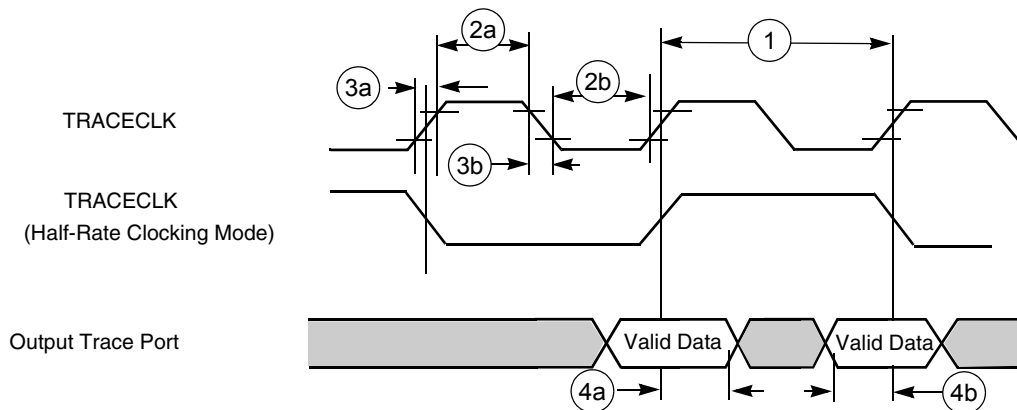


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns

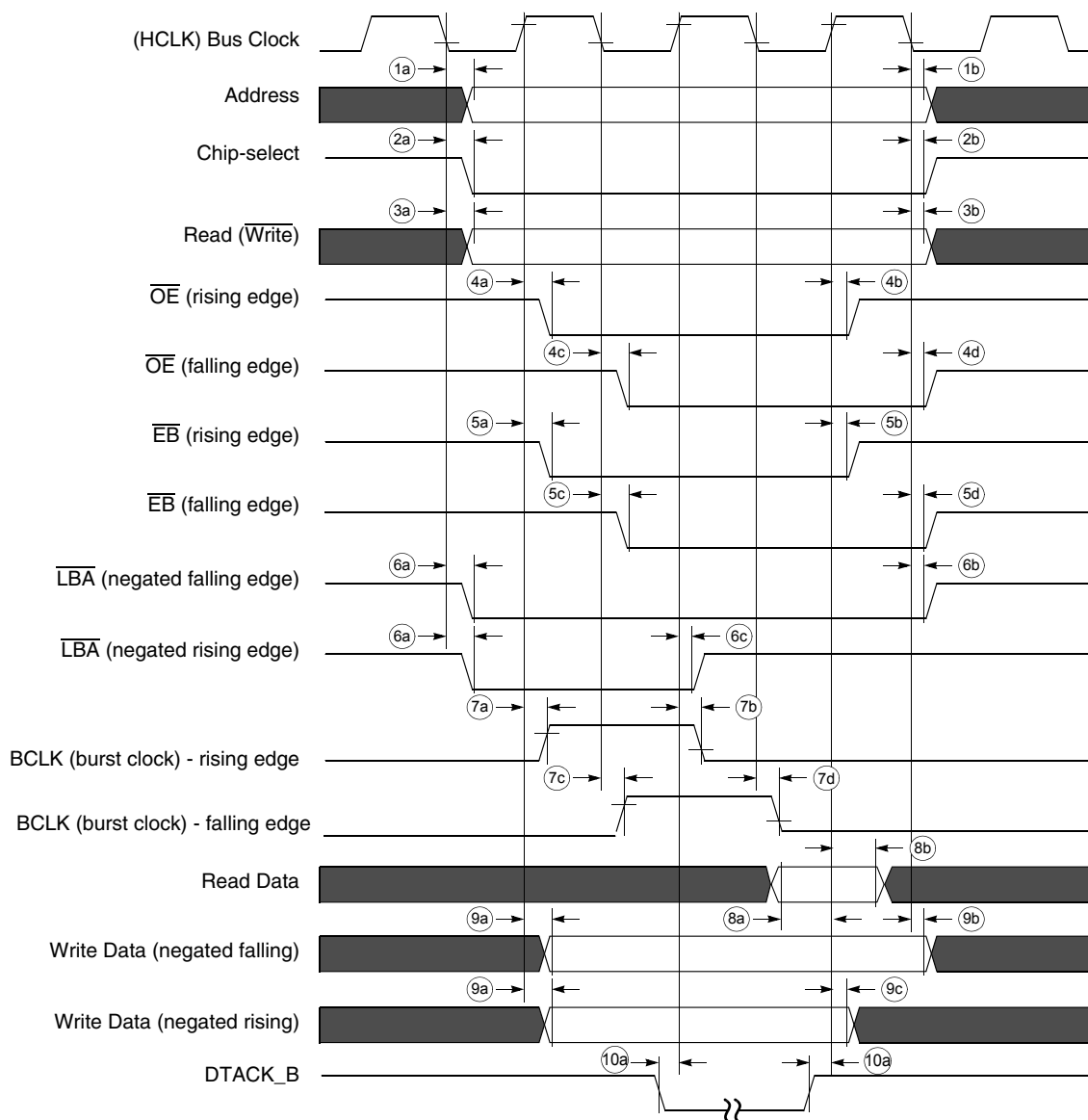


Figure 5. EIM Bus Timing Diagram

Table 12. EIM Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
1a	Clock fall to address valid	2.48	3.31	9.11	2.4	3.2	8.8	ns
1b	Clock fall to address invalid	1.55	2.48	5.69	1.5	2.4	5.5	ns
2a	Clock fall to chip-select valid	2.69	3.31	7.87	2.6	3.2	7.6	ns
2b	Clock fall to chip-select invalid	1.55	2.48	6.31	1.5	2.4	6.1	ns
3a	Clock fall to Read (Write) Valid	1.35	2.79	6.52	1.3	2.7	6.3	ns
3b	Clock fall to Read (Write) Invalid	1.86	2.59	6.11	1.8	2.5	5.9	ns

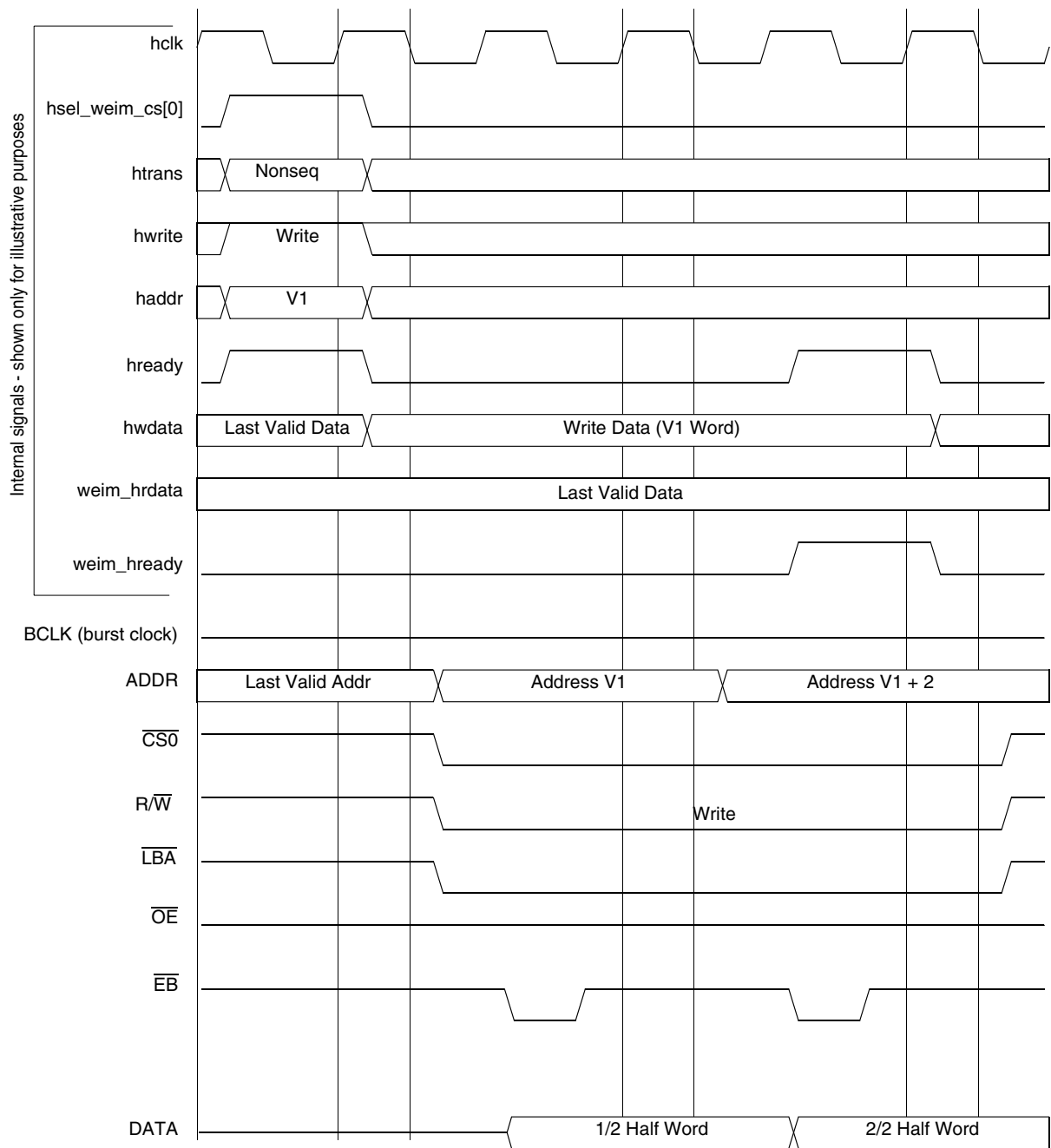


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF

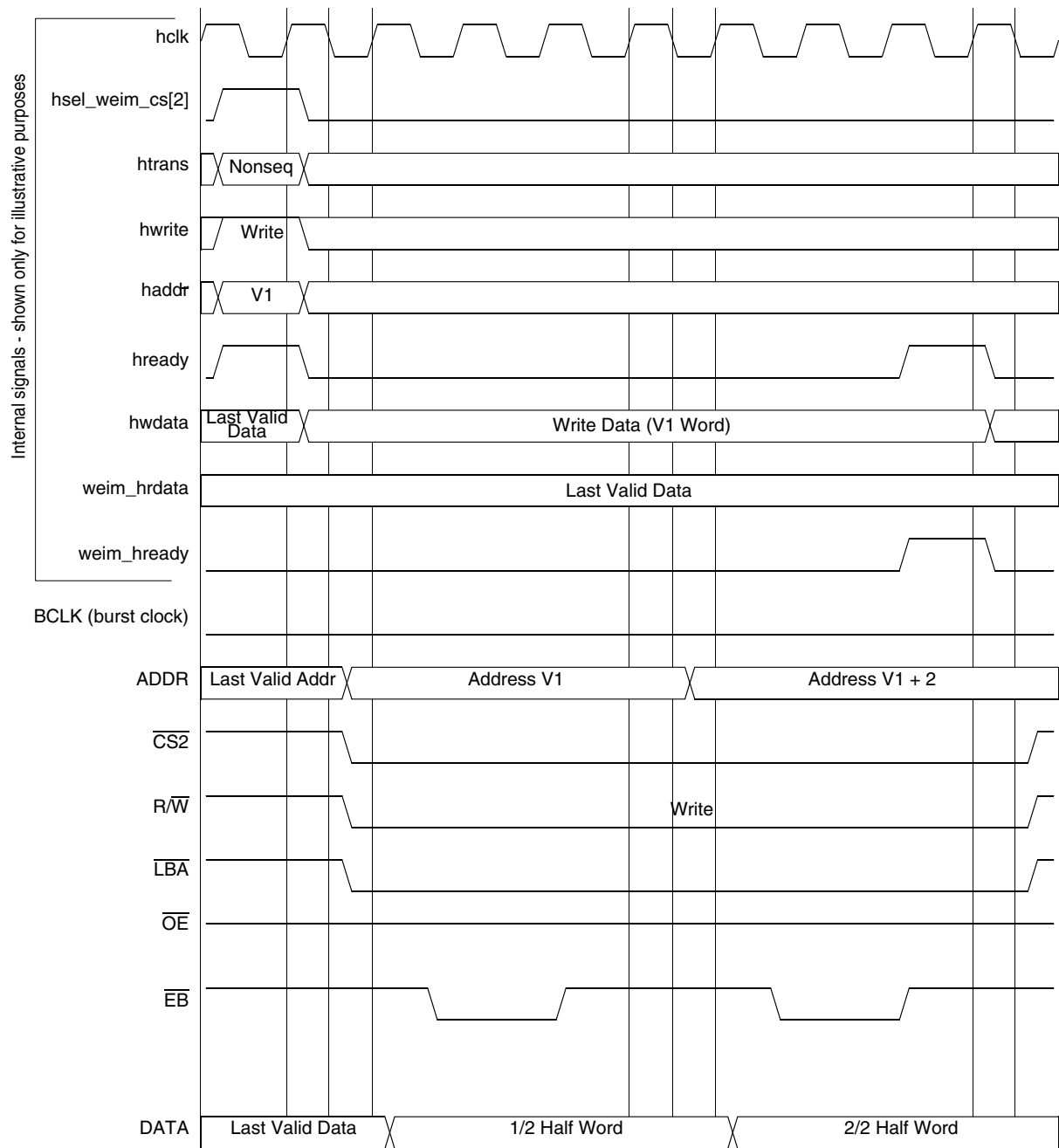
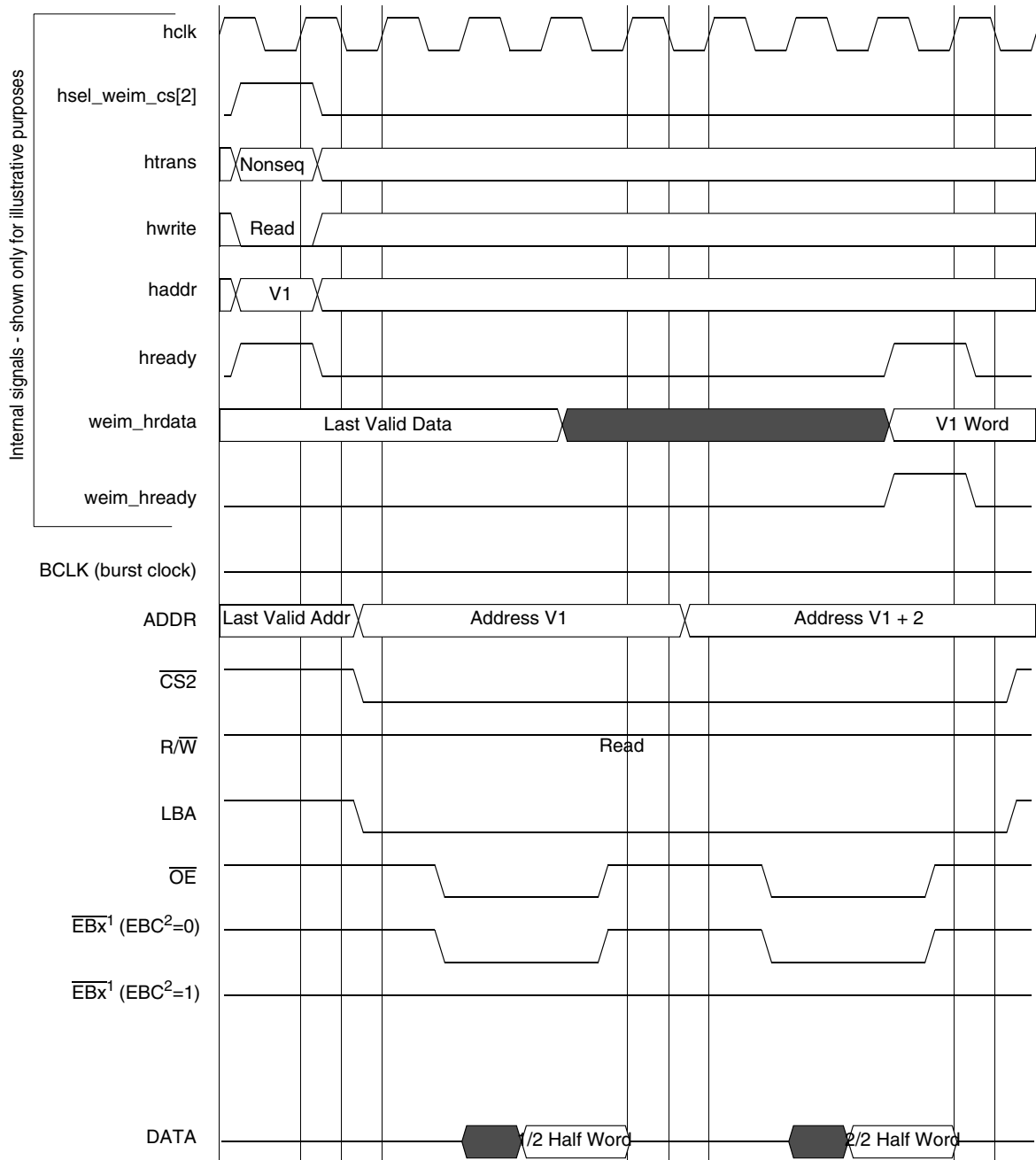


Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF

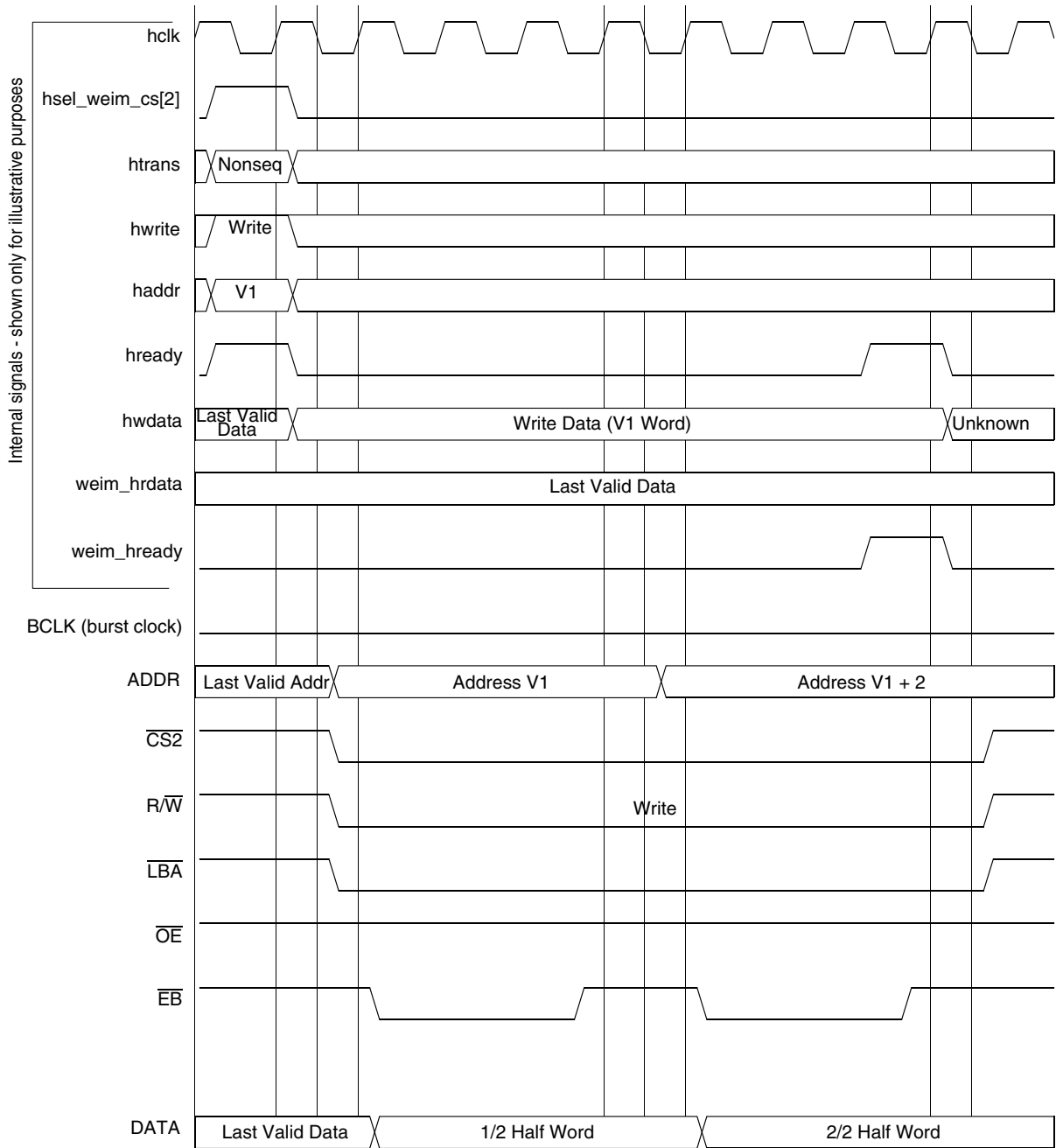


Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

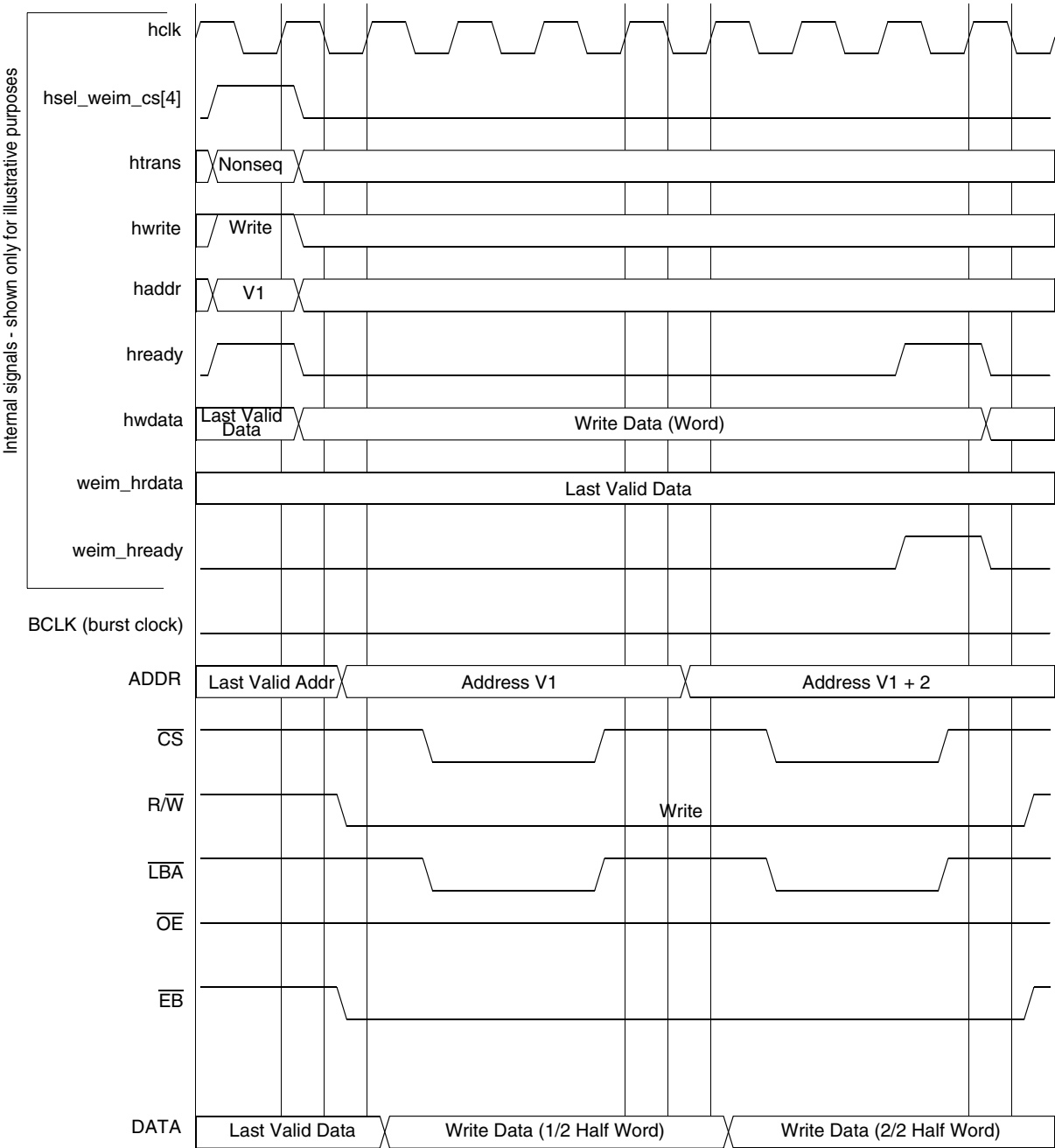
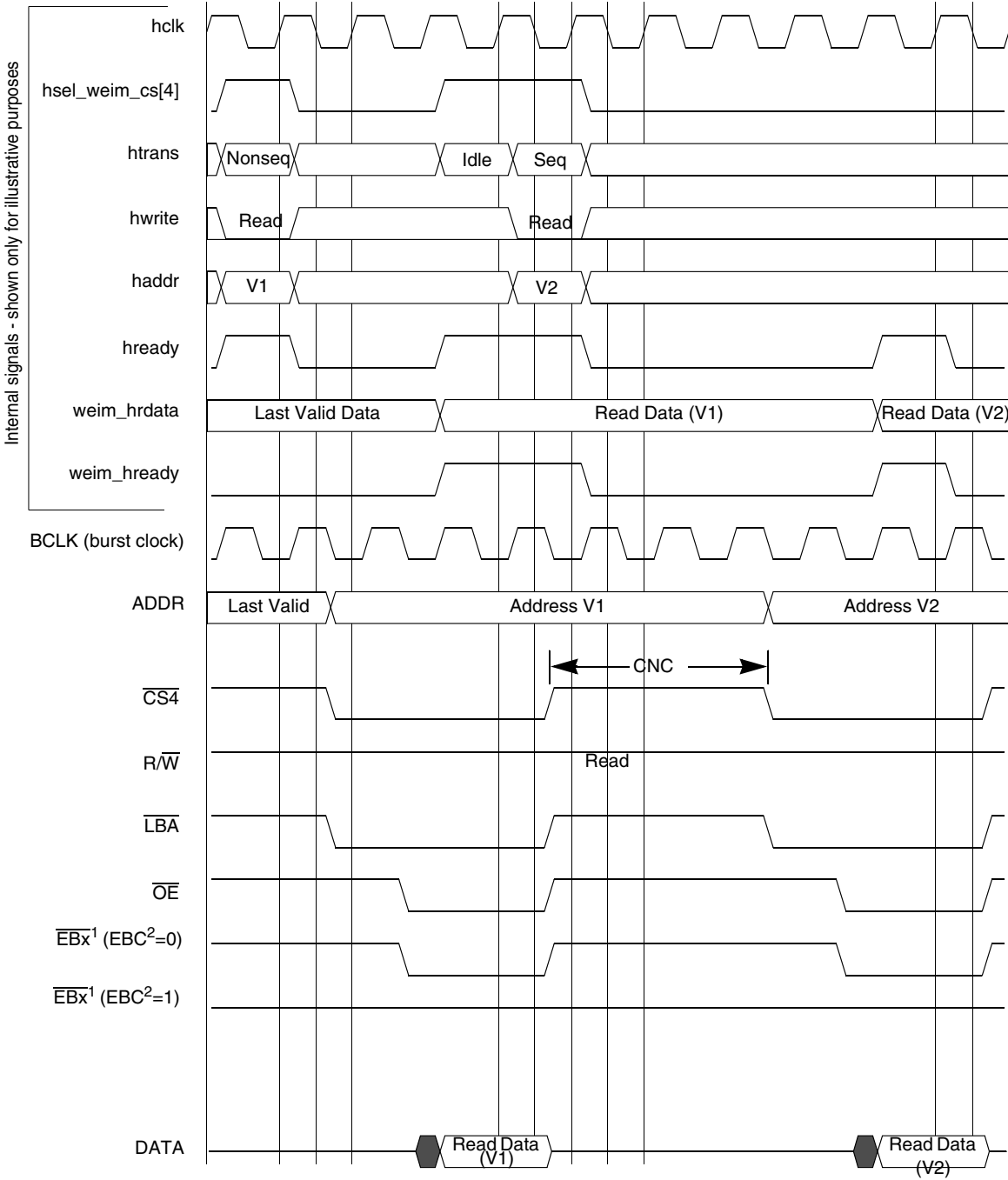


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF

4.4.4 Non-TFT Panel Timing

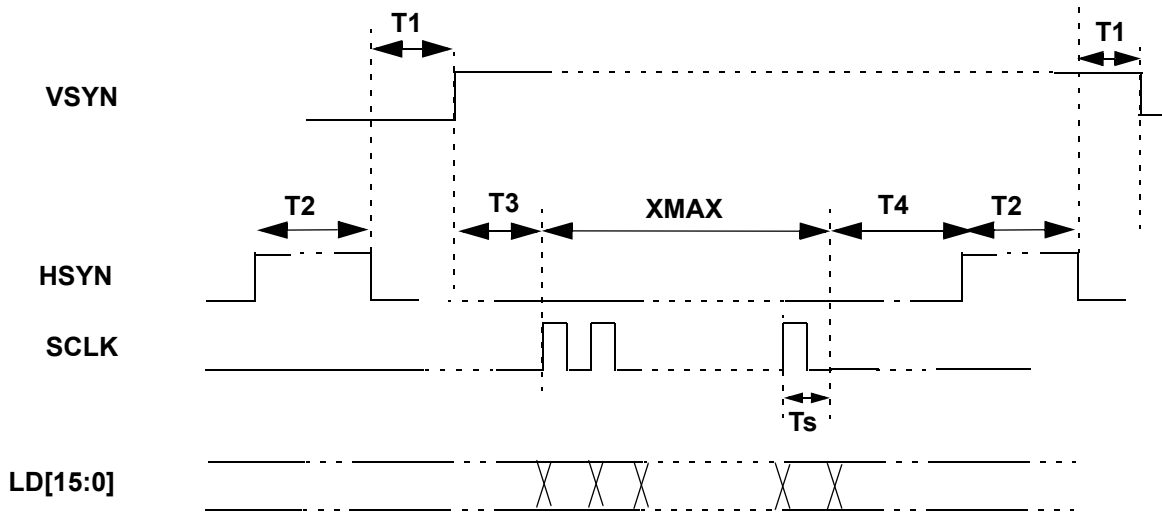


Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

Symbol	Parameter	Allowed Register Minimum Value ^{1, 2}	Actual Value	Unit
T1	HSYN to VSYN delay ³	0	HWAIT2+2	Tpix ⁴
T2	HSYN pulse width	0	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	$0 \leq T3 \leq Ts^5$	–
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

¹ Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.

² Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

³ VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.

⁴ Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).

⁵ Ts is the shift clock period. Ts = Tpix * (panel data bus width).

4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) and the SPI2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

Table 20. LCDC SCLK Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	SCLK to LD valid	–	2	ns

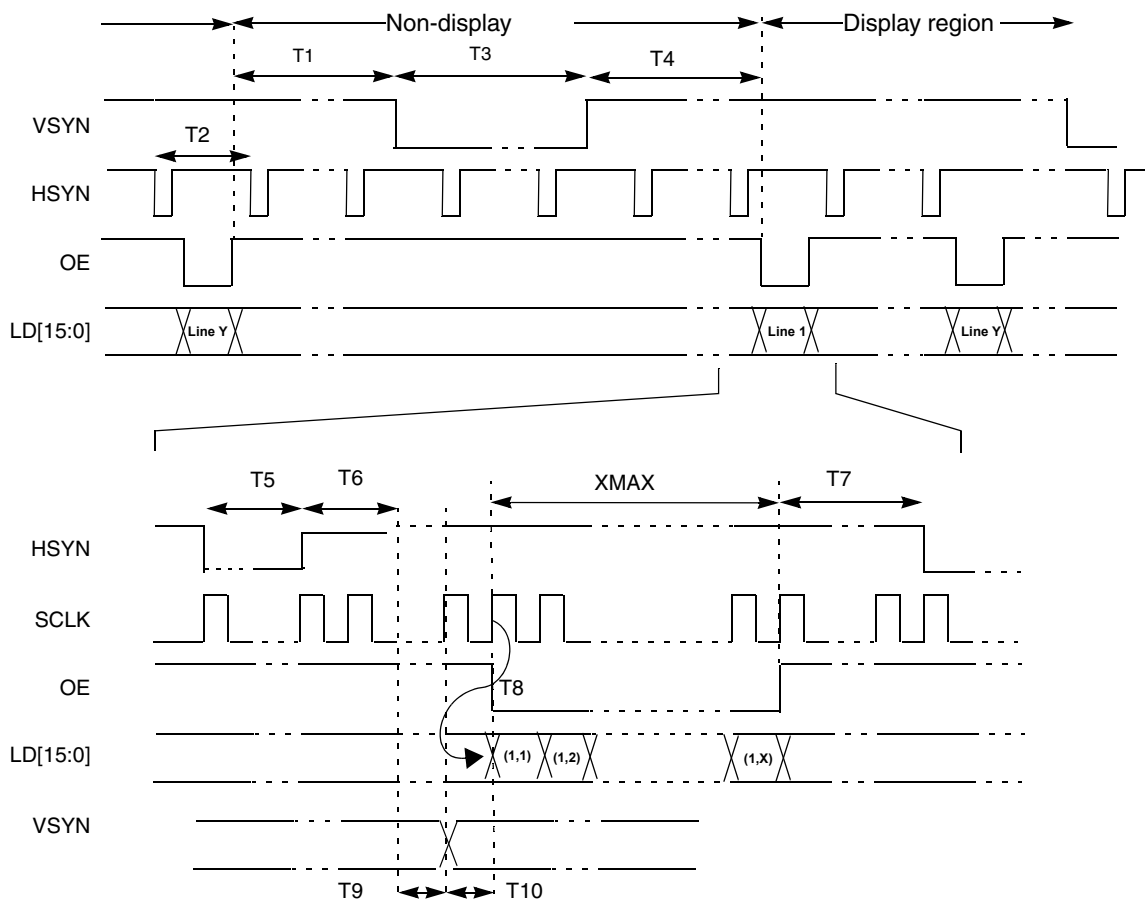


Figure 41. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Table 21. 4/8/16 Bit/Pixel TFT Color Mode Panel Timing

Symbol	Description	Minimum	Corresponding Register Value	Unit
T1	End of OE to beginning of VSYNC	$T5+T6+T7+T9$	$(VWAIT1 \cdot T2) + T5+T6+T7+T9$	Ts
T2	HSYN period	$XMAX+5$	$XMAX+T5+T6+T7+T9+T10$	Ts
T3	VSYNC pulse width	T2	$VWIDTH \cdot (T2)$	Ts
T4	End of VSYNC to beginning of OE	2	$VWAIT2 \cdot (T2)$	Ts
T5	HSYN pulse width	1	$HWIDTH+1$	Ts
T6	End of HSYN to beginning to T9	1	$HWAIT2+1$	Ts
T7	End of OE to beginning of HSYN	1	$HWAIT1+1$	Ts

Table 22. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP) ¹ —10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode ²	0	400	0	400	kHz
3a	Clock high time ¹ —10/30 cards	6/33	—	10/50	—	ns
3b	Clock low time ¹ —10/30 cards	15/75	—	10/50	—	ns
4a	Clock fall time ¹ —10/30 cards	—	10/50 (5.00) ³	—	10/50	ns
4b	Clock rise time ¹ —10/30 cards	—	14/67 (6.67) ³	—	10/50	ns
5a	Input hold time ³ —10/30 cards	10.3/10.3	—	9/9	—	ns
5b	Input setup time ³ —10/30 cards	10.3/10.3	—	9/9	—	ns
6a	Output hold time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
6b	Output setup time ³ —10/30 cards	5.7/5.7	—	5/5	—	ns
7	Output delay time ³	0	16	0	14	ns

¹ C_L ≤ 100 pF / 250 pF (10/30 cards)

² C_L ≤ 250 pF (21 cards)

³ C_L ≤ 25 pF (1 card)

4.7.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 43. The symbols for Figure 43 through Figure 47 are defined in Table 23.

Table 23. State Signal Parameters for Figure 43 through Figure 47

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)



Table 24. Timing Values for Figure 43 through Figure 47

MC9328MXL Technical Data, Rev. 8

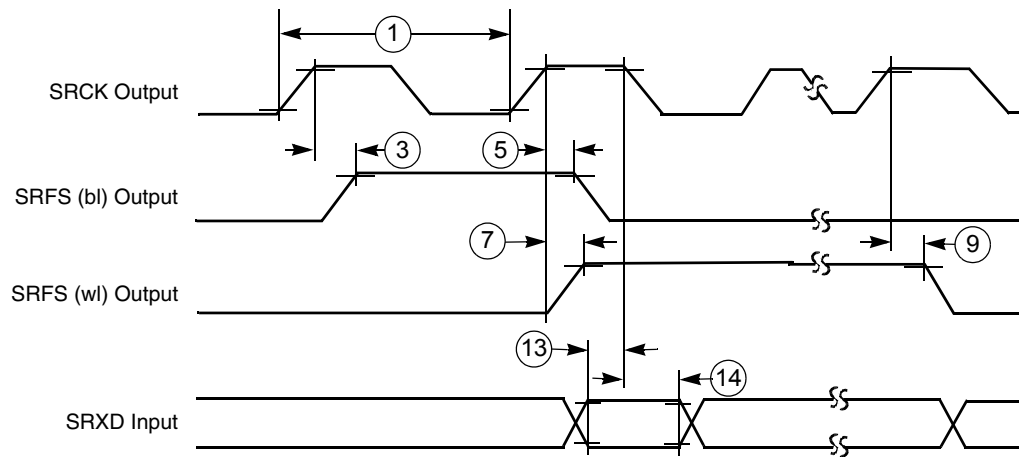
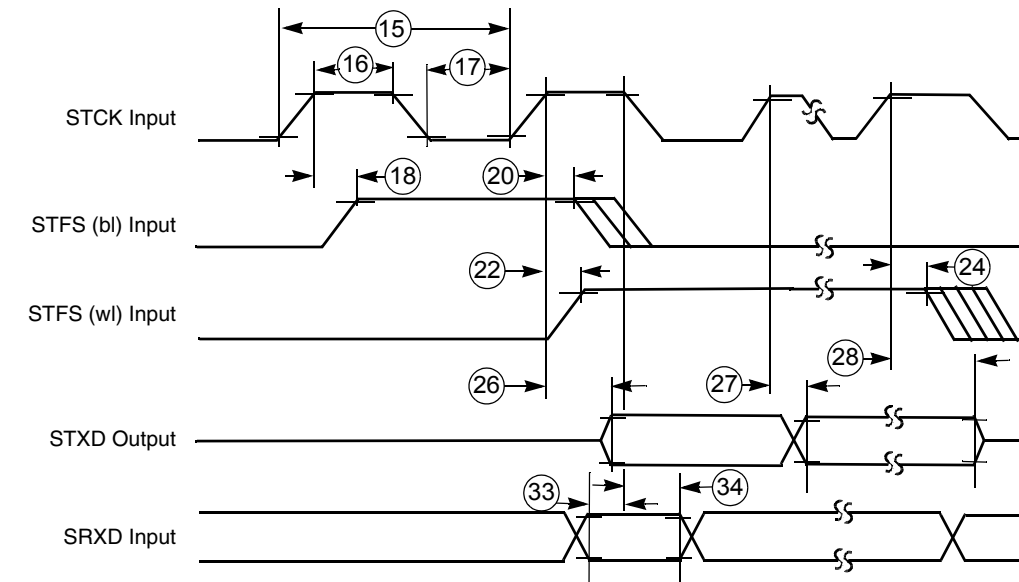


Figure 60. SSI Receiver Internal Clock Timing Diagram

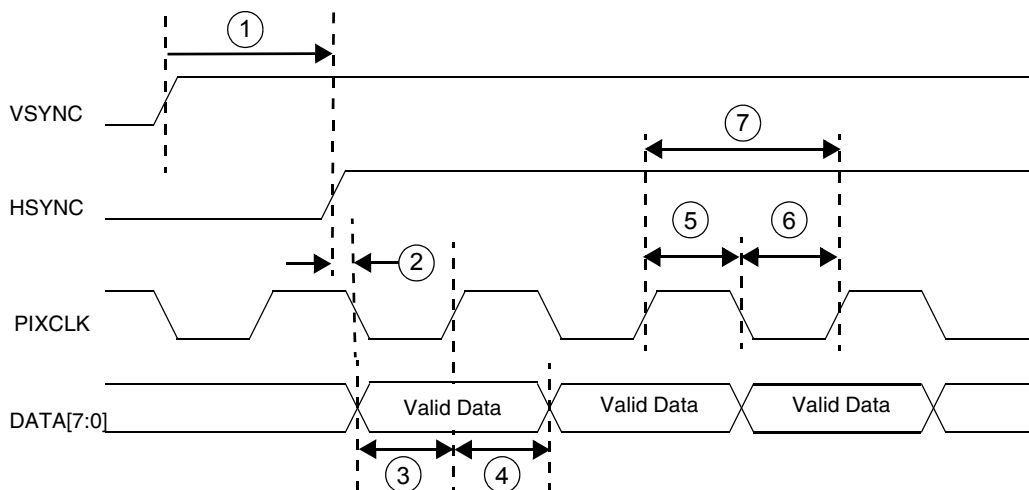


Note: SRXD Input in Synchronous mode only

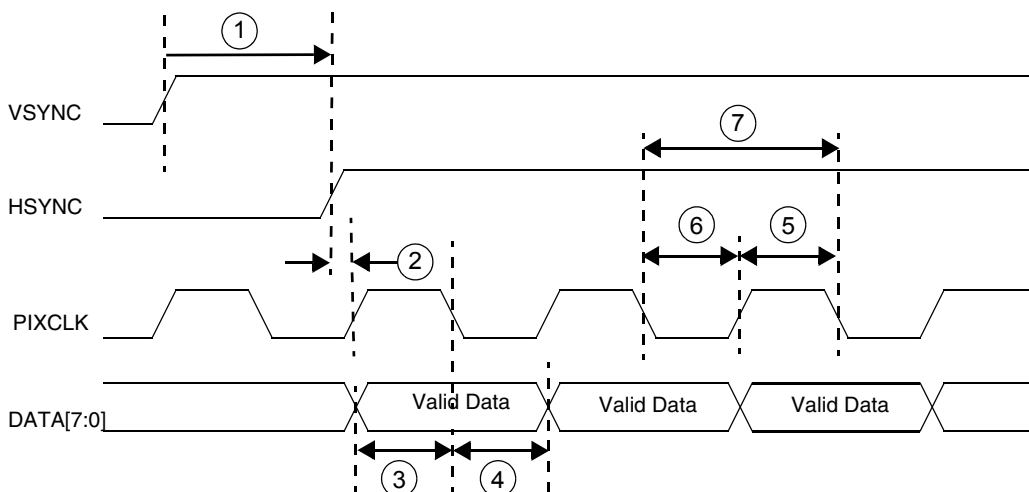
Figure 61. SSI Transmitter External Clock Timing Diagram

Table 34. SSI (Port B Alternate Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation ¹ (Port B Alternate Function ²)						
1	STCK/SRCK clock period ¹	95	–	83.3	–	ns
2	STCK high to STFS (bl) high ³	1.7	4.8	1.5	4.2	ns
3	SRCK high to SRFS (bl) high ³	-0.1	1.0	-0.1	1.0	ns
4	STCK high to STFS (bl) low ³	3.08	5.24	2.7	4.6	ns
5	SRCK high to SRFS (bl) low ³	1.25	2.28	1.1	2.0	ns
6	STCK high to STFS (wl) high ³	1.71	4.79	1.5	4.2	ns
7	SRCK high to SRFS (wl) high ³	-0.1	1.0	-0.1	1.0	ns
8	STCK high to STFS (wl) low ³	3.08	5.24	2.7	4.6	ns
9	SRCK high to SRFS (wl) low ³	1.25	2.28	1.1	2.0	ns
10	STCK high to STXD valid from high impedance	14.93	16.19	13.1	14.2	ns
11a	STCK high to STXD high	1.25	3.42	1.1	3.0	ns
11b	STCK high to STXD low	2.51	3.99	2.2	3.5	ns
12	STCK high to STXD high impedance	12.43	14.59	10.9	12.8	ns
13	SRXD setup time before SRCK low	20	–	17.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port B Alternate Function ²)						
15	STCK/SRCK clock period ¹	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns
18	STCK high to STFS (bl) high ³	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high ³	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low ³	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low ³	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high ³	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high ³	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low ³	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low ³	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.9	29.07	16.6	25.5	ns
27a	STCK high to STXD high	9.23	20.75	8.1	18.2	ns
27b	STCK high to STXD low	10.60	21.32	9.3	18.7	ns



**Figure 63. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**



**Figure 64. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 35. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

6 Product Documentation

6.1 Revision History

Table 39 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 39. i.MXL Data Sheet Revision History Rev. 8

Location	Revision
Table 2 on page 4 Signal Names and Descriptions	- Added the DMA_REQ signal to table. - Corrected signal name from <u>USBD_OE</u> to <u>USBD_ROE</u>
Table 3 on page 9 Signal Multiplex Table i.MXL	Added Signal Multiplex table from Reference Manual with the following changes: - Changed I/O Supply Voltage, PB31–20, from NVDD3 to NVDD4 - Added 225 BGA column. - Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 21	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 9	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at <http://www.freescale.com/imx>. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from <http://www.arm.com>.

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