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Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxldvm15

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
JTAG	
$\overline{\text{TRST}}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{\text{TDO}}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	
DMA_REQ	DMA Request—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{\text{ECB}}$, $\overline{\text{LBA}}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
UART1_RTS	Request to Send
UART1_CTS	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
UART2_RTS	Request to Send
UART2_CTS	Clear to Send
UART2_DSR	Data Set Ready
UART2_RI	Ring Indicator
UART2_DCD	Data Carrier Detect
UART2_DTR	Data Terminal Ready
Serial Audio Port – SSI (configurable to I²S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I²C	
I2C_SCL	I ² C Clock
I2C_SDA	I ² C Data

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
PWM	
PWMO	PWM Output
Test Function	
TRISTATE	Forces all I/O signals to high impedance for test purposes. For normal operation, terminate this input with a 1 k ohm resistor to ground. (TRI-STATE® is a registered trademark of National Semiconductor.)
Digital Supply Pins	
NVDD	Digital Supply for the I/O pins
NVSS	Digital Ground for the I/O pins
Supply Pins – Analog Modules	
AVDD	Supply for analog blocks
Internal Power Supply	
QVDD	Power supply pins for silicon internal circuitry
QVSS	Ground pins for silicon internal circuitry

2.1 I/O Pads Power Supply and Signal Multiplexing Scheme

This section describes detailed information about both the power supply for each I/O pin and its function multiplexing scheme. The user can reference information provided in [Table 6 on page 18](#) to configure the power supply scheme for each device in the system (memory and external peripherals). The function multiplexing information also shown in [Table 6](#) allows the user to select the function of each pin by configuring the appropriate GPIO registers when those pins are multiplexed to provide different functions.

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	D2	B1	A24	O		ETMTRAC ESYNC	O	PA0	69K	SPI2_ SCLK			A24
NVDD1	C1	C2	D31	I/O	69K								
NVDD1	D1	C1	A23	O		ETMTRAC ECLK	O	PA31	69K				A23
NVDD1	E3	D2	D30	I/O	69K								
NVDD1	E2	D1	A22	O		ETMPIPE STAT2	O	PA30	69K				A22
NVDD1	E4	D3	D29	I/O	69K								
NVDD1	E1	E2	A21	O		ETMPIPE STAT1	O	PA29	69K				A21
NVDD1	F3	E3	D28	I/O	69K								

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	F1	E1	A20	O		ETMPIPE STAT0	O	PA28	69K				A20
NVDD1	F4	F2	D27	I/O	69K								
NVDD1	F2	F4	A19	O		ETMTRAC EPKT3	O	PA27	69K				A19
NVDD1	G3	E4	D26	I/O	69K								
NVDD1	G2	F1	A18	O		ETMTRAC EPKT2	O	PA26	69K				A18
NVDD1	G4	F3	D25	I/O	69K								
NVDD1	G1	G2	A17	O		ETMTRAC EPKT1	O	PA25	69K				A17
NVDD1	H4	G3	D24	I/O	69K								
NVDD1	H2	F5	A16	O		ETMTRAC EPKT0	O	PA24	69K				A16
NVDD1	H3	G4	D23	I/O	69K								
NVDD1	H1	G1	A15	O									
NVDD1	H5	H2	D22	I/O	69K								
NVDD1	J1	H3	A14	O									
NVDD1	J3	G5	D21	I/O	69K								
NVDD1	K1	H1	A13	O									
NVDD1	J4	H4	D20	I/O	69K								
NVDD1	J2	J1	A12	O									
NVDD1	K4	J4	D19	I/O	69K								
NVDD1	K2	J2	A11	O									
NVDD1	L4	J3	D18	I/O	69K								
NVDD1	L1	K1	A10	O									
NVDD1	L3	K4	D17	I/O	69K								
NVDD1	L2	K3	A9	O									
NVDD1	M1	K2	D16	I/O	69K								
NVDD1	N1	L1	A8	O									
NVDD1	M2	L4	D15	I/O	69K								
NVDD1	N2	L2	A7	O									
NVDD1	P1	L5	D14	I/O	69K								
NVDD1	R1	M4	A6	O									
NVDD1	M3	L3	D13	I/O	69K								
NVDD1	P2	M1	A5	O									
NVDD1	N3	M2	D12	I/O	69K								
NVDD1	P3	N1	A4	O									
NVDD1	R2	M3	D11	I/O	69K								

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	F5	J5	NVDD	Static									
	J6	K6	NVSS	Static									
NVDD1	G5	K5	NVDD1	Static									
	K6	M6	NVSS	Static									
NVDD1	J5	H6	NVDD1	Static									
	H7	J7	NVSS	Static									
NVDD1	K5	L6	NVDD1	Static									
	J7	J7	NVSS	Static									
NVDD1	L5	L6	NVDD1	Static									
	G8	K7	NVSS	Static									
NVDD1	L5	J8	NVDD1	Static									
	H8	L7	NVSS	Static									
	K7	T16	QVSS	Static									
NVDD2	H10	K10	NVDD2	Static									
	G9	J10	NVSS	Static									
QVDD3	F11	J15	QVDD3	Static									
	G10	J16	QVSS	Static									
NVDD2	C15	K9	NVDD2	Static									
	H9	J9	NVSS	Static									
QVDD4	D7	A13	QVDD4	Static									
	L13	B13	QVSS	Static									
NVDD3	D9	A10	NVDD3	Static									
	J9	A7	NVSS	Static									
	K9	A4	NVSS	Static									
NVDD4	G7	A6	NVDD4	Static									
NVDD1	F6		NVDD1	Static									
NVDD1	L6		NVDD1	Static									
NVDD1	M6		NVDD1	Static									
NVDD1	K8		NVDD1	Static									
	L10		NVSS	Static									
	L11		NVSS	Static									
	M11		NVSS	Static									

- ¹ Pull down this input with 1K Ω resistor to GND.
- ² External circuit required to drive this input.
- ³ Tie this input high (to AVDD) or pull down with 1K Ω resistor to GND.
- ⁴ Pull up this output with a resistor to NVDD2.

4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in [Figure 3](#) and [Figure 4](#).

NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

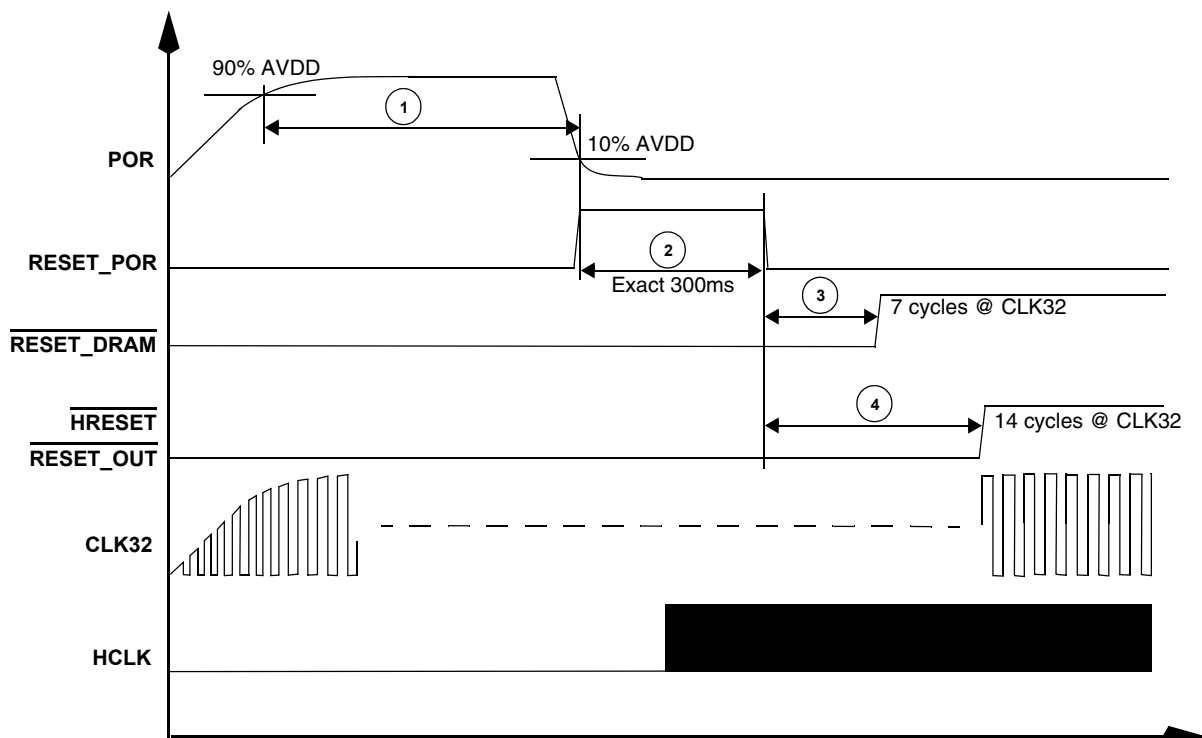


Figure 3. Timing Relationship with POR

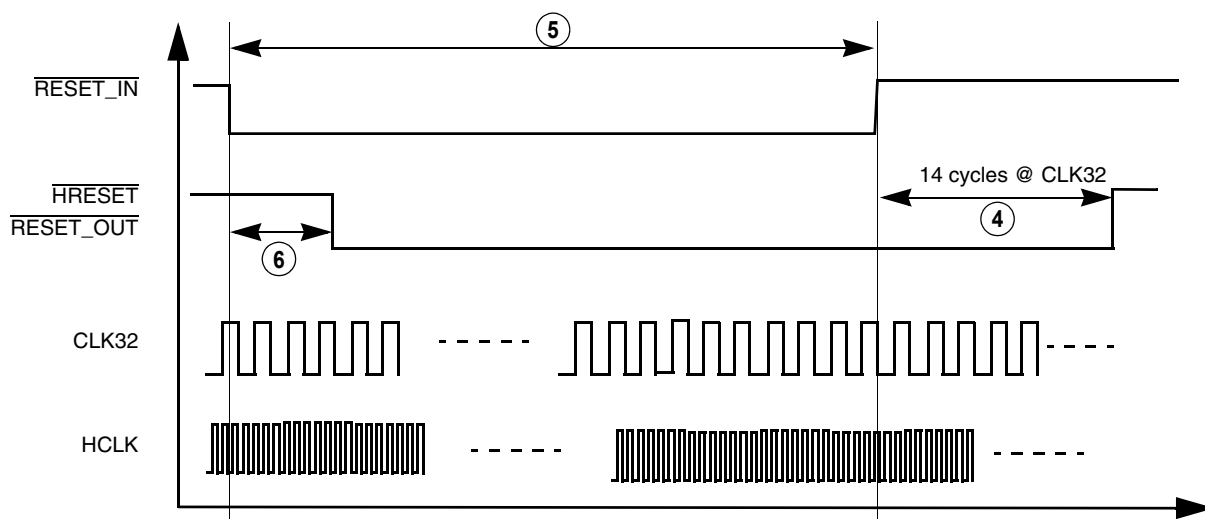


Figure 4. Timing Relationship with RESET_IN

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
4a	Clock ¹ rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock ¹ rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock ¹ fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock ¹ fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock ¹ rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock ¹ rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock ¹ fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock ¹ fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock ¹ fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock ¹ fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock ¹ rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock ¹ rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock ¹ rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock ¹ fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock ¹ fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock ¹ rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock ¹ fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock ¹ rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

¹ Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

4.4.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

4.4.2.2 WAIT Read Cycle DMA Enabled

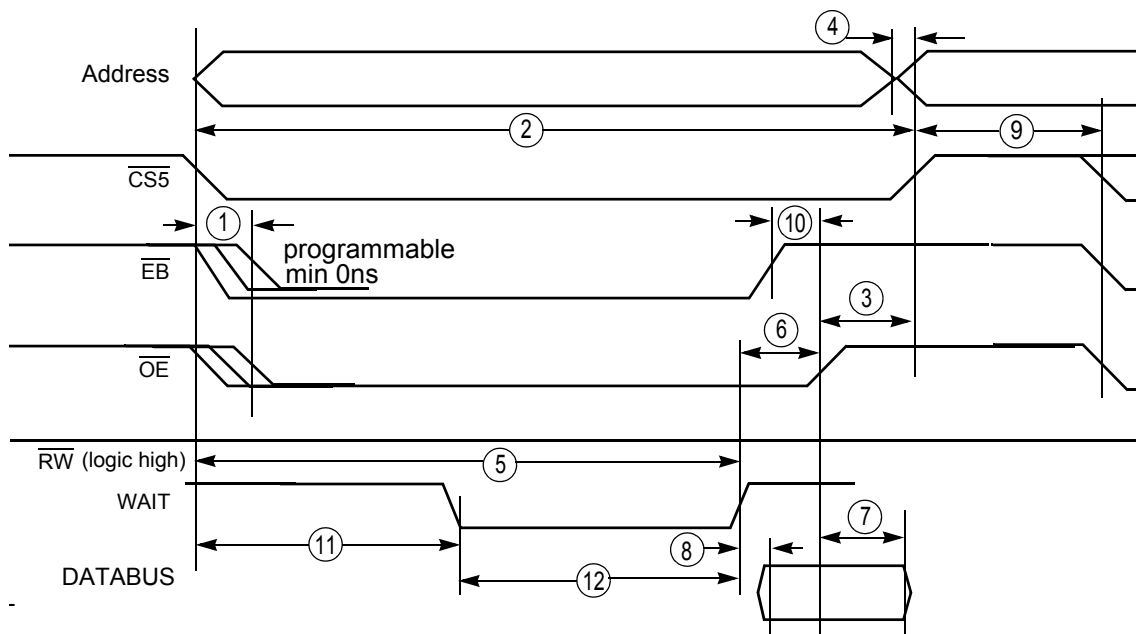
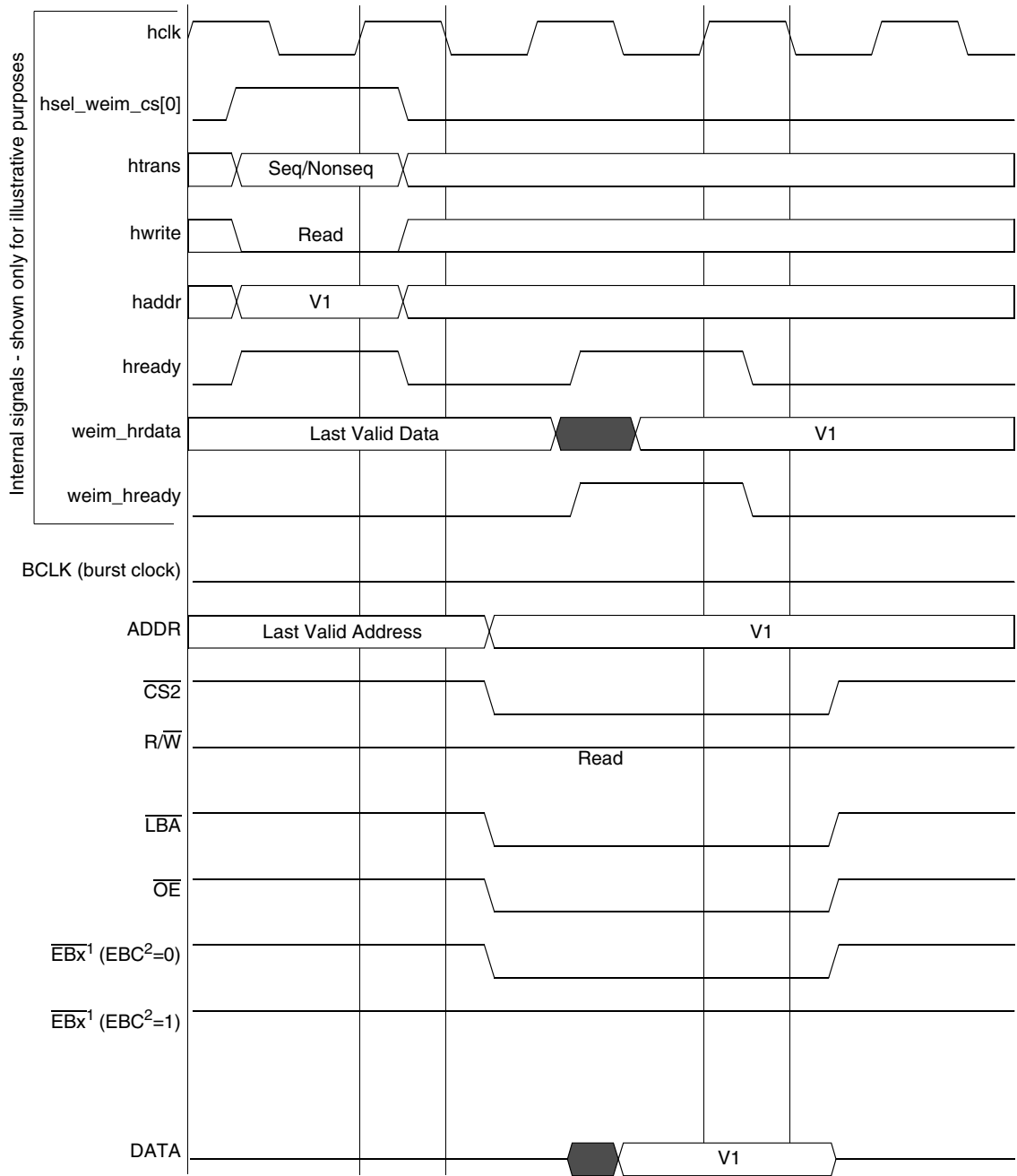


Figure 7. DTACK WAIT Read Cycle DMA Enabled

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	1.5T-0.68	1.5T-0.06	ns
4	Address inactivated before $\overline{CS}$ negated	–	0.05	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
7	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
8	Data ready after wait is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
10	OE negate after EB negate	0.06	0.18	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF

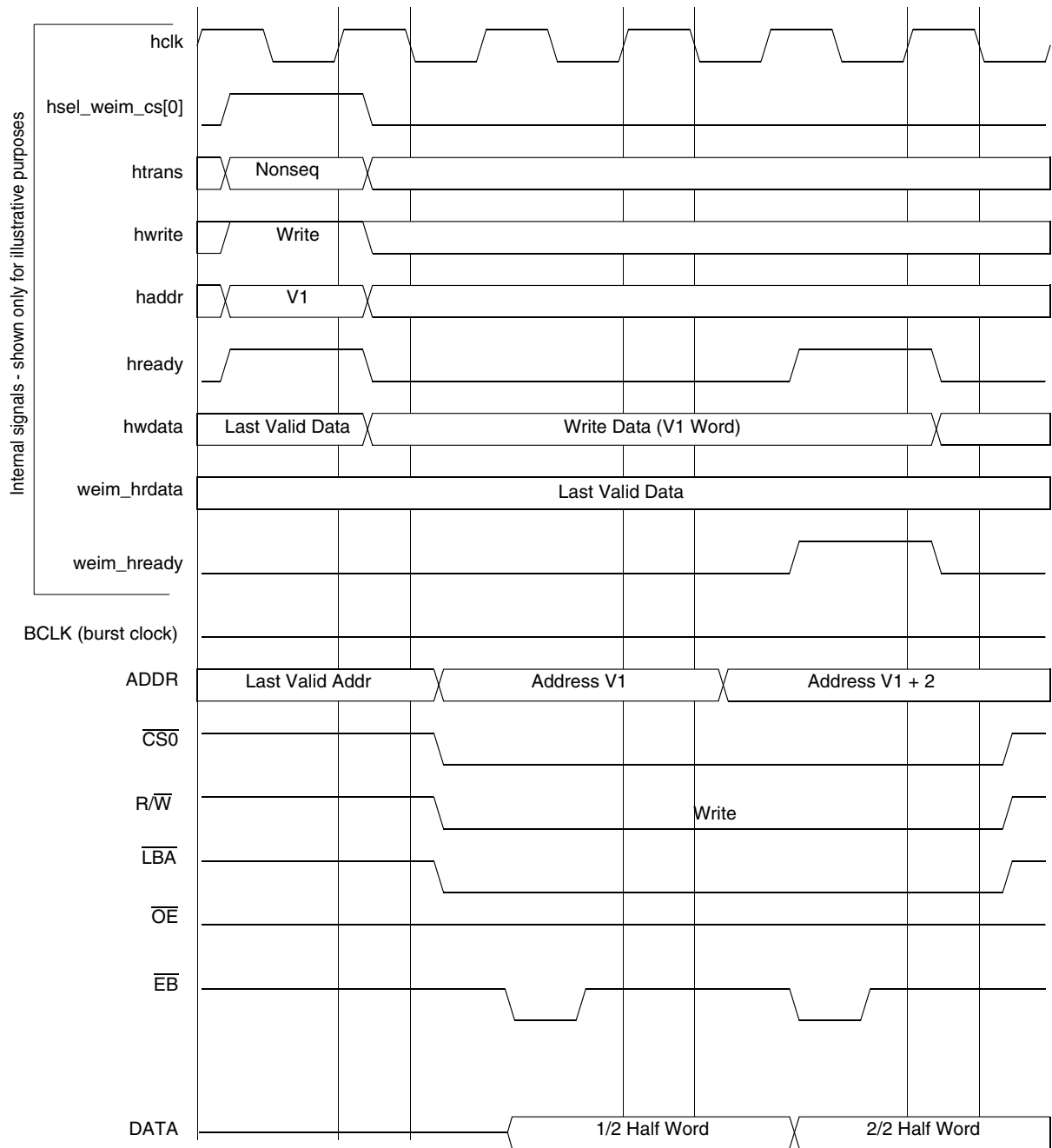
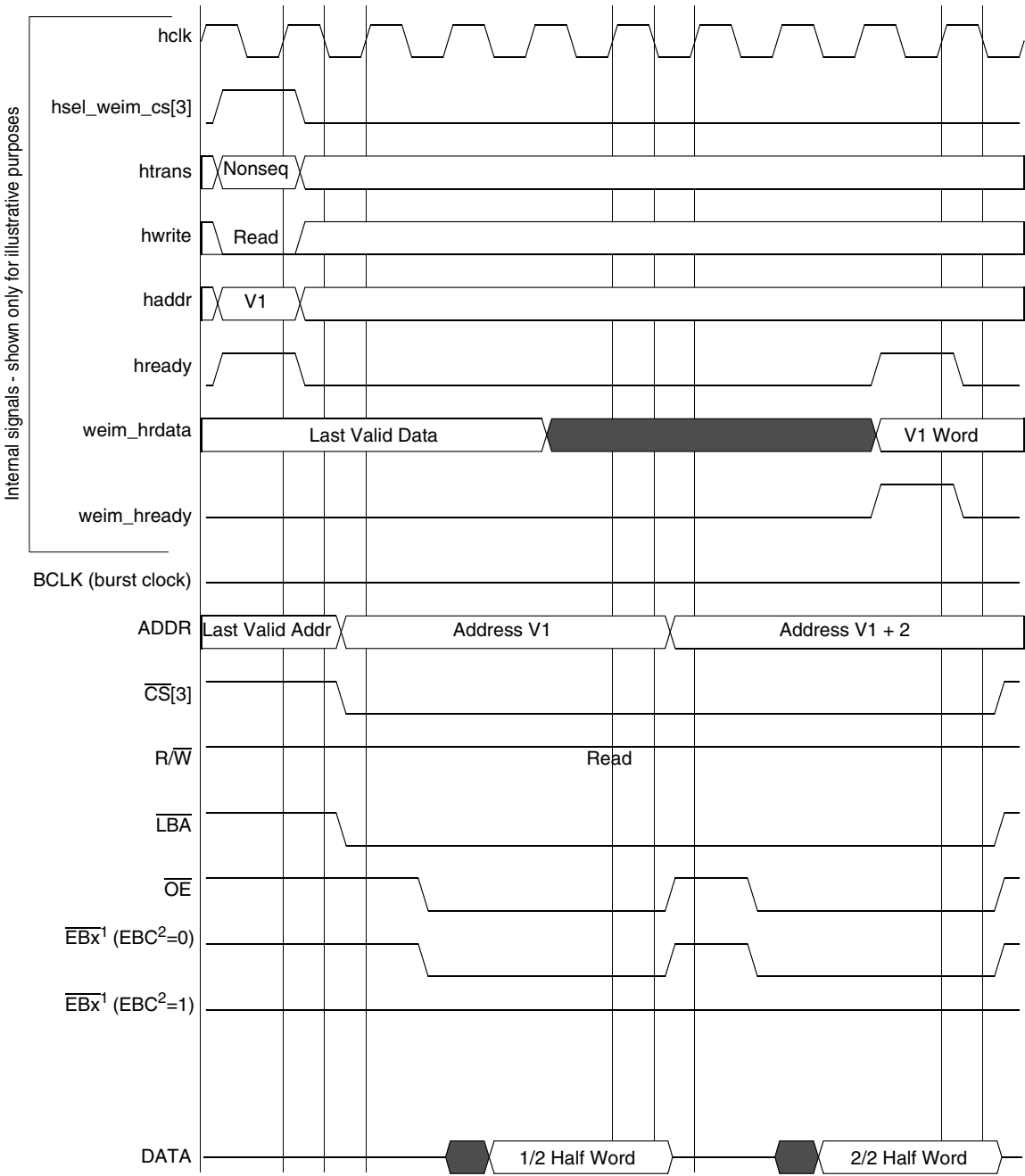


Figure 13. WSC = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF

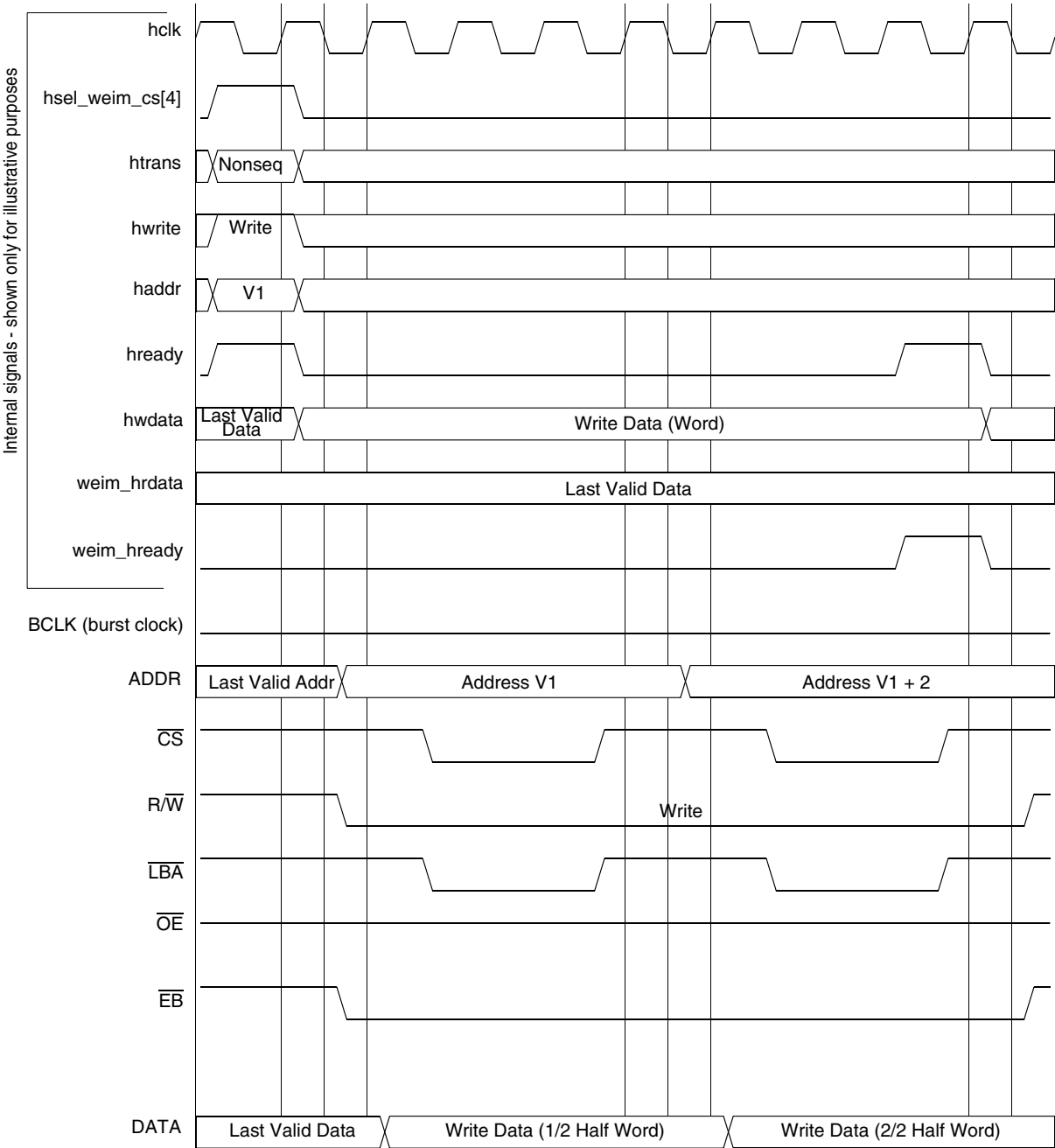
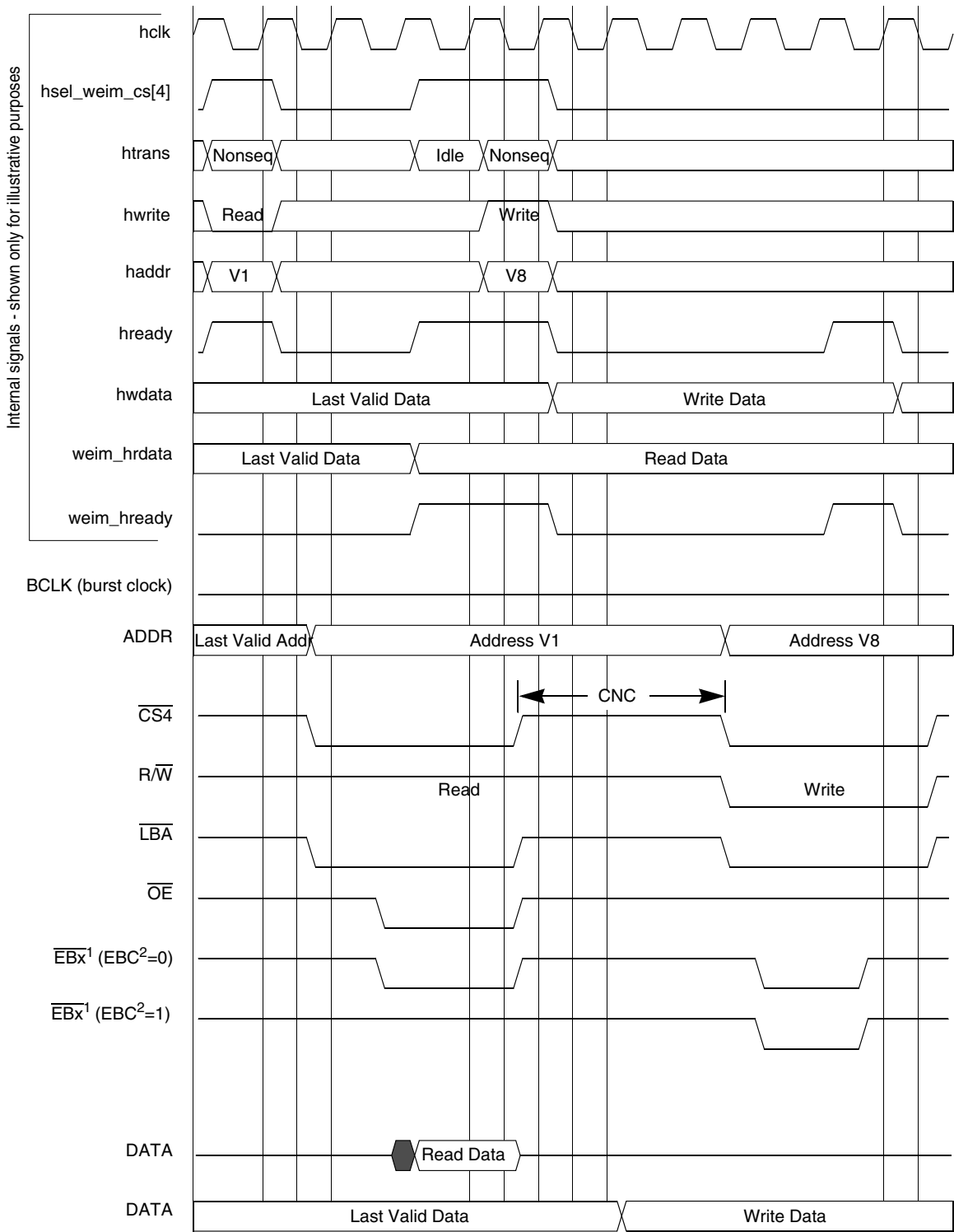


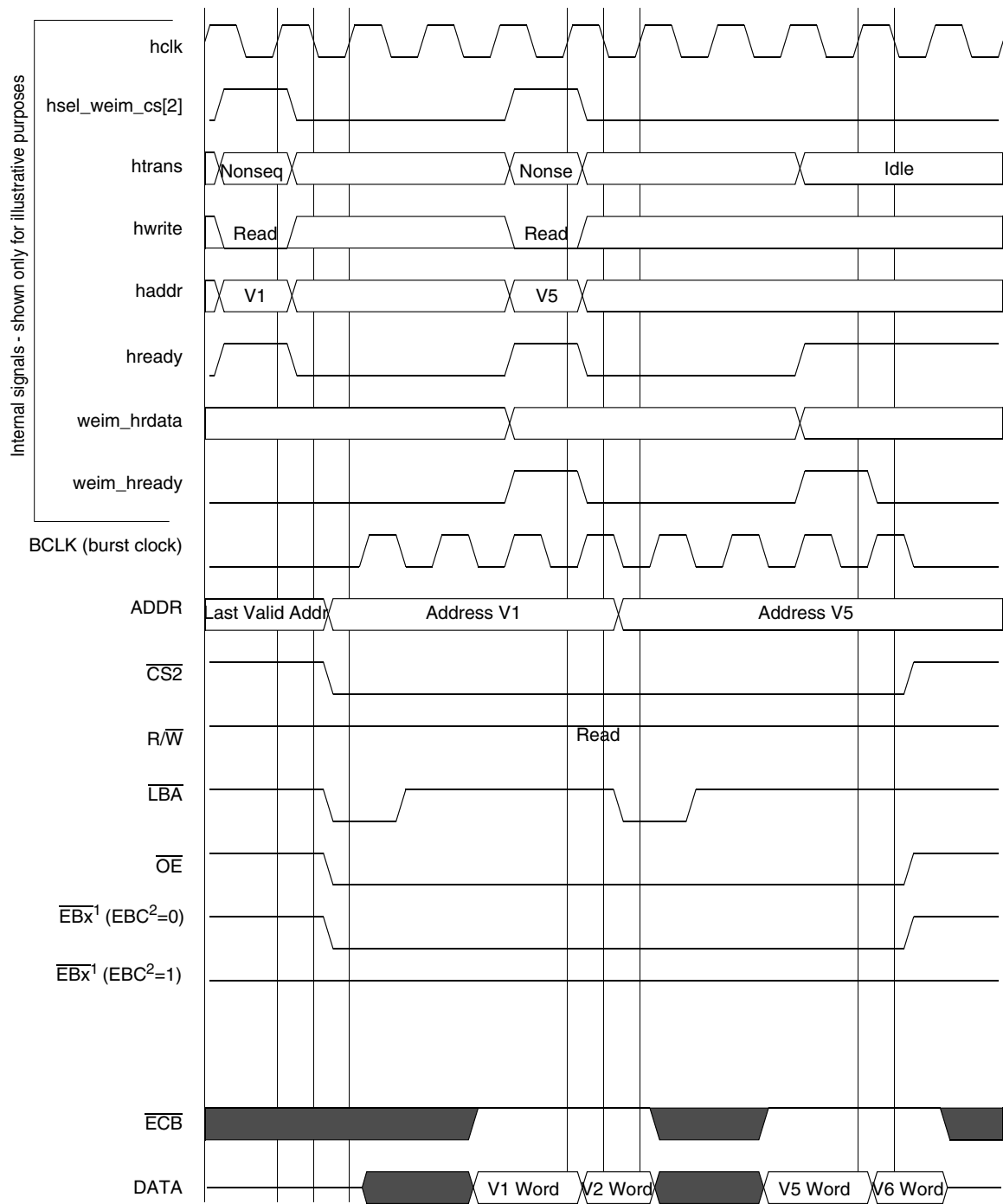
Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3

Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
 Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF

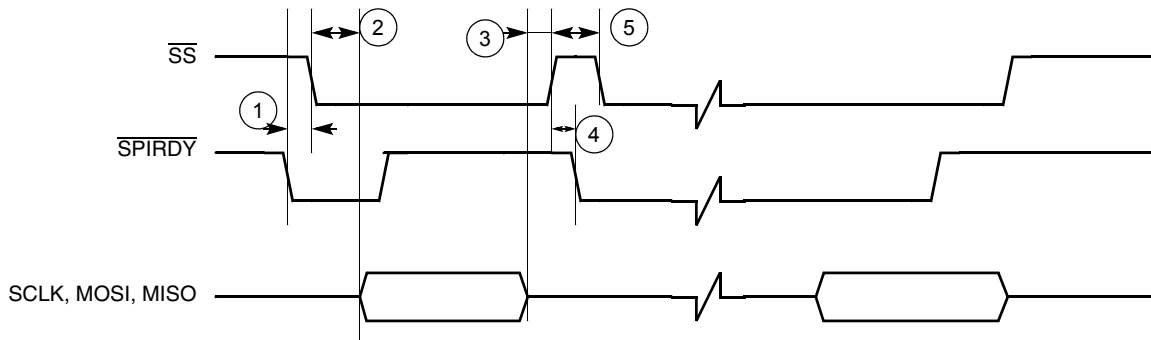


Figure 34. Master SPI Timing Diagram Using $\overline{\text{SPI_RDY}}$ Edge Trigger

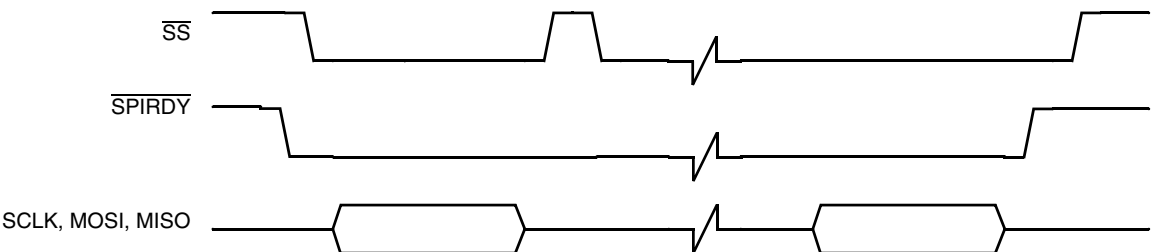


Figure 35. Master SPI Timing Diagram Using $\overline{\text{SPI_RDY}}$ Level Trigger

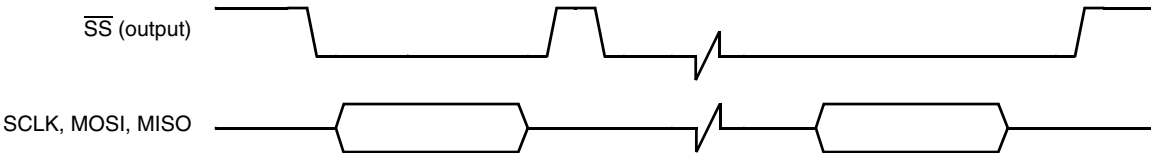


Figure 36. Master SPI Timing Diagram Ignore $\overline{\text{SPI_RDY}}$ Level Trigger

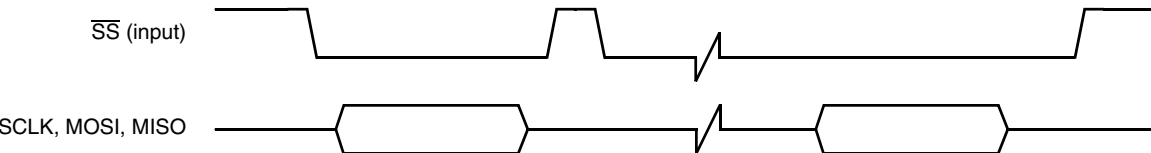


Figure 37. Slave SPI Timing Diagram FIFO Advanced by BIT COUNT

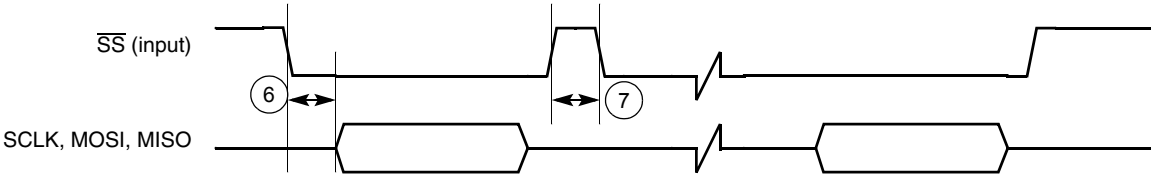


Figure 38. Slave SPI Timing Diagram FIFO Advanced by $\overline{\text{SS}}$ Rising Edge

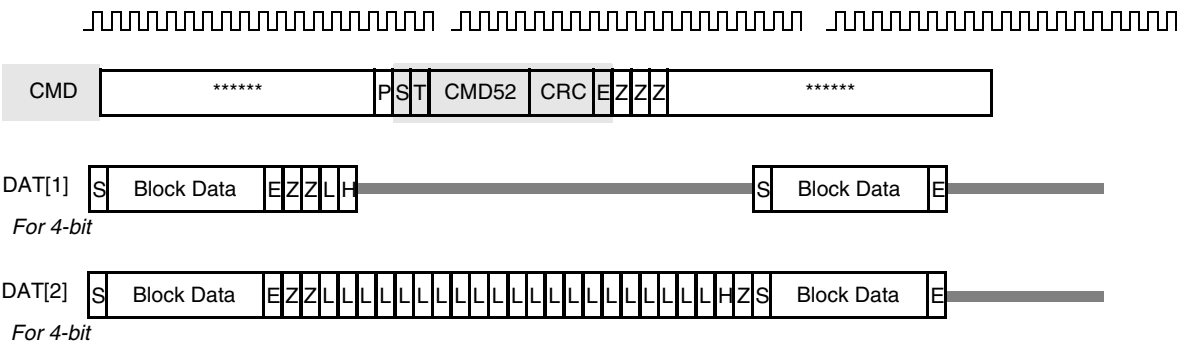


Figure 49. SDIO ReadWait Timing Diagram

4.8 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

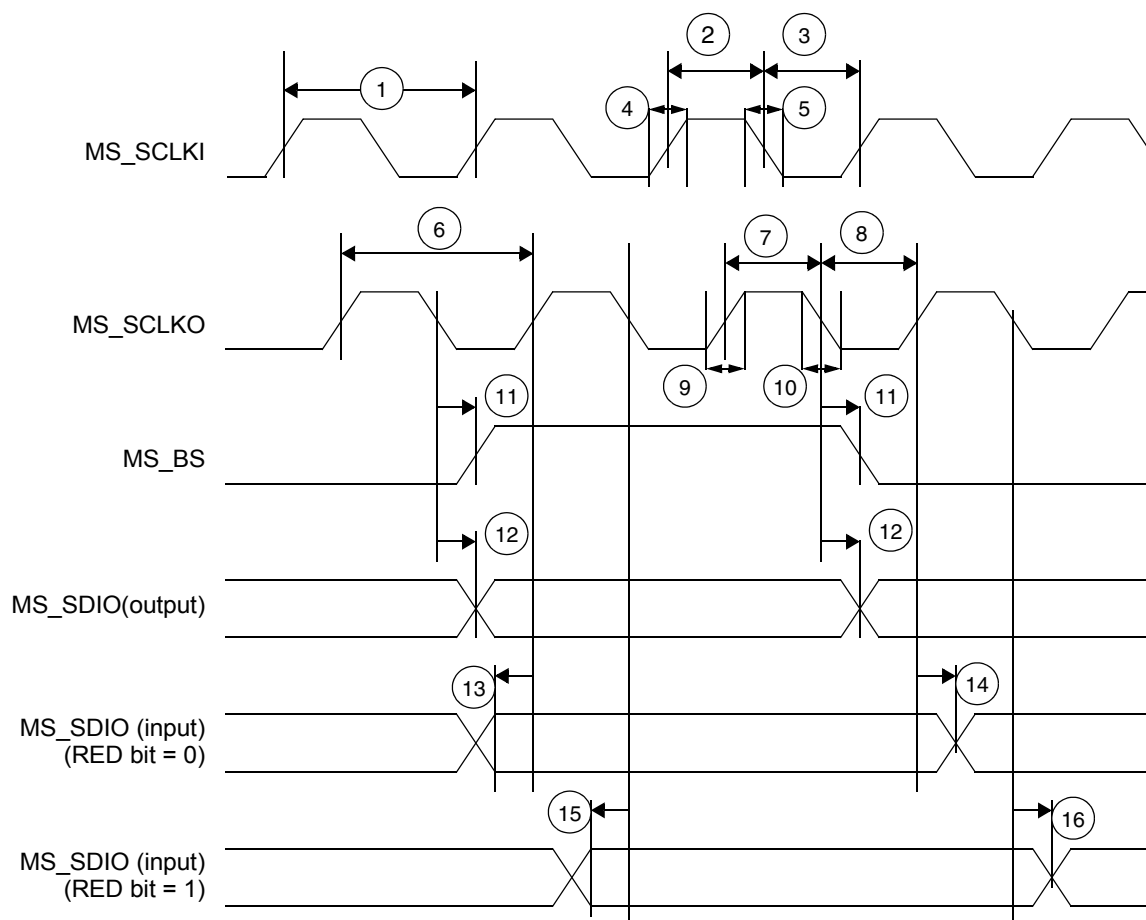


Figure 50. MSHC Signal Timing Diagram

Table 25. MSHC Signal Timing Parameter Table

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	MS_SCLKI frequency	–	25	MHz
2	MS_SCLKI high pulse width	20	–	ns
3	MS_SCLKI low pulse width	20	–	ns
4	MS_SCLKI rise time	–	3	ns
5	MS_SCLKI fall time	–	3	ns
6	MS_SCLKO frequency ¹	–	25	MHz
7	MS_SCLKO high pulse width ¹	20	–	ns
8	MS_SCLKO low pulse width ¹	15	–	ns
9	MS_SCLKO rise time ¹	–	5	ns
10	MS_SCLKO fall time ¹	–	5	ns
11	MS_BS delay time ¹	–	3	ns

Table 25. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	MS_SDIO output delay time ^{1,2}	–	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0) ³	18	–	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0) ³	0	–	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1) ⁴	23	–	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1) ⁴	0	–	ns

¹ Loading capacitor condition is less than or equal to 30pF.

² An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.

³ If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.

⁴ If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

4.9 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 51 and the parameters are listed in Table 26.

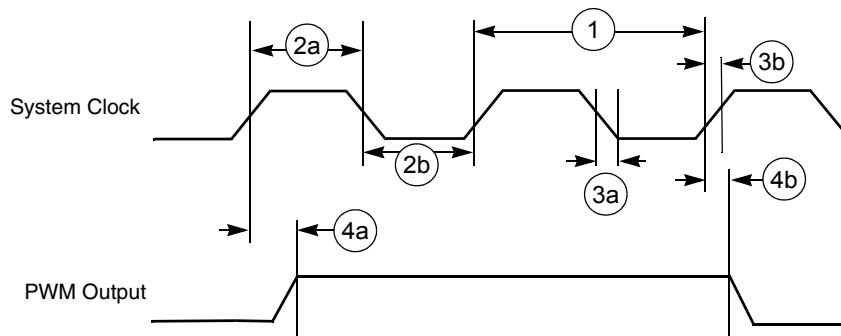


Figure 51. PWM Output Timing Diagram

Table 26. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency ¹	0	87	0	100	MHz
2a	Clock high time ¹	3.3	–	5/10	–	ns
2b	Clock low time ¹	7.5	–	5/10	–	ns
3a	Clock fall time ¹	–	5	–	5/10	ns

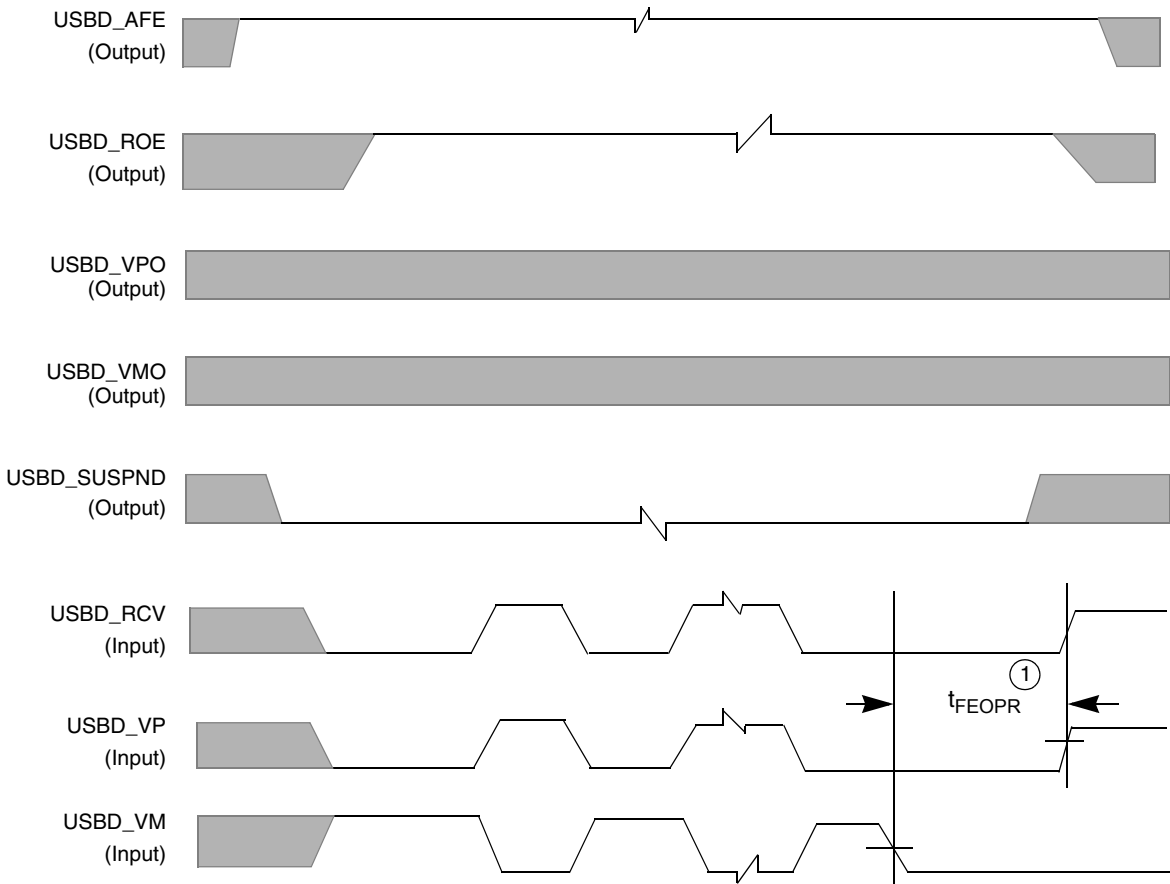


Figure 57. USB Device Timing Diagram for Data Transfer from USB Transceiver (RX)

Table 31. USB Device Timing Parameter Table for Data Transfer from USB Transceiver (RX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{FEOPR} ; Receiver SE0 interval of EOP	82	—	ns

4.12 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

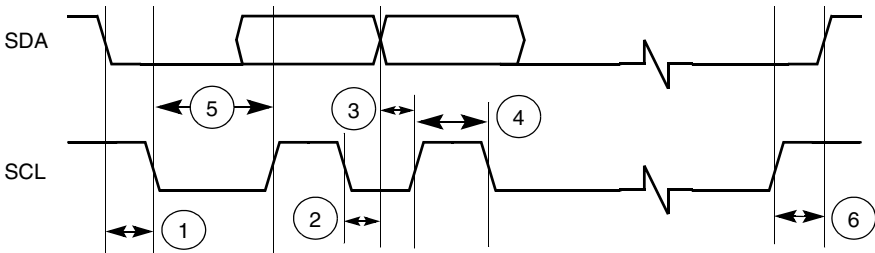


Figure 58. Definition of Bus Timing for I²C

6 Product Documentation

6.1 Revision History

Table 39 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 39. i.MXL Data Sheet Revision History Rev. 8

Location	Revision
Table 2 on page 4 Signal Names and Descriptions	- Added the DMA_REQ signal to table. - Corrected signal name from <u>USBD_OE</u> to <u>USBD_ROE</u>
Table 3 on page 9 Signal Multiplex Table i.MXL	Added Signal Multiplex table from Reference Manual with the following changes: - Changed I/O Supply Voltage, PB31–20, from NVDD3 to NVDD4 - Added 225 BGA column. - Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 21	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 9	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at <http://www.freescale.com/imx>. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from <http://www.arm.com>.