Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mxldvm15r2

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
JTAG	
$\overline{TRST}$	Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller.
$\overline{TDO}$	Serial Output for test instructions and data. Changes on the falling edge of TCK.
TDI	Serial Input for test instructions and data. Sampled on the rising edge of TCK.
TCK	Test Clock to synchronize test logic and control register access through the JTAG port.
TMS	Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK.
DMA	
$\overline{DMA\_REQ}$	$\overline{DMA\ Request}$—external DMA request signal. Multiplexed with SPI1_SPI_RDY.
BIG_ENDIAN	Big Endian—Input signal that determines the configuration of the external chip-select space. If it is driven logic-high at reset, the external chip-select space will be configured to big endian. If it is driven logic-low at reset, the external chip-select space will be configured to little endian. This input must not change state after power-on reset negates or during chip operation.
ETM	
ETMTRACESYNC	ETM sync signal which is multiplexed with A24. ETMTRACESYNC is selected in ETM mode.
ETMTRACECLK	ETM clock signal which is multiplexed with A23. ETMTRACECLK is selected in ETM mode.
ETMPIPESTAT [2:0]	ETM status signals which are multiplexed with A [22:20]. ETMPIPESTAT [2:0] are selected in ETM mode.
ETMTRACEPKT [7:0]	ETM packet signals which are multiplexed with $\overline{ECB}$, $\overline{LBA}$, BCLK (burst clock), PA17, A [19:16]. ETMTRACEPKT [7:0] are selected in ETM mode.
CMOS Sensor Interface	
CSI_D [7:0]	Sensor port data
CSI_MCLK	Sensor port master clock
CSI_VSYNC	Sensor port vertical sync
CSI_HSYNC	Sensor port horizontal sync
CSI_PIXCLK	Sensor port data latch clock
LCD Controller	
LD [15:0]	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
FLM/VSYNC	Frame Sync or Vsync—This signal also serves as the clock signal output for the gate driver (dedicated signal SPS for Sharp panel HR-TFT).
LP/HSYNC	Line pulse or H sync
LSCLK	Shift clock
ACD/OE	Alternate crystal direction/output enable.
CONTRAST	This signal is used to control the LCD bias voltage as contrast control.
SPL_SPR	Program horizontal scan direction (Sharp panel dedicated signal).
PS	Control signal output for source driver (Sharp panel dedicated signal).

3 Electrical Characteristics

This section contains the electrical specifications and timing diagrams for the i.MXL processor.

3.1 Maximum Ratings

Table 4 provides information on maximum ratings which are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits listed in Recommended Operating Range Table 5 on page 18 or the DC Characteristics table.

Table 4. Maximum Ratings

Symbol	Rating	Minimum	Maximum	Unit
NV_{DD}	DC I/O Supply Voltage	-0.3	3.3	V
QV_{DD}	DC Internal (core = 150 MHz) Supply Voltage	-0.3	1.9	V
QV_{DD}	DC Internal (core = 200 MHz) Supply Voltage	-0.3	2.0	V
AV_{DD}	DC Analog Supply Voltage	-0.3	3.3	V
$BTRFV_{DD}$	DC Bluetooth Supply Voltage	-0.3	3.3	V
VESD_HBM	ESD immunity with HBM (human body model)	–	2000	V
VESD_MM	ESD immunity with MM (machine model)	–	100	V
ILatchup	Latch-up immunity	–	200	mA
Test	Storage temperature	-55	150	°C
Pmax	Power Consumption	800[1]	1300[2]	mW

[1] A typical application with 30 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM® core-that is, 7x GPIO, 15x Data bus, and 8x Address bus.

[2] A worst-case application with 70 pads simultaneously switching assumes the GPIO toggling and instruction fetches from the ARM core-that is, 32x GPIO, 30x Data bus, 8x Address bus. These calculations are based on the core running its heaviest OS application at 200MHz, and where the whole image is running out of SDRAM. QVDD at 2.0V, NVDD and AVDD at 3.3V, therefore, 180mA is the worst measurement recorded in the factory environment, max 5mA is consumed for OSC pads, with each toggle GPIO consuming 4mA.

3.2 Recommended Operating Range

Table 5 provides the recommended operating ranges for the supply voltages and temperatures. The i.MXL processor has multiple pairs of VDD and VSS power supply and return pins. QVDD and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because AVDD pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the AVDD pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 2 on page 4.

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA
I_{IH}	Input high leakage current (V_{IN} = V_{DD}, no pull-up or pull-down)	–	–	±1	µA
I_{OH}	Output high current (V_{OH} = $0.8V_{DD}$, V_{DD} = 1.8V)	4.0	–	–	mA
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	-4.0	–	–	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is high impedance)	–	–	±5	µA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXL.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.
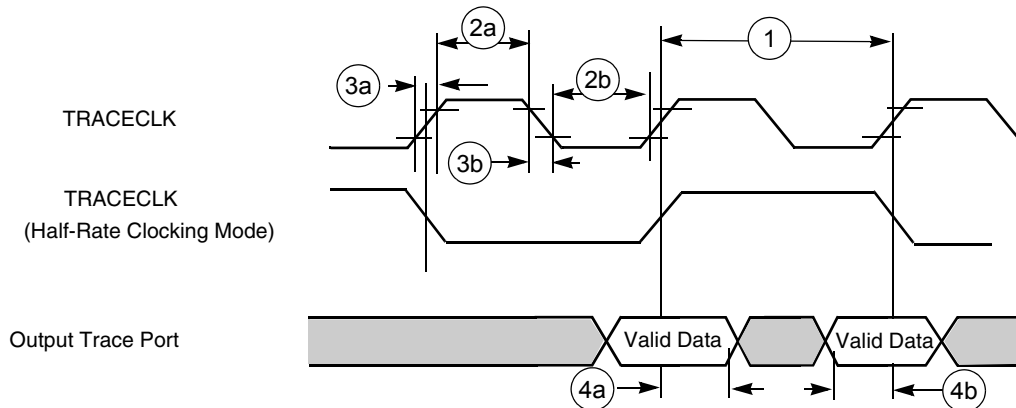

Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	**Maximum**	**Minimum**	**Maximum**	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
4a	Clock[1] rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock[1] rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock[1] fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock[1] fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock[1] rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock[1] rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock[1] fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock[1] fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock[1] rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock[1] rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock[1] rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock[1] fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock[1] fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock[1] rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock[1] fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock[1] rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{DTACK}$ setup time	2.52	–	–	2.5	–	–	ns

[1] Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{DTACK}$ Signal Description

The $\overline{DTACK}$ signal is the external input data acknowledge signal. When using the external $\overline{DTACK}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{DTACK}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

4.4.2 $\overline{DTACK}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	**Maximum**	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

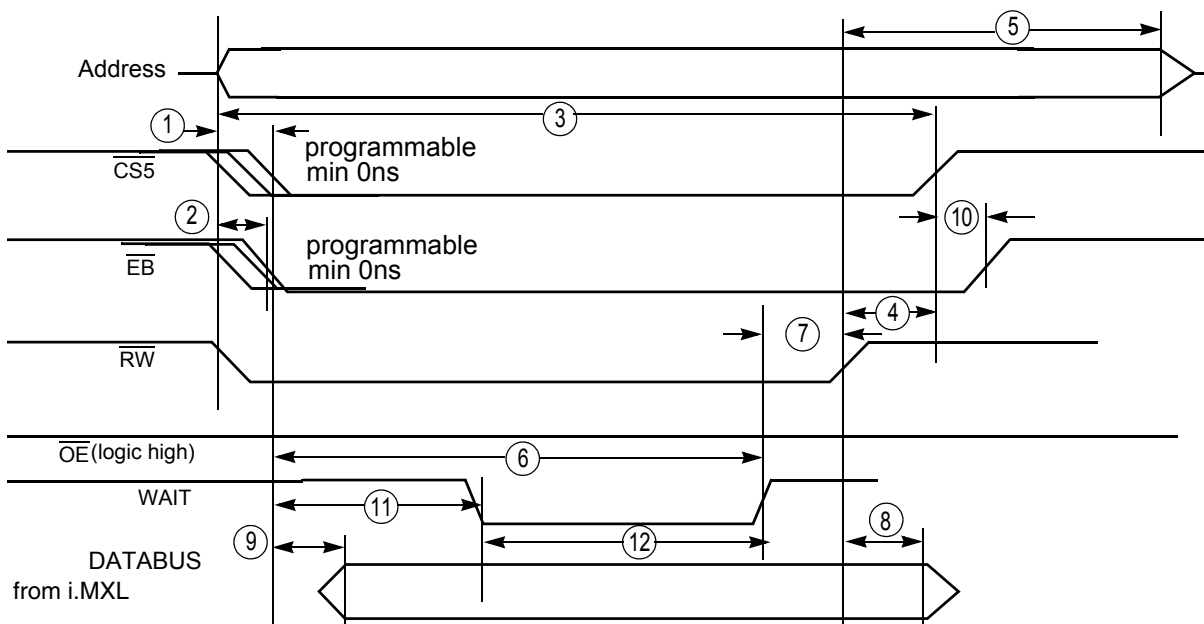## 4.4.2.3 WAIT Write Cycle without DMA

Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

| Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	**Maximum**	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	$\overline{RW}$ negated to Address inactive	64.22	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns

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Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	**Maximum**	
7	Wait asserted to $\overline{RW}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{RW}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	0.5T	0.5T+0.5	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

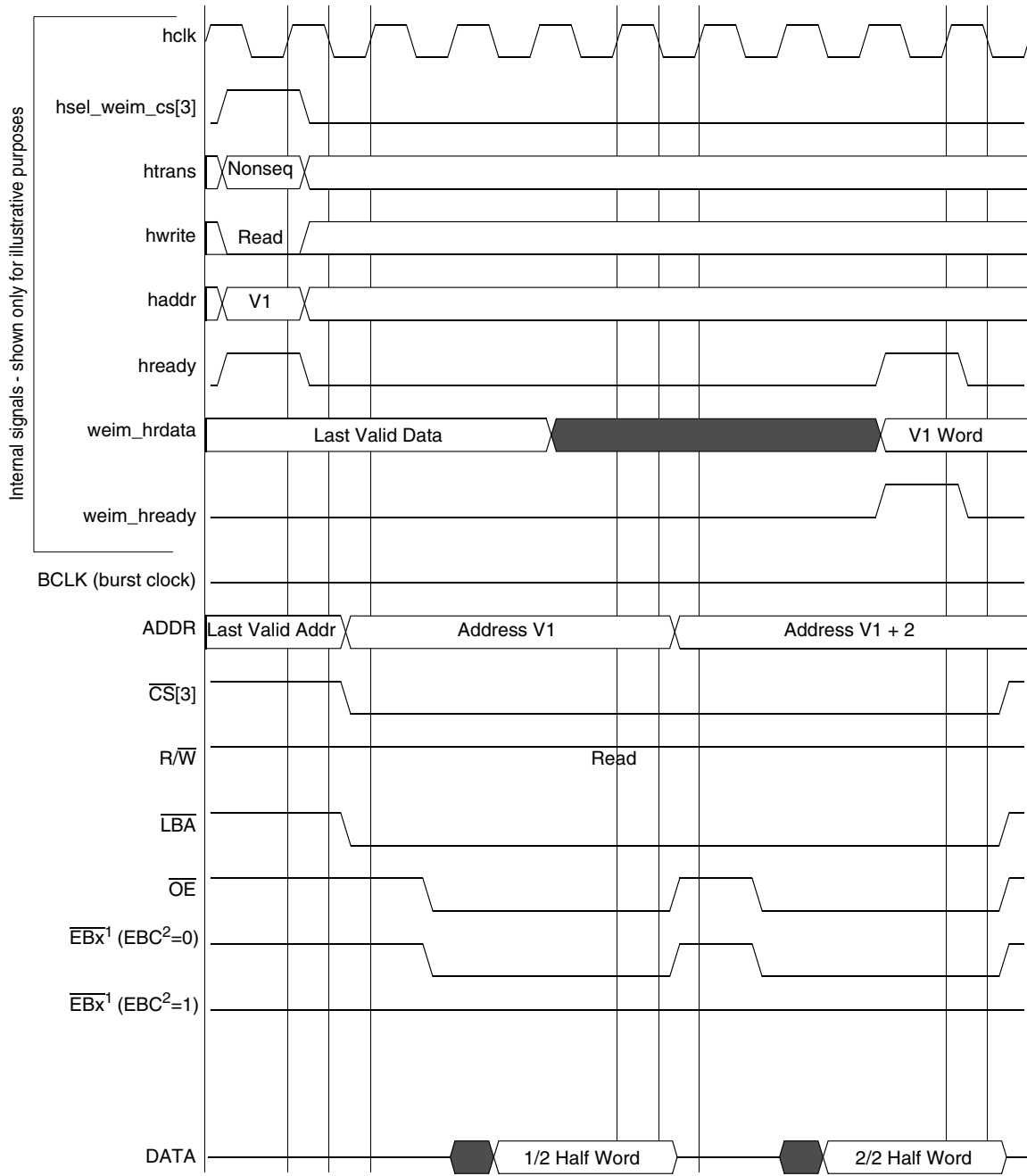## 4.4.2.4   WAIT Write Cycle DMA Enabled
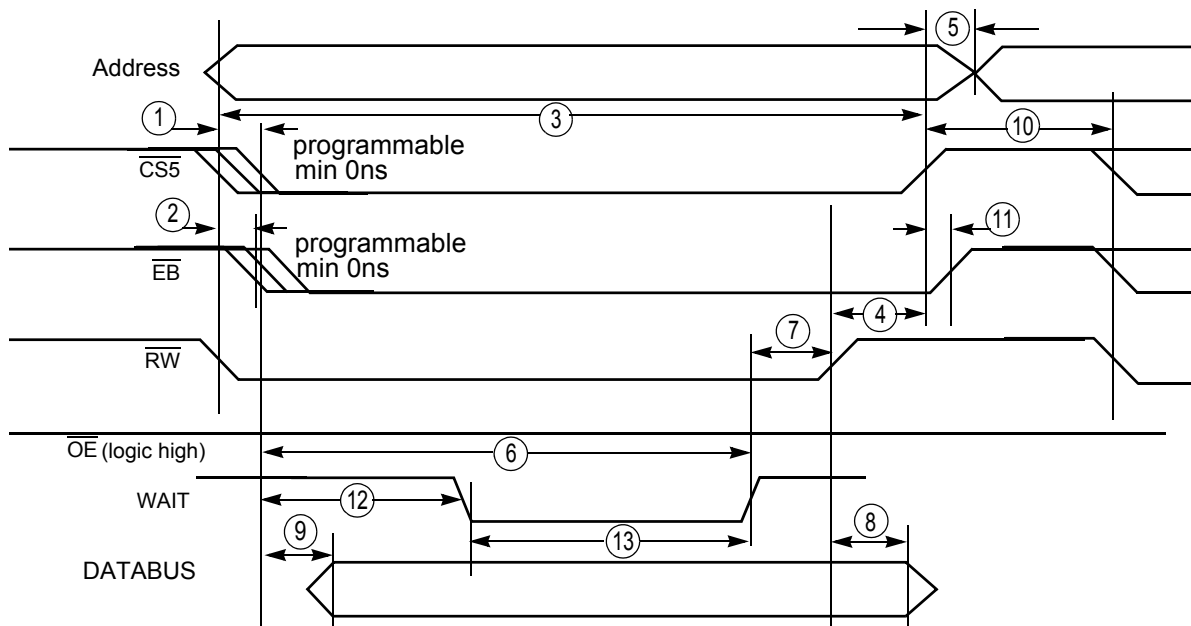
Figure 9. WAIT Write Cycle DMA Enabled
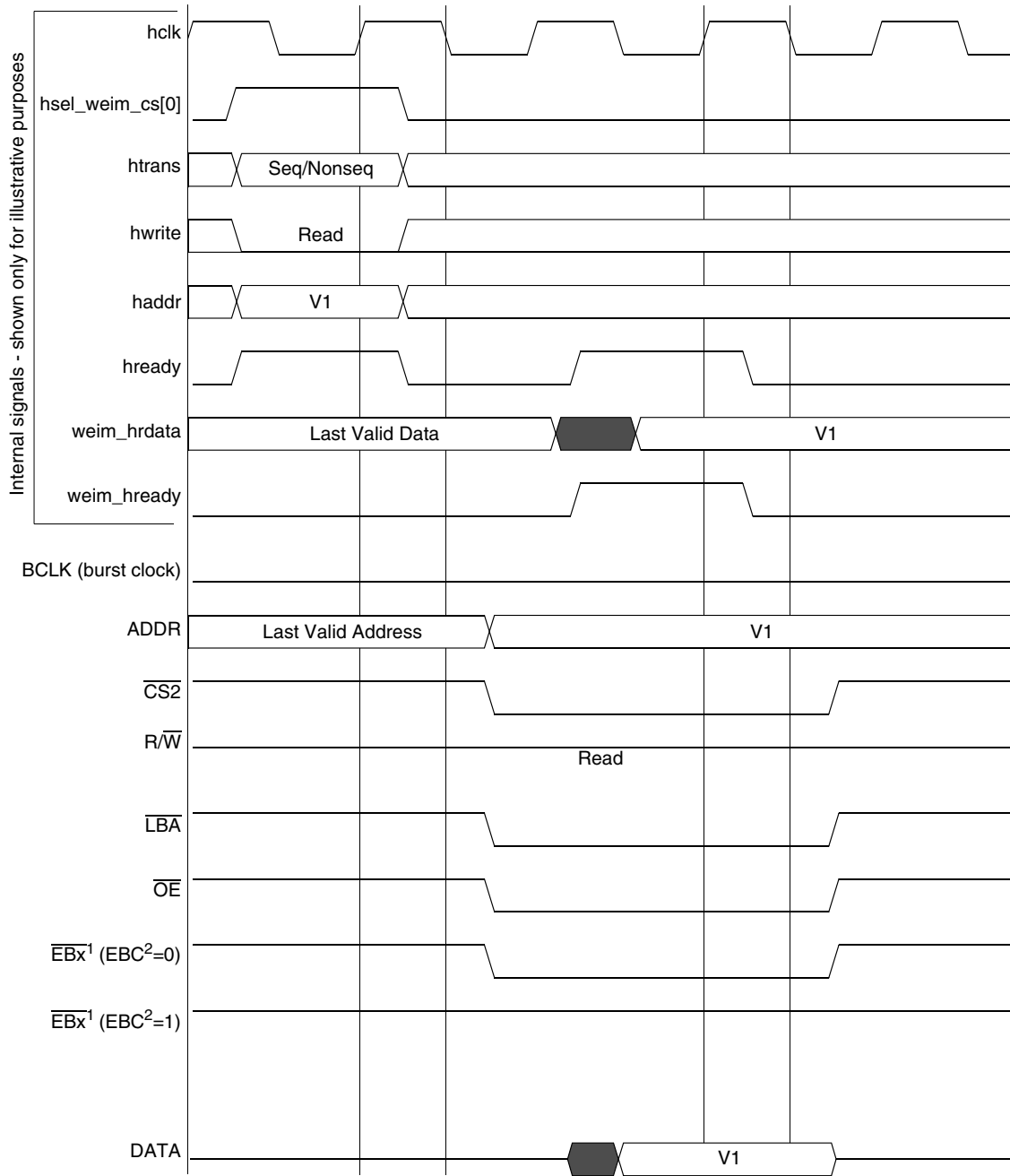
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register
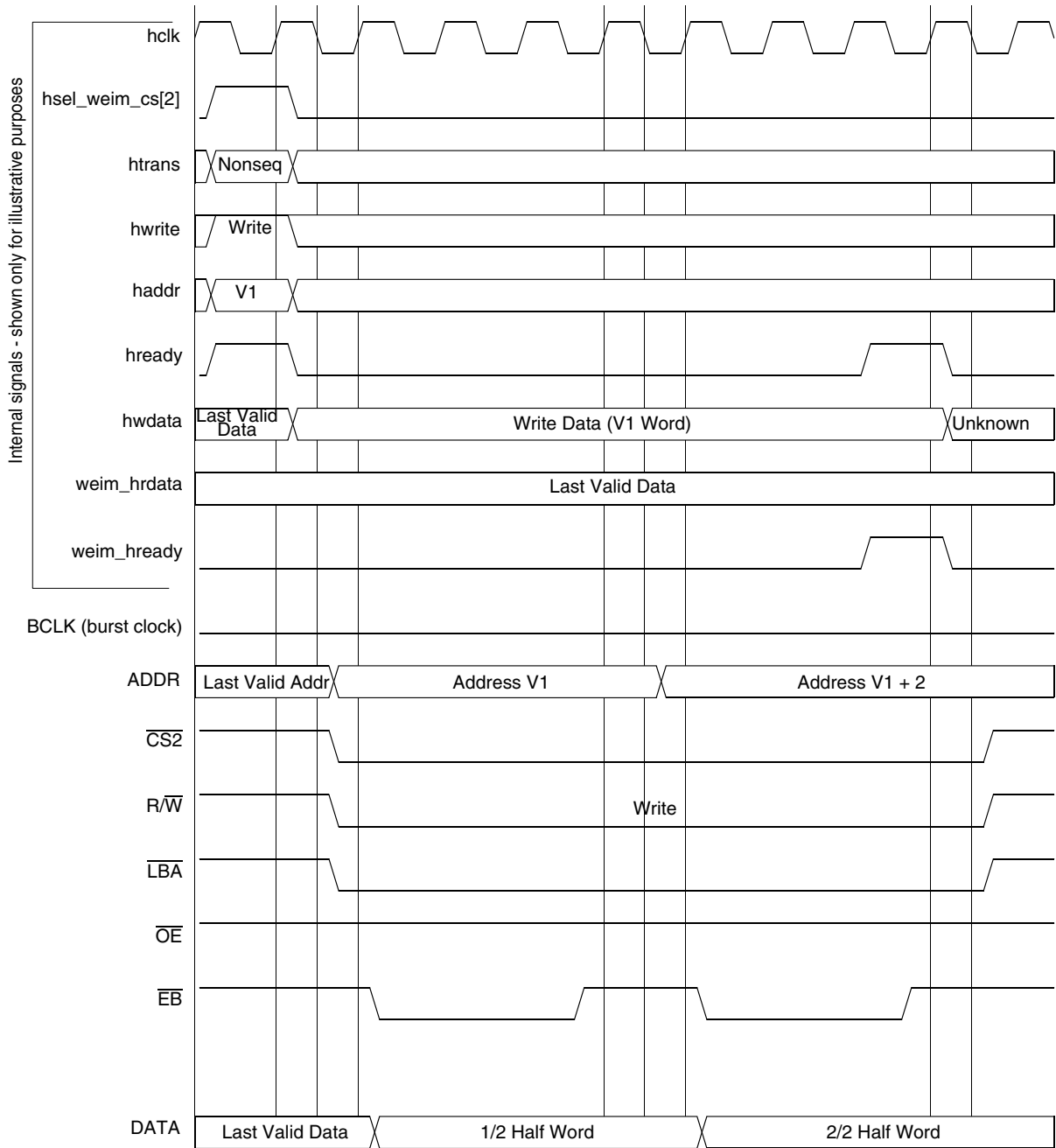
Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF
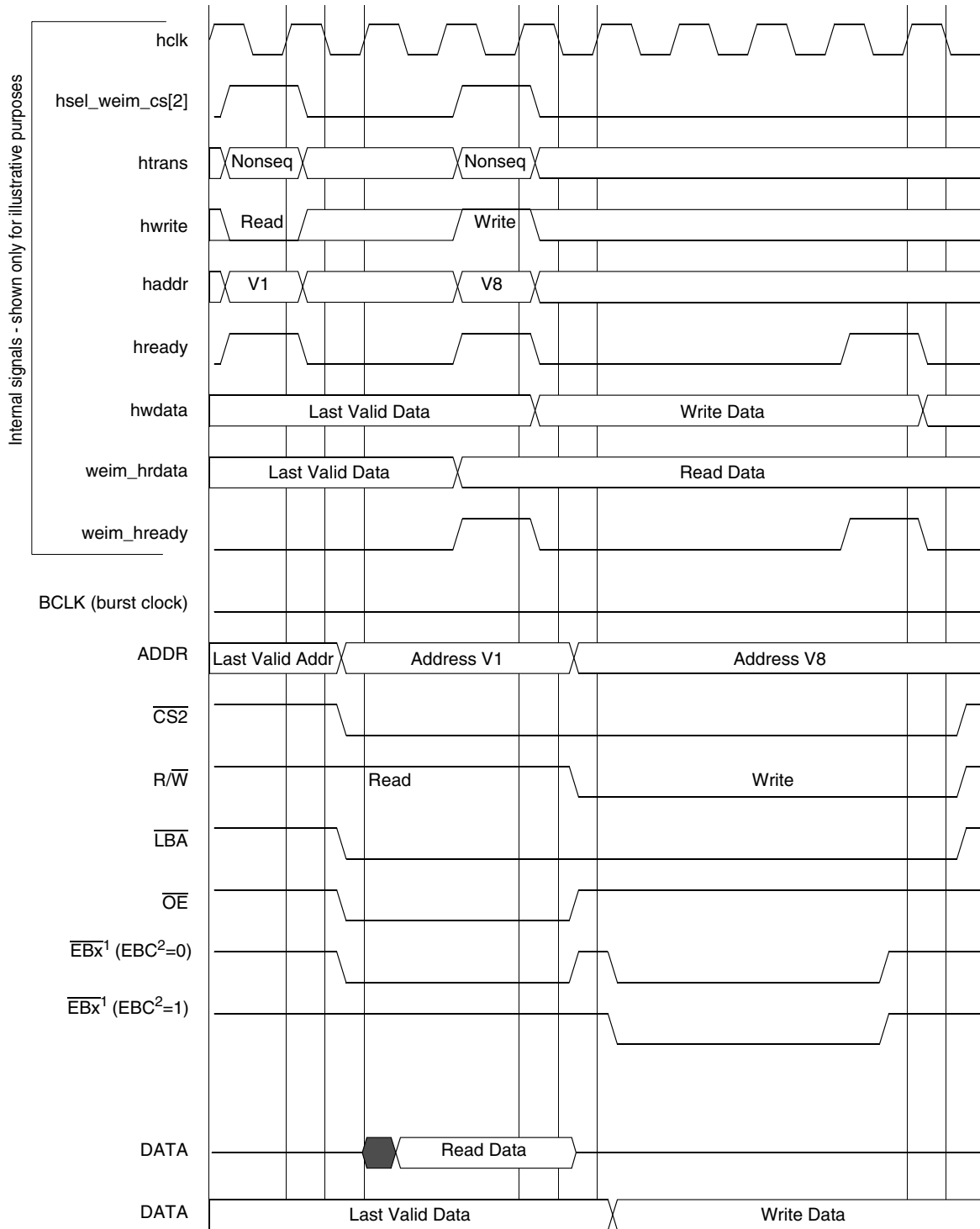
Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register
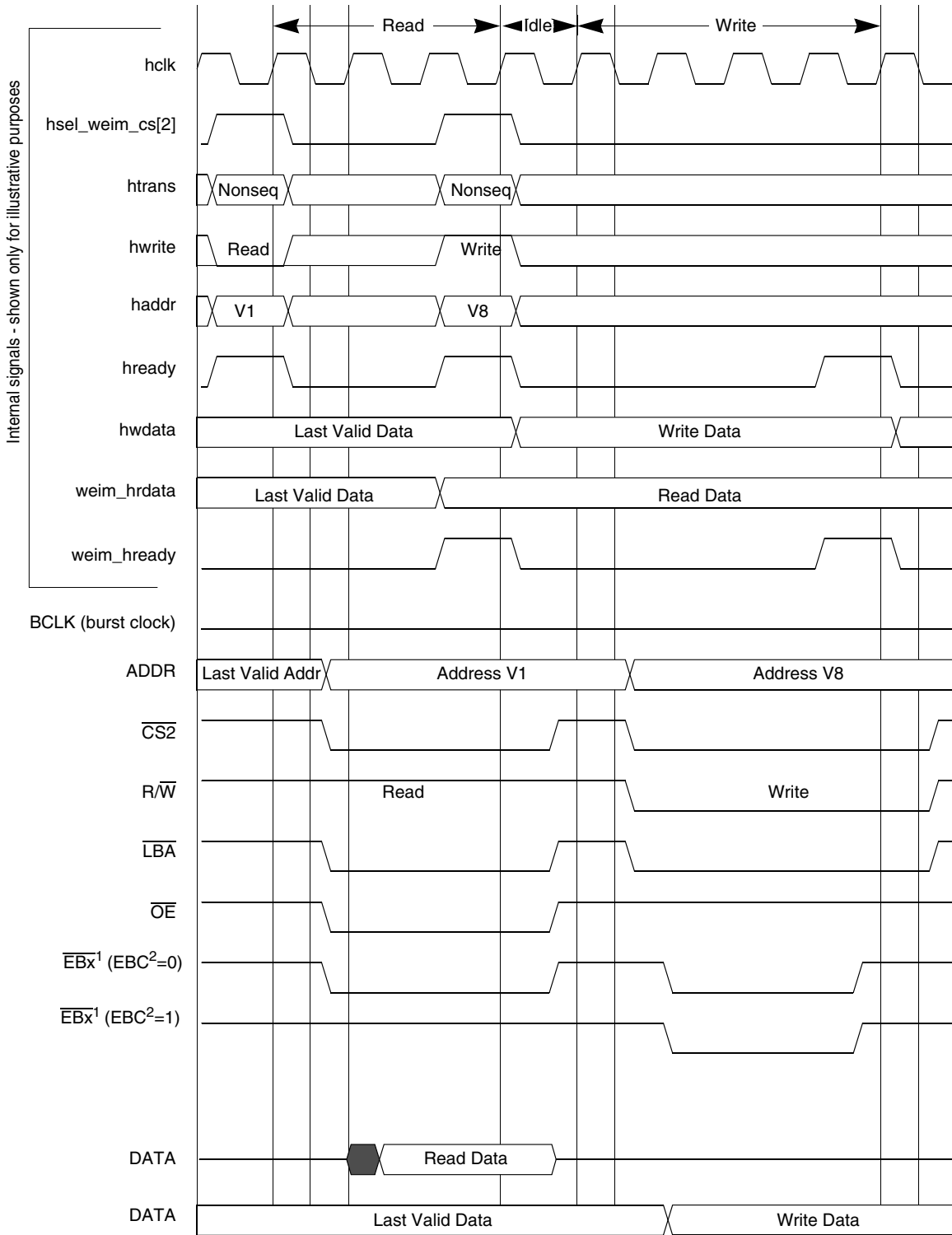
Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF
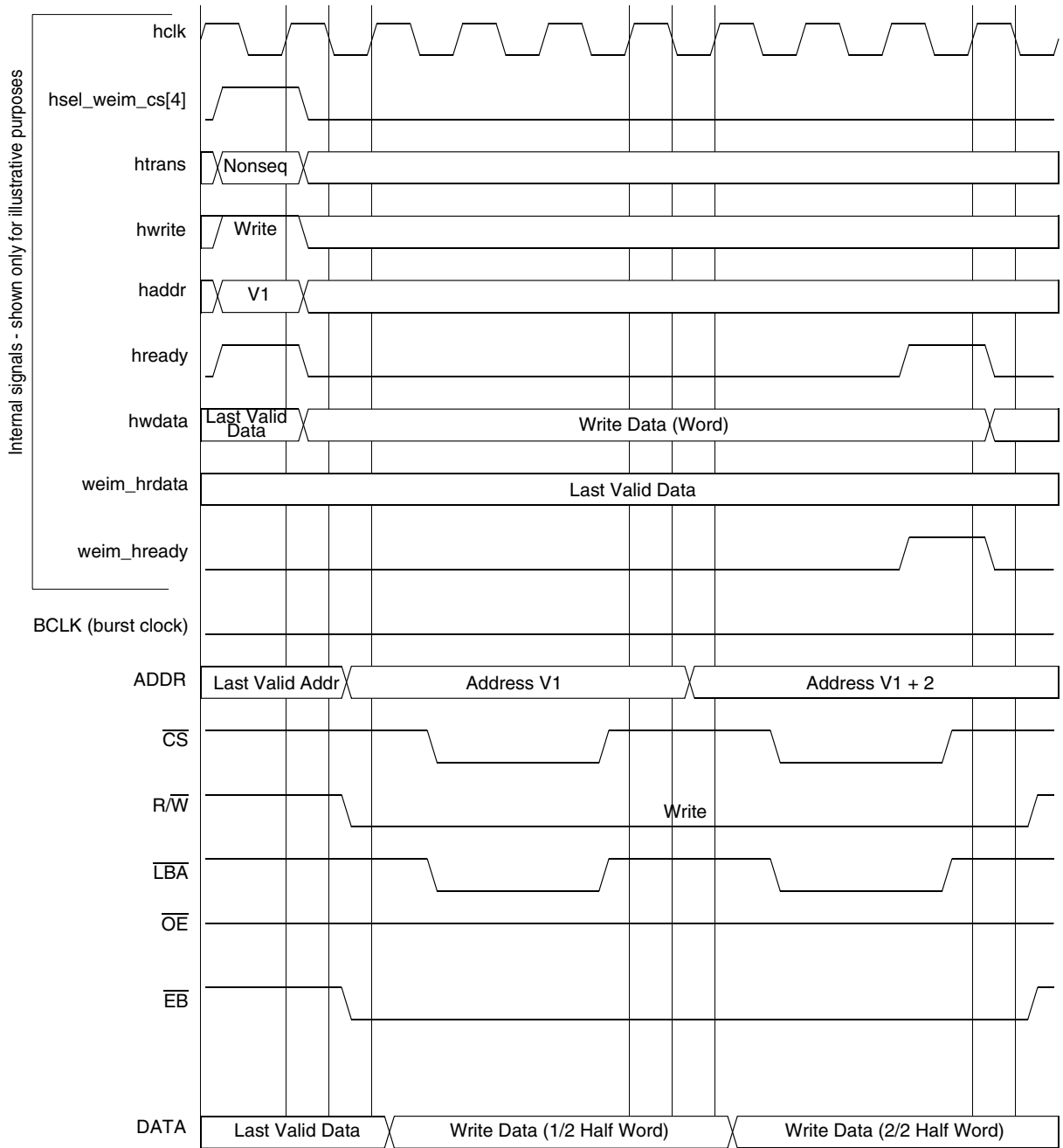
Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF

Figure 46. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 47 shows the different scenarios on the bus.

Figure 47. Stop Transmission During Different Scenarios

Table 24. Timing Values for Figure 43 through Figure 47

Parameter	Symbol	Minimum	Maximum	Unit
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL)				
Command response cycle	NCR	2	64	Clock cycles
Identification response cycle	NID	5	5	Clock cycles
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles

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Table 32. I²C Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	Hold time (repeated) START condition	182	–	160	–	ns
2	Data hold time	0	171	0	150	ns
3	Data setup time	11.4	–	10	–	ns
4	HIGH period of the SCL clock	80	–	120	–	ns
5	LOW period of the SCL clock	480	–	320	–	ns
6	Setup time for STOP condition	182.4	–	160	–	ns

4.13 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 60 through Figure 62.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.
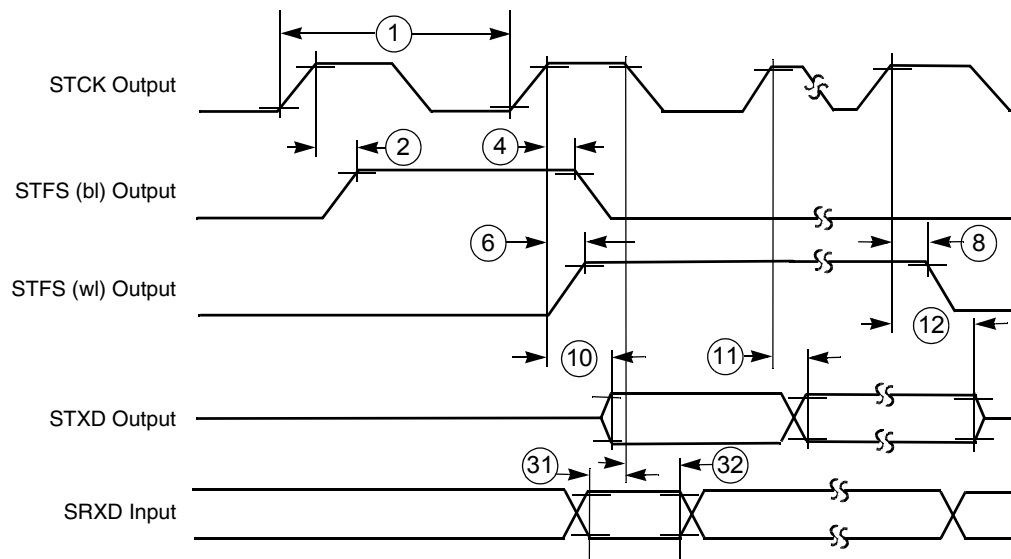
Note: SRXD input in synchronous mode only.

Figure 59. SSI Transmitter Internal Clock Timing Diagram

Table 33. SSI (Port C Primary Function) Timing Parameter Table (Continued)

| Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

[1] All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

[2] There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

[3] bl = bit length; wl = word length.
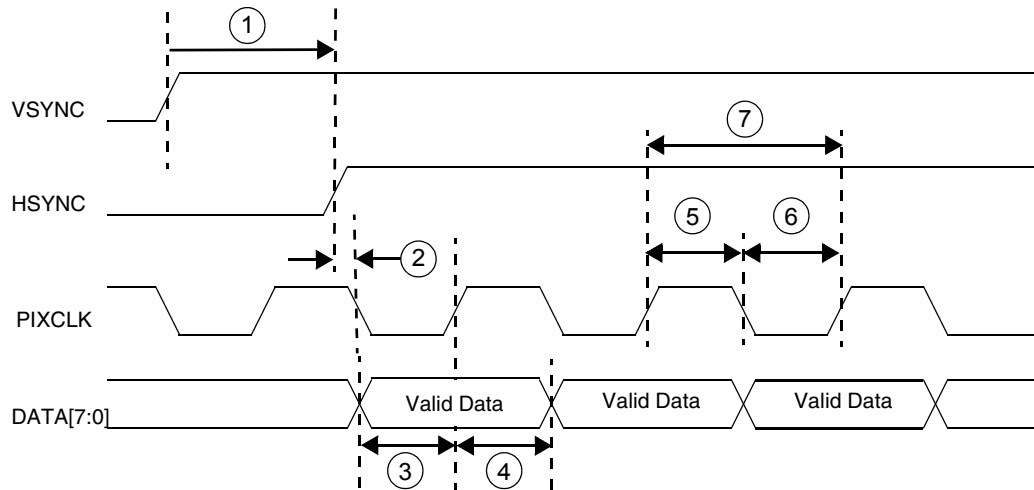
**Figure 63. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**
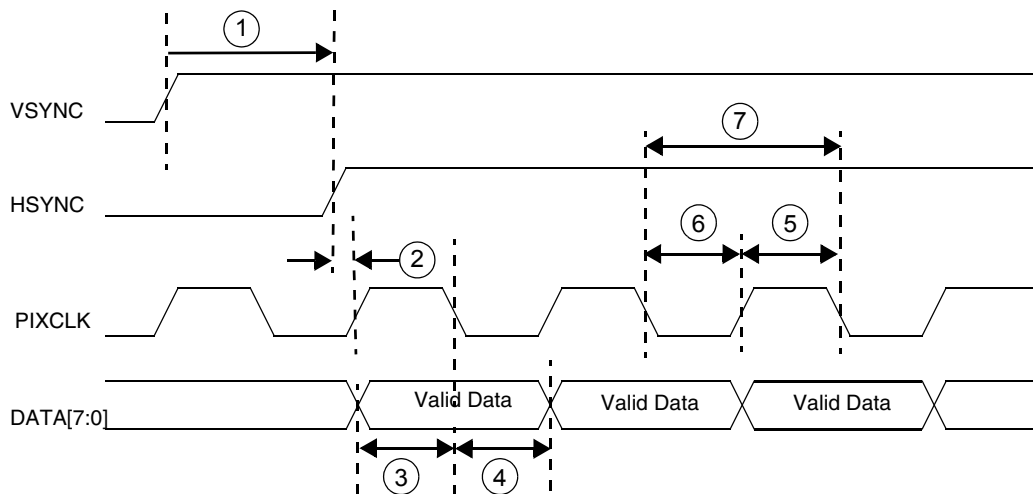
**Figure 64. Sensor Output Data on Pixel Clock Rising Edge
CSI Latches Data on Pixel Clock Falling Edge**

Table 35. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

> max rise time allowed = (positive duty cycle - hold time)
> max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

> max rise time = (period / 2 - hold time)
> max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

> positive duty cycle = 10 / 2 = 5ns
> => max rise time allowed = 5 - 1 = 4ns
>
> negative duty cycle = 10 / 2 = 5ns
> => max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

> max fall time allowed = (negative duty cycle - hold time)
> max rise time allowed = (positive duty cycle - setup time)

4.14.2   Non-Gated Clock Mode

Figure 65 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 66 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 36.
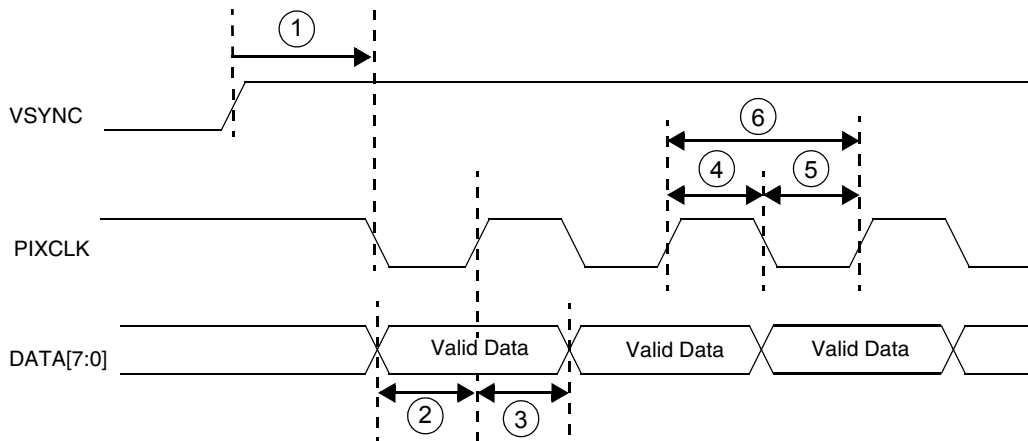
**Figure 65. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge**

5 Pin-Out and Package Information

Table 37 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 9.

Table 37. i.MXL 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS	SD_DAT3	SD_CLK	NVSS	USBD_AFE	NVDD4	NVSS	$\overline{\text{UART1\_RTS}}$	UART1_RXD	NVDD3	N.C.	N.C.	QVDD4	N.C.	N.C.	N.C.	A
B	A24	SD_DAT1	SD_CMD	PB16	$\overline{\text{USBD\_ROE}}$	USBD_VP	SSI_RXCLK	SSI_TXCLK	SPI1_SCLK	N.C.	N.C.	N.C.	QVSS	N.C.	N.C.	N.C.	B
C	A23	D31	SD_DAT0	PB15	USBD_RCV	$\overline{\text{UART2\_CTS}}$	UART2_RXD	SSI_RXFS	UART1_TXD	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	C
D	A22	D30	D29	PB14	USBD_SUSPND	USBD_VPO	USBD_VMO	SSI_RXDAT	$\overline{\text{SPI1\_SPI\_RDY}}$	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	$\overline{\text{UART2\_RTS}}$	SSI_TXDAT	SPI1_$\overline{\text{SS}}$	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	E
F	A18	D27	D25	A19	A16	PB18	UART2_TXD	SSI_TXFS	SPI1_MISO	N.C.	N.C.	REV	N.C.	N.C.	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	PB17	PB19	$\overline{\text{UART1\_CTS}}$	SPI1_MOSI	N.C.	CLS	CONTRAST	ACD/OE	LP/HSYNC	FLM/VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS	QVSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS	NVDD1	NVSS	NVSS	LD6	LD7	LD8	LD11	QVDD3	QVSS	J
K	A10	D16	A9	D17	NVDD1	NVSS	NVSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS	$\overline{\text{CAS}}$	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS	$\overline{\text{RW}}$	MA10	$\overline{\text{RAS}}$	$\overline{\text{RESET\_IN}}$	BIG_ENDIAN	CSI_D4	CSI_HSYNC	CSI_VSYNC	CSI_D6	CSI_D5	M
N	A4	$\overline{\text{EB1}}$	D10	D7	A0	D4	PA17	D1	DQM1	$\overline{\text{RESET\_SF}}$[1]	$\overline{\text{RESET\_OUT}}$	BOOT2	CSI_PIXCLK	CSI_D7	TMS	TDI	N
P	A3	D9	$\overline{\text{EB0}}$	$\overline{\text{CS3}}$	D6	$\overline{\text{ECB}}$	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	$\overline{\text{TRST}}$	I2C_SCL	I2C_SDA	XTAL32K	P
R	$\overline{\text{EB2}}$	$\overline{\text{EB3}}$	A1	$\overline{\text{CS4}}$	D8	D5	$\overline{\text{LBA}}$	BCLK[2]	D0	DQM0	SDCKE0	POR	BOOT1	$\overline{\text{TDO}}$	QVDD2	EXTAL32K	R
T	NVSS	A2	$\overline{\text{OE}}$	$\overline{\text{CS5}}$	$\overline{\text{CS2}}$	$\overline{\text{CS1}}$	$\overline{\text{CS0}}$	MA11	DQM2	$\overline{\text{SDWE}}$	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

[1] This signal is not used and should be floated in an actual application.

[2] burst clock