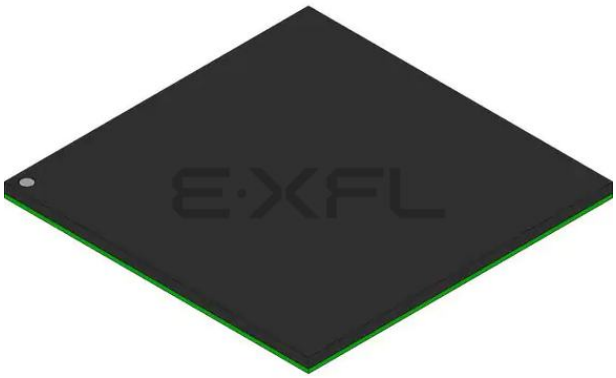

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9328mxldvm20

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD2	D11	G14	LP/HSYNC	O				PD13	69K				PD13
NVDD2	E11	G13	ACD/OE	O				PD12	69K				PD12
NVDD2	C10	G12	CONTRAST	O				PD11	69K				PD11
NVDD2	B11	F16	SPL_SPR	O		$\overline{\text{UART2\_DSR}}$	O	PD10	69K	SPI2_TXD			PD10
NVDD2	A12	H10	PS	O		$\overline{\text{UART2\_RI}}$	O	PD9	69K			SPI2_RXD_1	PD9
NVDD2	F10	G11	CLS	O		$\overline{\text{UART2\_DCD}}$	O	PD8	69K	$\overline{\text{SPI2\_SS}}$			PD8
NVDD2	A11	F12	REV	O		$\overline{\text{UART2\_DTR}}$	I	PD7	69K	SPI2_SCLK			PD7
NVDD2	B10	F15	LSCLK	O				PD6	69K				PD6
NVDD3	D10	G9	SPI1_MOSI	I/O				PC17	69K				PC17
NVDD3	E10	F9	SPI1_MISO	I/O				PC16	69K				PC16
NVDD3	B9	E9	SPI1_$\overline{\text{SS}}$	I/O				PC15	69K				PC15
NVDD3	A10	B9	SPI1_SCLK	I/O				PC14	69K				PC14
NVDD3	A9	D9	SPI1_$\overline{\text{SPI_RDY}}$	I/O				PC13	69K			$\overline{\text{DMA\_REQ}}$	PC13
NVDD3	E8	A9	UART1_RXD	I				PC12	69K				PC12
NVDD3	B8	C9	UART1_TXD	O				PC11	69K				PC11
NVDD3	C9	A8	$\overline{\text{UART1\_RTS}}$	I				PC10	69K				PC10
NVDD3	E9	G8	$\overline{\text{UART1\_CTS}}$	O				PC9	69K				PC9
NVDD3	A8	B8	SSI_TXCLK	I/O				PC8	69K				PC8
NVDD3	C8	F8	SSI_TXFS	I/O				PC7	69K				PC7
NVDD3	F9	E8	SSI_TXDAT	O				PC6	69K				PC6
NVDD3	B7	D8	SSI_RXDAT	I				PC5	69K				PC5
NVDD3	F8	B7	SSI_RXCLK	I				PC4	69K				PC4
NVDD3	A7	C8	SSI_RXFS	I				PC3	69K				PC3
NVDD4	C7	C7	UART2_RXD	I				PB31	69K				PB31

4.4.2.2 WAIT Read Cycle DMA Enabled

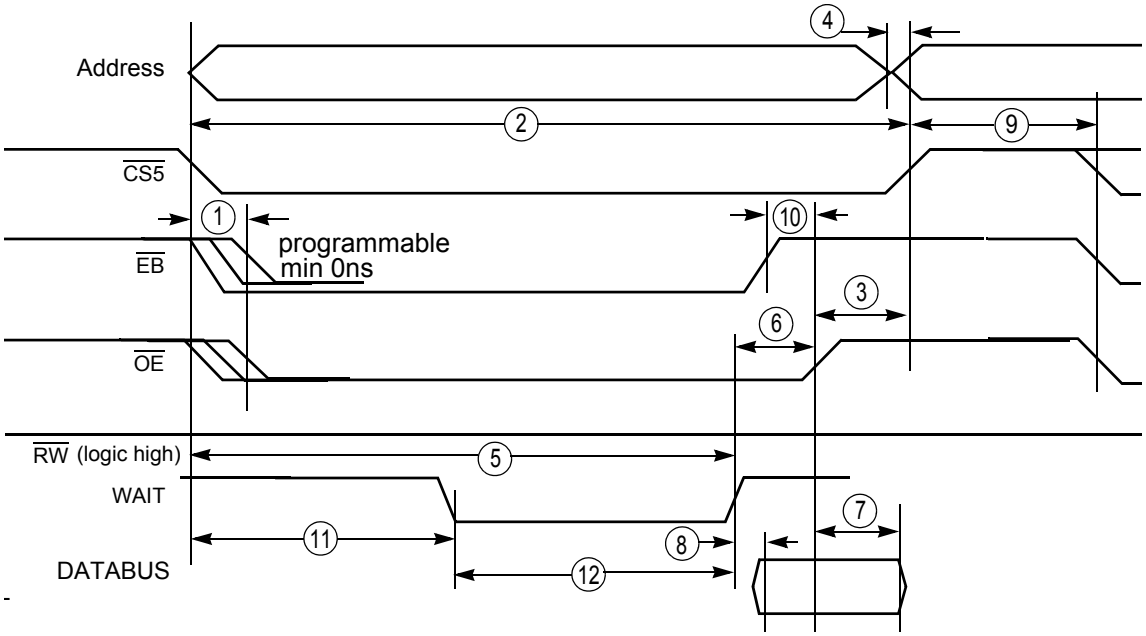
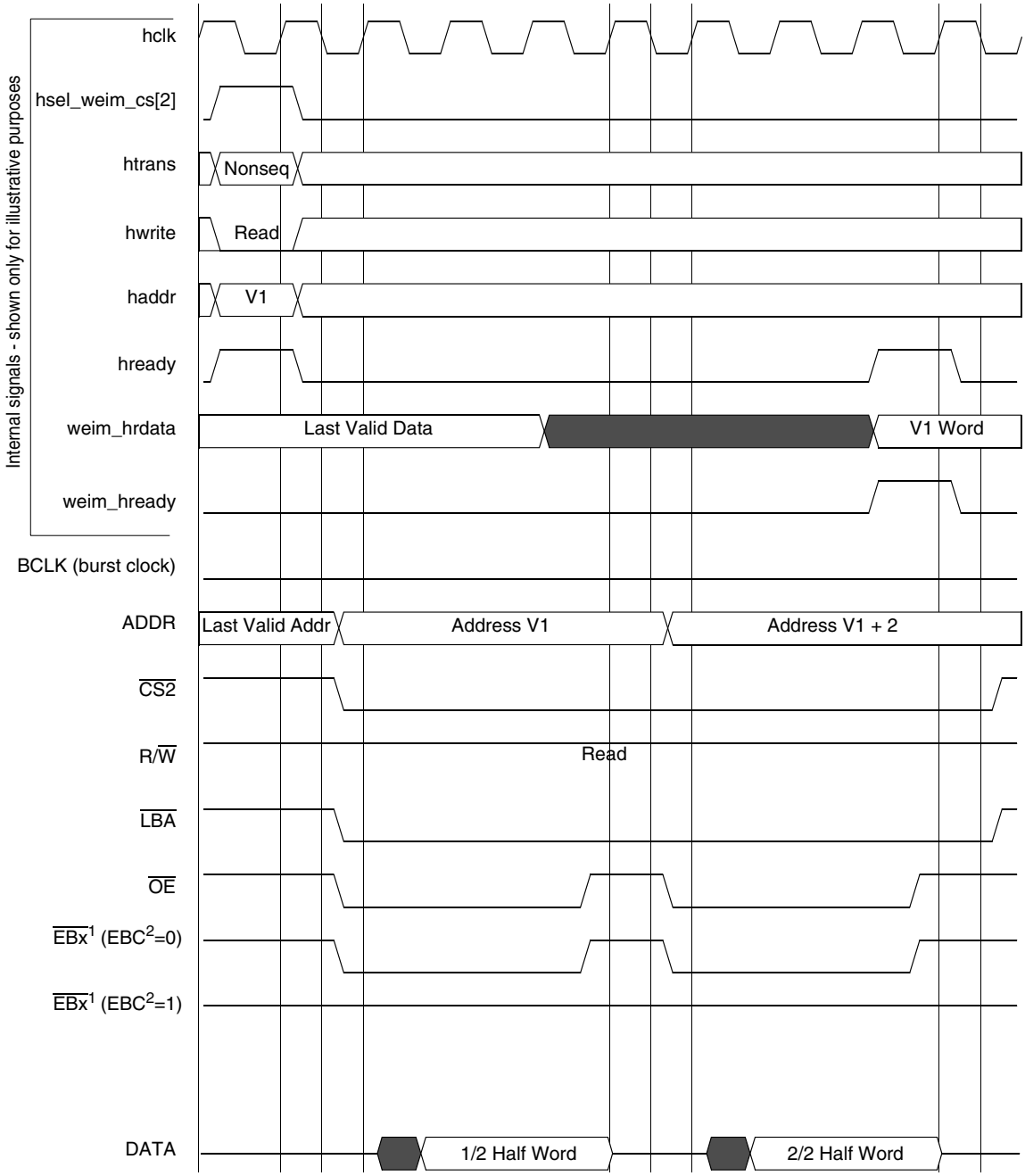


Figure 7. DTACK WAIT Read Cycle DMA Enabled

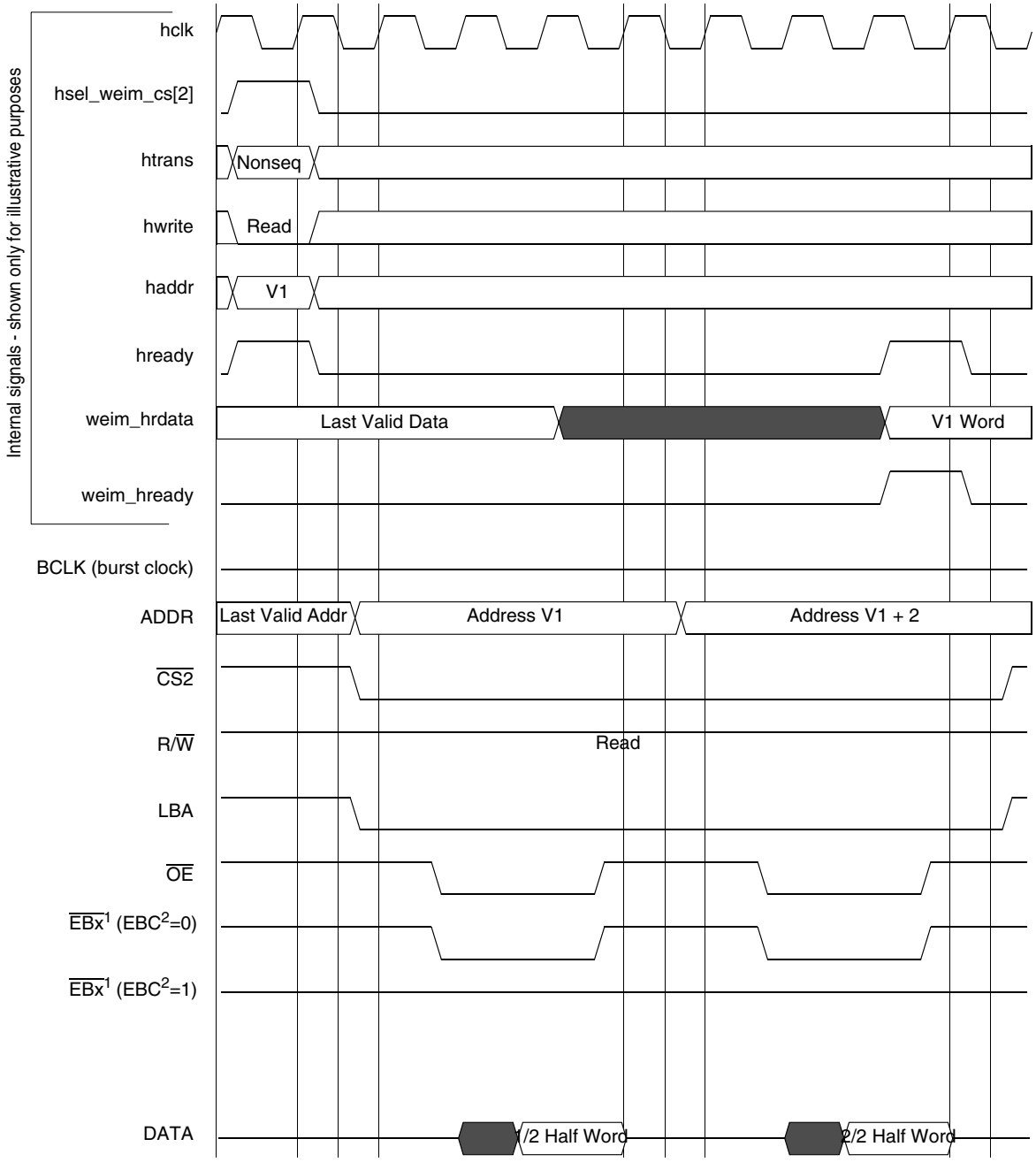
Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{OE}$ and $\overline{EB}$ assertion time	See note 2	–	ns
2	$\overline{CS}$ pulse width	3T	–	ns
3	$\overline{OE}$ negated before $\overline{CS5}$ is negated	1.5T-0.68	1.5T-0.06	ns
4	Address inactived before $\overline{CS}$ negated	–	0.05	ns
5	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
6	Wait asserted to $\overline{OE}$ negated	2T+1.57	3T+7.33	ns
7	Data hold timing after $\overline{OE}$ negated	T-1.49	–	ns
8	Data ready after wait is asserted	–	T	ns
9	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
10	OE negate after EB negate	0.06	0.18	ns
11	Wait becomes low after CS5 asserted	0	1019T	ns



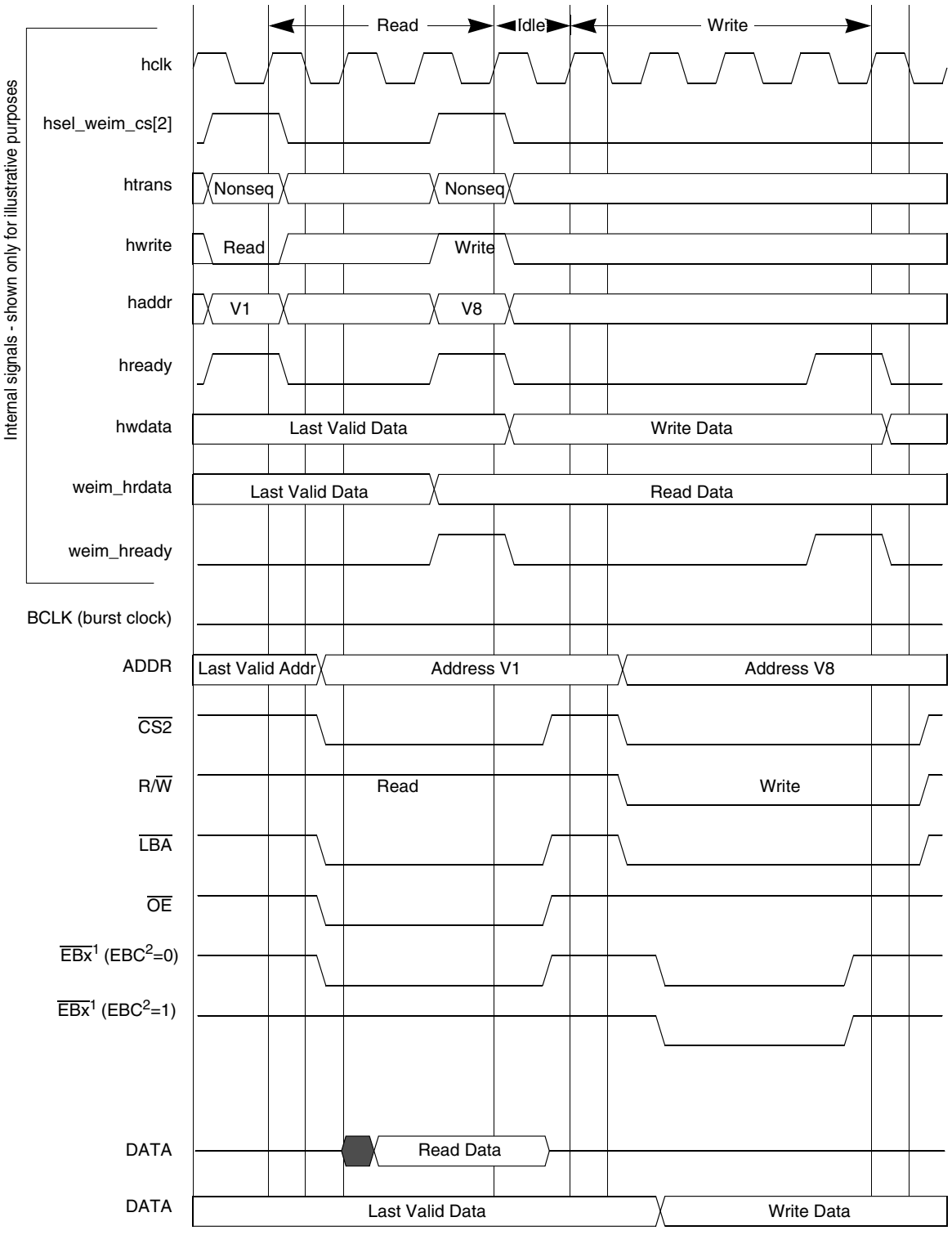
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF



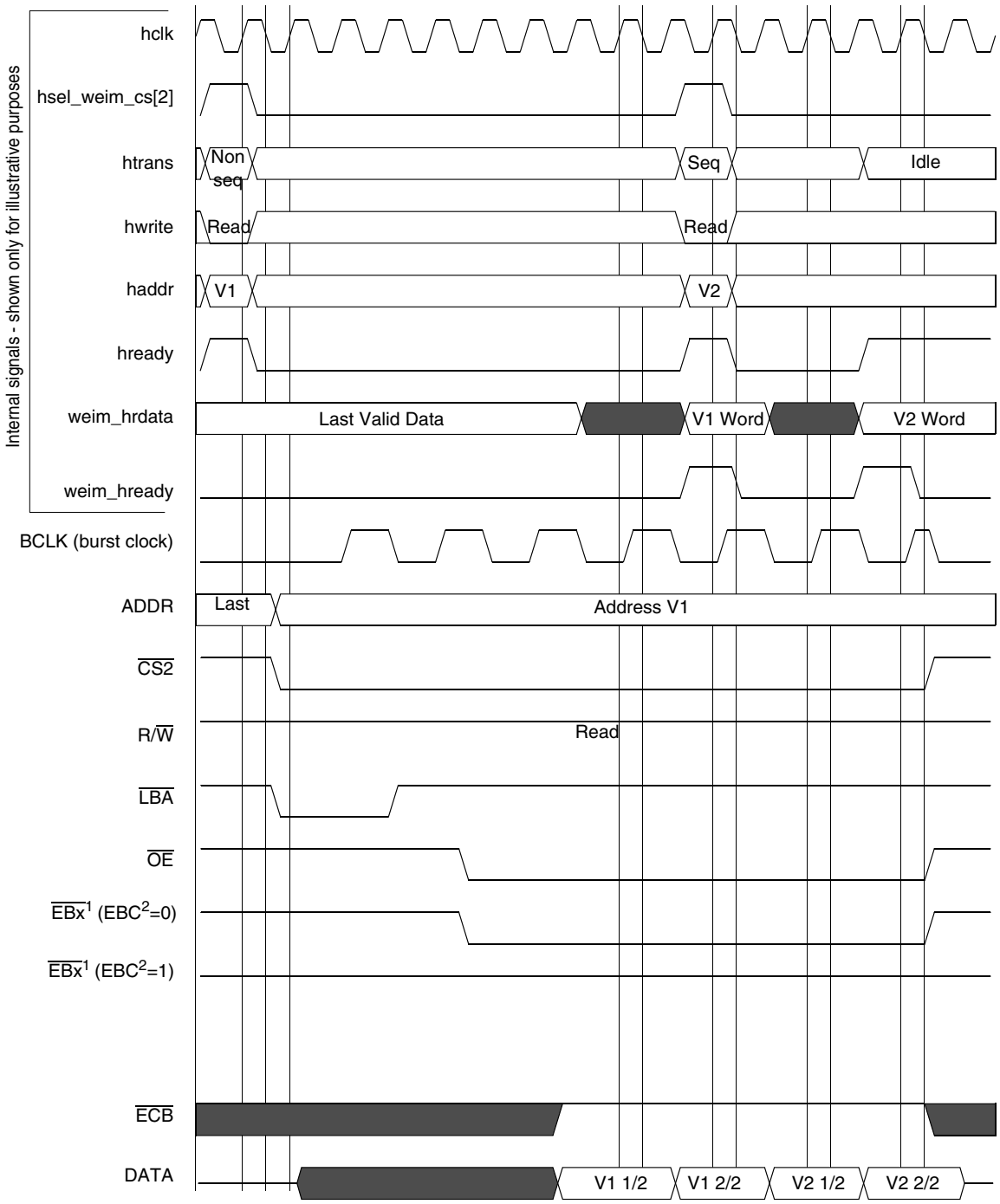
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 19. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF



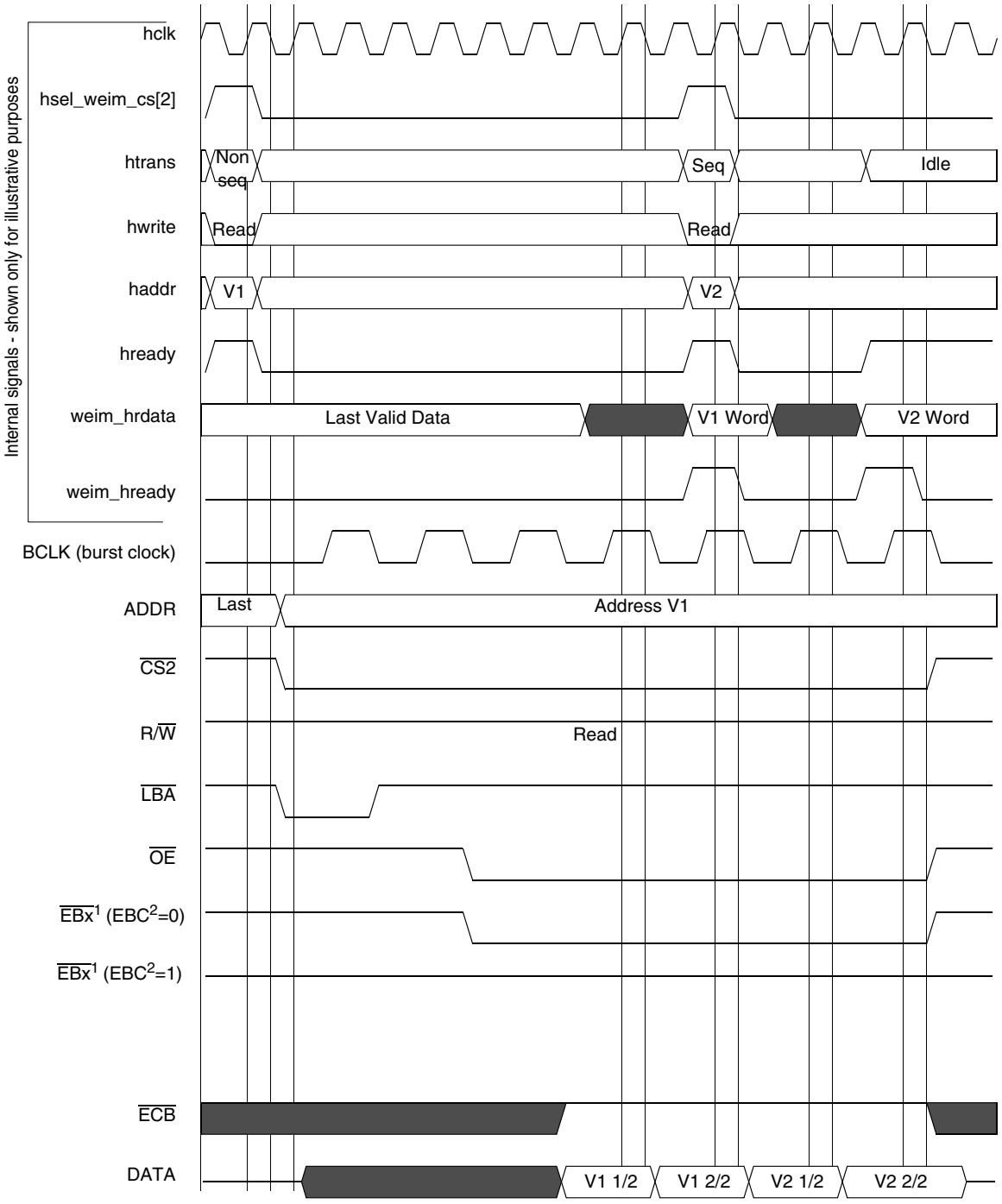
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 31. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF

Table 22. SDHC Bus Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency at Data transfer Mode (PP)[1]—10/30 cards	0	25/5	0	25/5	MHz
2	CLK frequency at Identification Mode[2]	0	400	0	400	kHz
3a	Clock high time[1]—10/30 cards	6/33	–	10/50	–	ns
3b	Clock low time[1]—10/30 cards	15/75	–	10/50	–	ns
4a	Clock fall time[1]—10/30 cards	–	10/50 (5.00)[3]	–	10/50	ns
4b	Clock rise time[1]—10/30 cards	–	14/67 (6.67)[3]	–	10/50	ns
5a	Input hold time[3]—10/30 cards	10.3/10.3	–	9/9	–	ns
5b	Input setup time[3]—10/30 cards	10.3/10.3	–	9/9	–	ns
6a	Output hold time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
6b	Output setup time[3]—10/30 cards	5.7/5.7	–	5/5	–	ns
7	Output delay time[3]	0	16	0	14	ns

1 $C_L \leq 100$ pF / 250 pF (10/30 cards)
2 $C_L \leq 250$ pF (21 cards)
3 $C_L \leq 25$ pF (1 card)

4.7.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly N_{ID} clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 43. The symbols for Figure 43 through Figure 47 are defined in Table 23.

Table 23. State Signal Parameters for Figure 43 through Figure 47

Card Active		Host Active	
Symbol	Definition	Symbol	Definition
Z	High impedance state	S	Start bit (0)
D	Data bits	T	Transmitter bit (Host = 1, Card = 0)
*	Repetition	P	One-cycle pull-up (1)
CRC	Cyclic redundancy check bits (7 bits)	E	End bit (1)

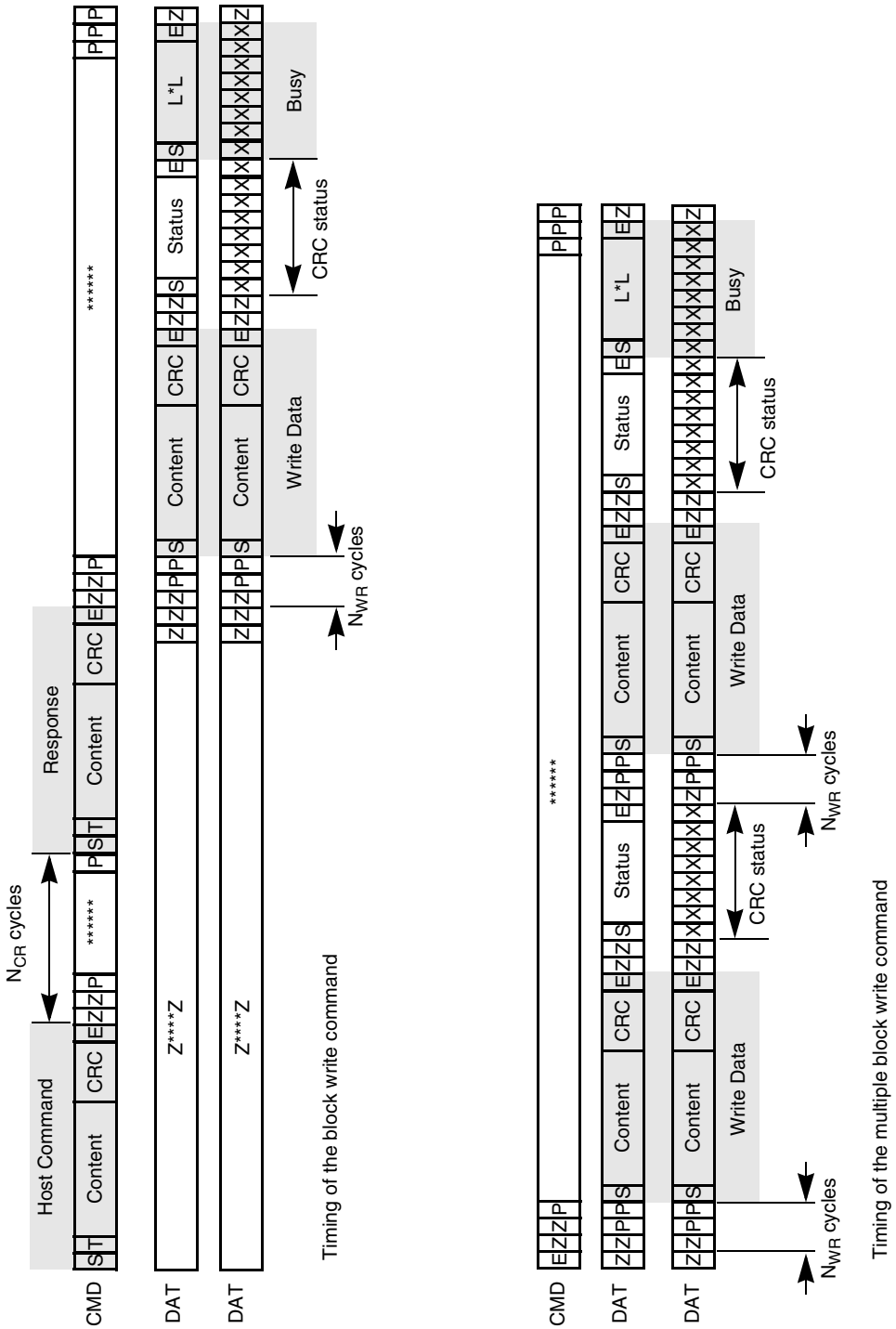


Figure 46. Timing Diagrams at Data Write

The stop transmission command may occur when the card is in different states. Figure 47 shows the different scenarios on the bus.

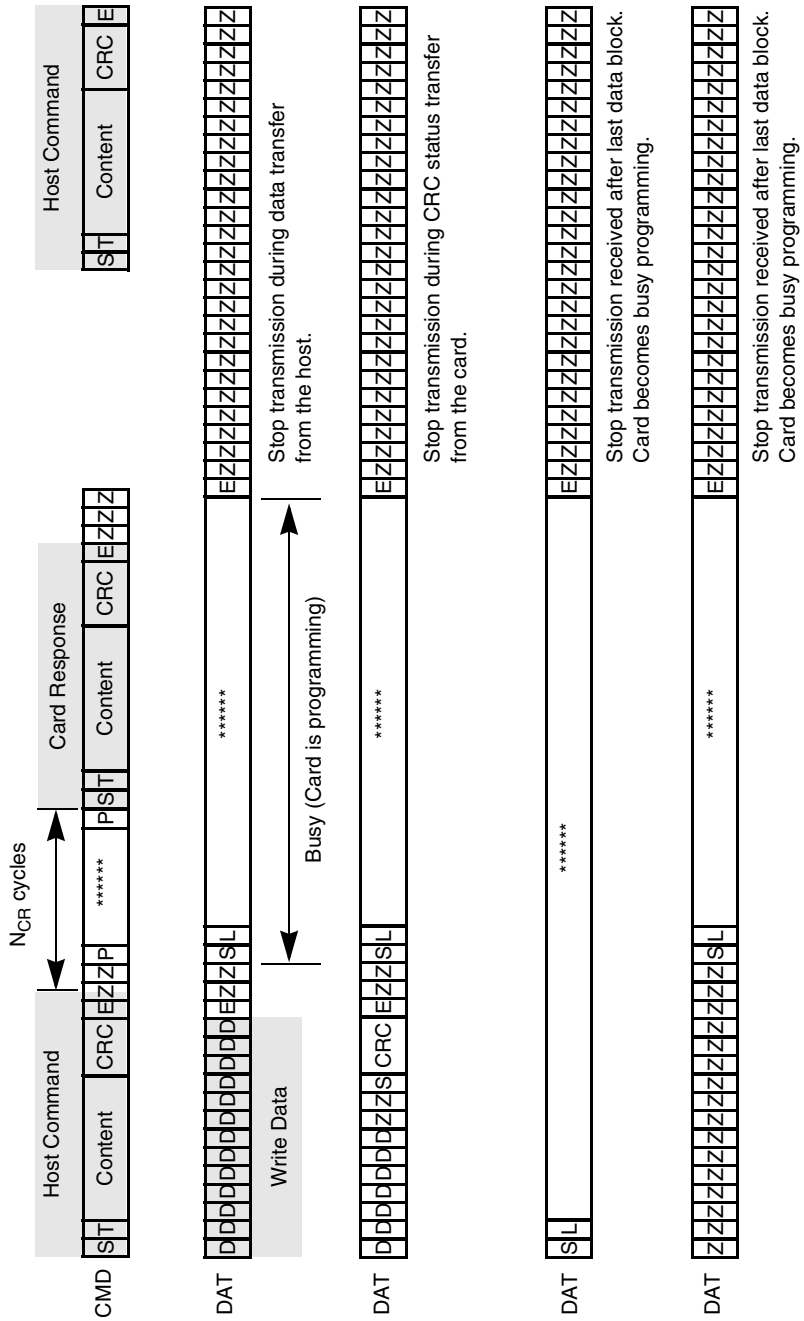


Figure 47. Stop Transmission During Different Scenarios

Table 24. Timing Values for Figure 43 through Figure 47

Parameter	Symbol	Minimum	Maximum	Unit
MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL)				
Command response cycle	NCR	2	64	Clock cycles
Identification response cycle	NID	5	5	Clock cycles
Access time delay cycle	NAC	2	TAAC + NSAC	Clock cycles

Table 25. MSHC Signal Timing Parameter Table (Continued)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	MS_SDIO output delay time[1,2]	–	3	ns
13	MS_SDIO input setup time for MS_SCLKO rising edge (RED bit = 0)[3]	18	–	ns
14	MS_SDIO input hold time for MS_SCLKO rising edge (RED bit = 0)[3]	0	–	ns
15	MS_SDIO input setup time for MS_SCLKO falling edge (RED bit = 1)[4]	23	–	ns
16	MS_SDIO input hold time for MS_SCLKO falling edge (RED bit = 1)[4]	0	–	ns

1 Loading capacitor condition is less than or equal to 30pF.

2 An external resistor (100 ~ 200 ohm) should be inserted in series to provide current control on the MS_SDIO pin, because of a possibility of signal conflict between the MS_SDIO pin and Memory Stick SDIO pin when the pin direction changes.

3 If the MSC2[RED] bit = 0, MSHC samples MS_SDIO input data at MS_SCLKO rising edge.

4 If the MSC2[RED] bit = 1, MSHC samples MS_SDIO input data at MS_SCLKO falling edge.

4.9 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin. Its timing diagram is shown in Figure 51 and the parameters are listed in Table 26.

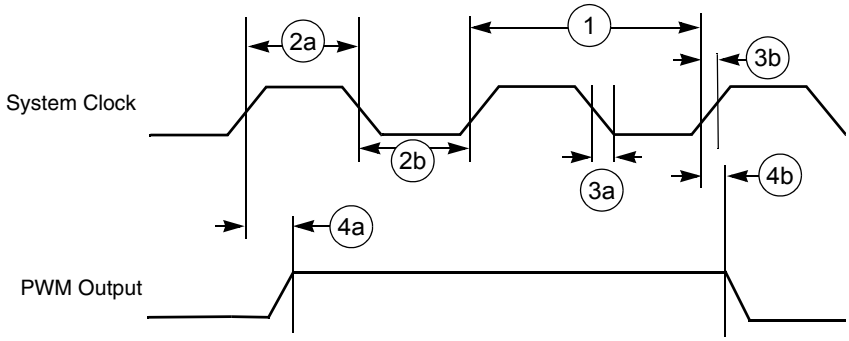


Figure 51. PWM Output Timing Diagram

Table 26. PWM Output Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	System CLK frequency[1]	0	87	0	100	MHz
2a	Clock high time[1]	3.3	–	5/10	–	ns
2b	Clock low time[1]	7.5	–	5/10	–	ns
3a	Clock fall time[1]	–	5	–	5/10	ns

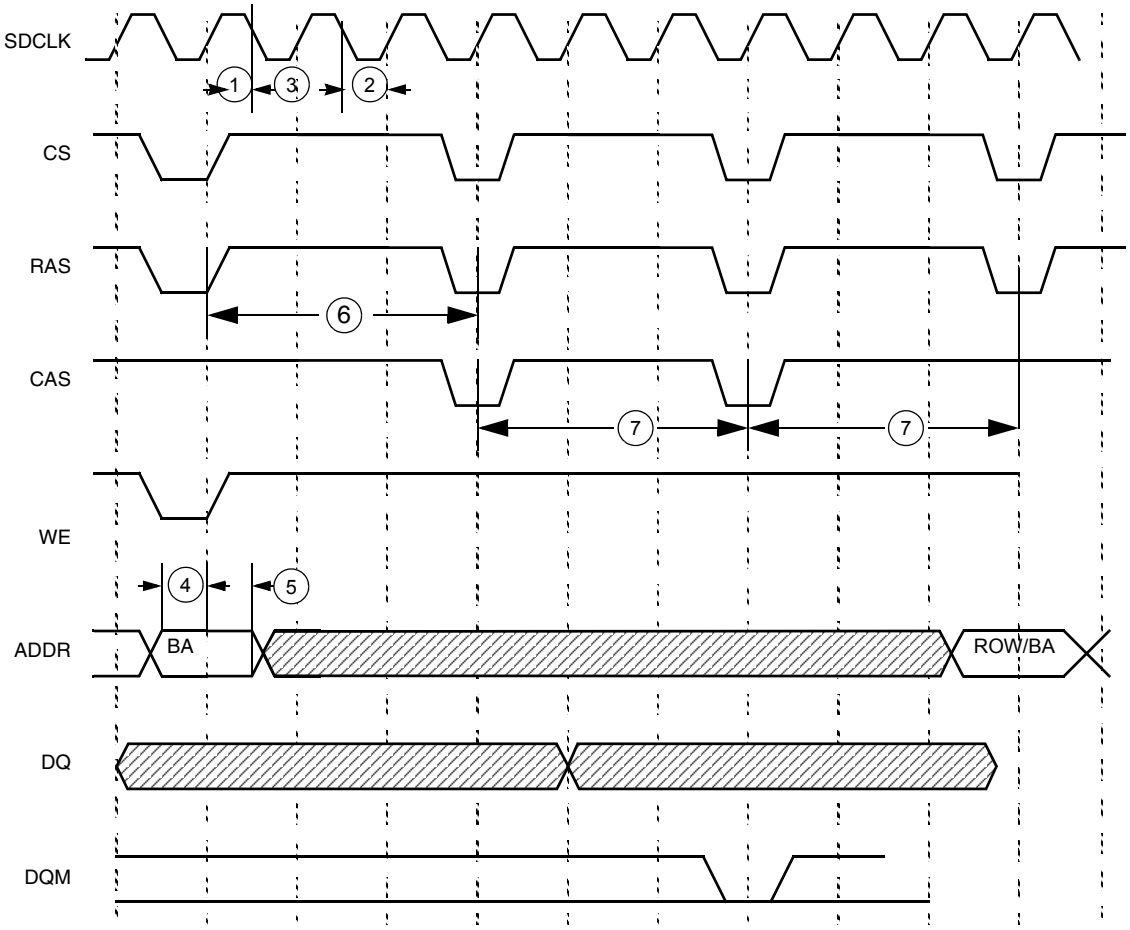


Figure 54. SDRAM Refresh Timing Diagram

Table 29. SDRAM Refresh Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period	t_{RP}[1]	–	t_{RP1}	–	ns
7	Auto precharge command period	t_{RC1}	–	t_{RC1}	–	ns

[1] t_{RP} and t_{RC} = SDRAM clock cycle time. These settings can be found in the *MC9328MXL reference manual*.

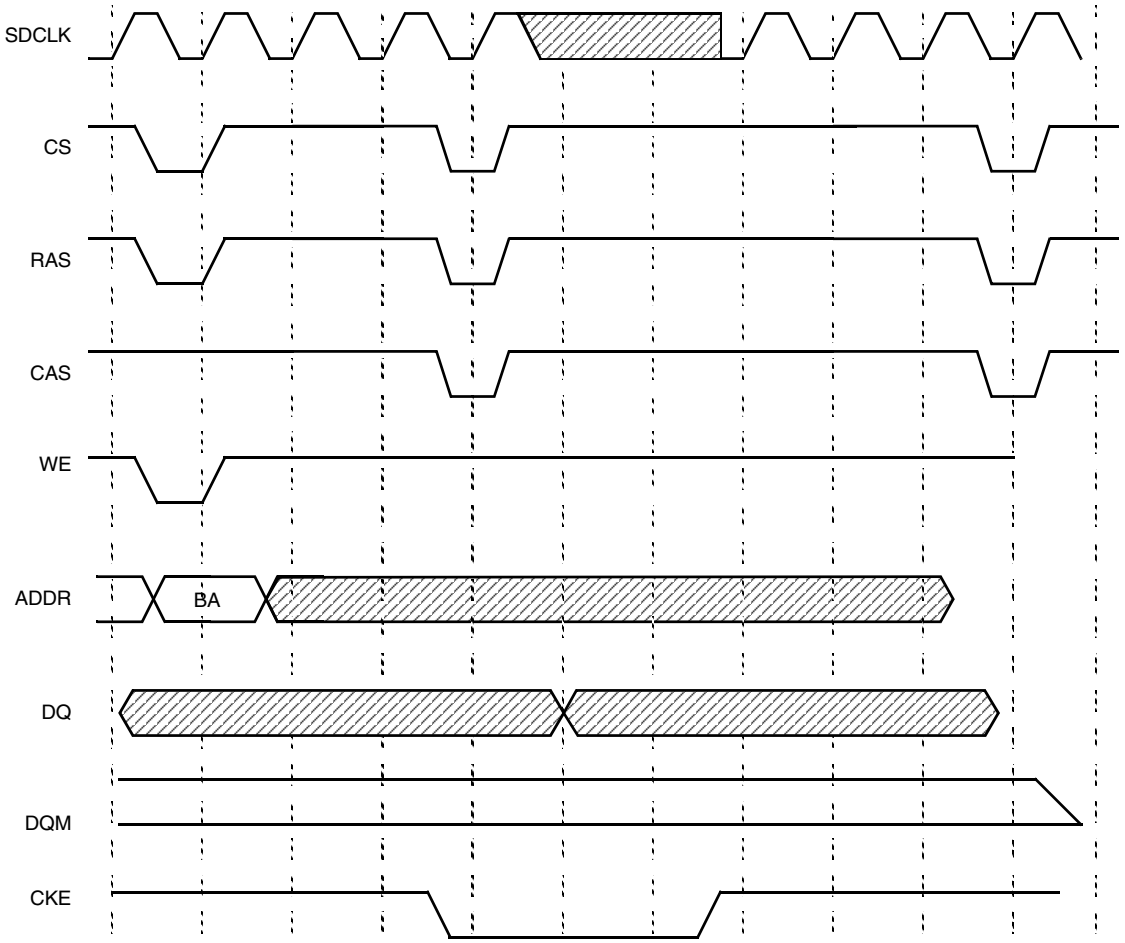


Figure 55. SDRAM Self-Refresh Cycle Timing Diagram

4.11 USB Device Port

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers, and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, however, because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

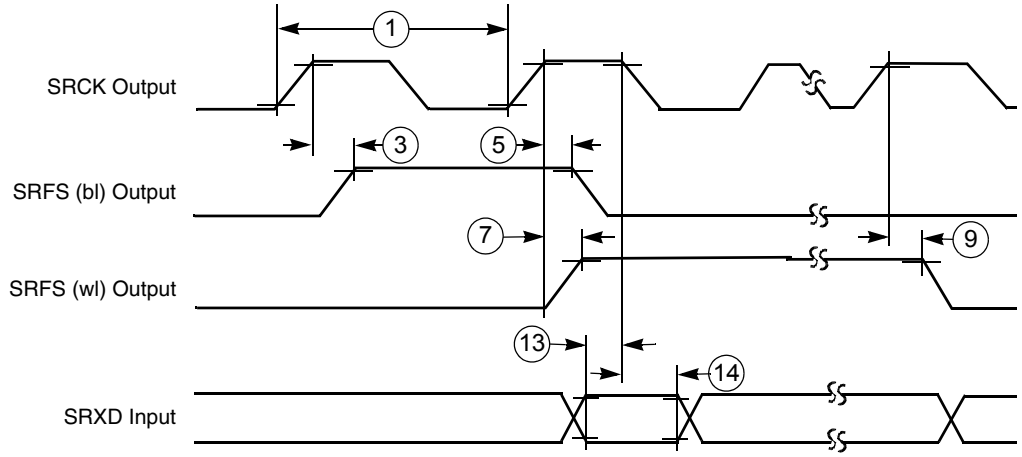
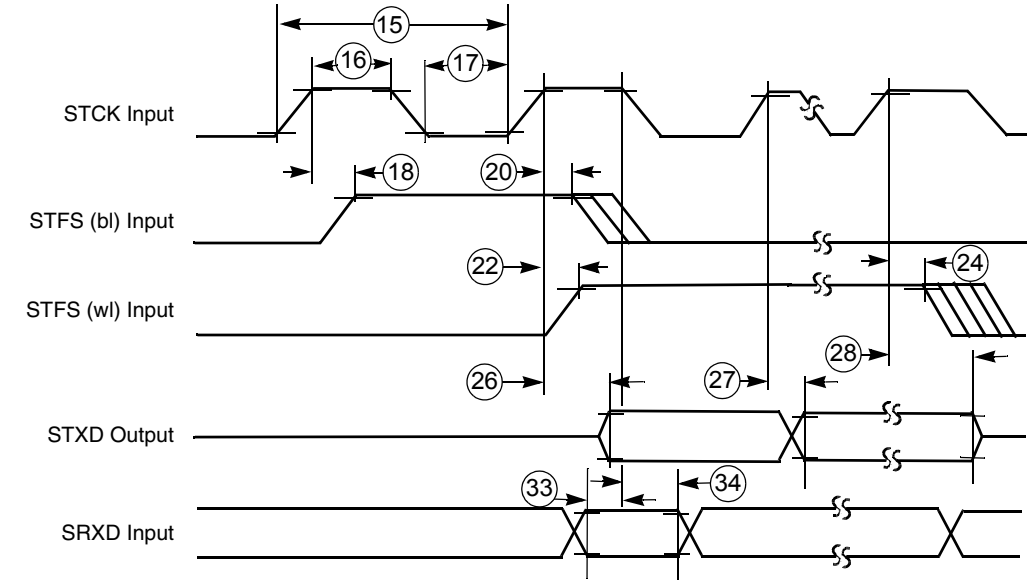


Figure 60. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 61. SSI Transmitter External Clock Timing Diagram

Table 33. SSI (Port C Primary Function) Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
18	STCK high to STFS (bl) high[3]	–	92.8	0	81.4	ns
19	SRCK high to SRFS (bl) high[3]	–	92.8	0	81.4	ns
20	STCK high to STFS (bl) low[3]	–	92.8	0	81.4	ns
21	SRCK high to SRFS (bl) low[3]	–	92.8	0	81.4	ns
22	STCK high to STFS (wl) high[3]	–	92.8	0	81.4	ns
23	SRCK high to SRFS (wl) high[3]	–	92.8	0	81.4	ns
24	STCK high to STFS (wl) low[3]	–	92.8	0	81.4	ns
25	SRCK high to SRFS (wl) low[3]	–	92.8	0	81.4	ns
26	STCK high to STXD valid from high impedance	18.01	28.16	15.8	24.7	ns
27a	STCK high to STXD high	8.98	18.13	7.0	15.9	ns
27b	STCK high to STXD low	9.12	18.24	8.0	16.0	ns
28	STCK high to STXD high impedance	18.47	28.5	16.2	25.0	ns
29	SRXD setup time before SRCK low	1.14	–	1.0	–	ns
30	SRXD hole time after SRCK low	0	–	0	–	ns
Synchronous Internal Clock Operation (Port C Primary Function[2])						
31	SRXD setup before STCK falling	15.4	–	13.5	–	ns
32	SRXD hold after STCK falling	0	–	0	–	ns
Synchronous External Clock Operation (Port C Primary Function[2])						
33	SRXD setup before STCK falling	1.14	–	1.0	–	ns
34	SRXD hold after STCK falling	0	–	0	–	ns

1 All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

2 There are 2 sets of I/O signals for the SSI module. They are from Port C primary function (pad 257 to pad 261) and Port B alternate function (pad 283 to pad 288). When SSI signals are configured as outputs, they can be viewed both at Port C primary function and Port B alternate function. When SSI signals are configured as input, the SSI module selects the input based on status of the FMCR register bits in the Clock controller module (CRM). By default, the input are selected from Port C primary function.

3 bl = bit length; wl = word length.

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

4.14.2 Non-Gated Clock Mode

Figure 65 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 66 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 36.

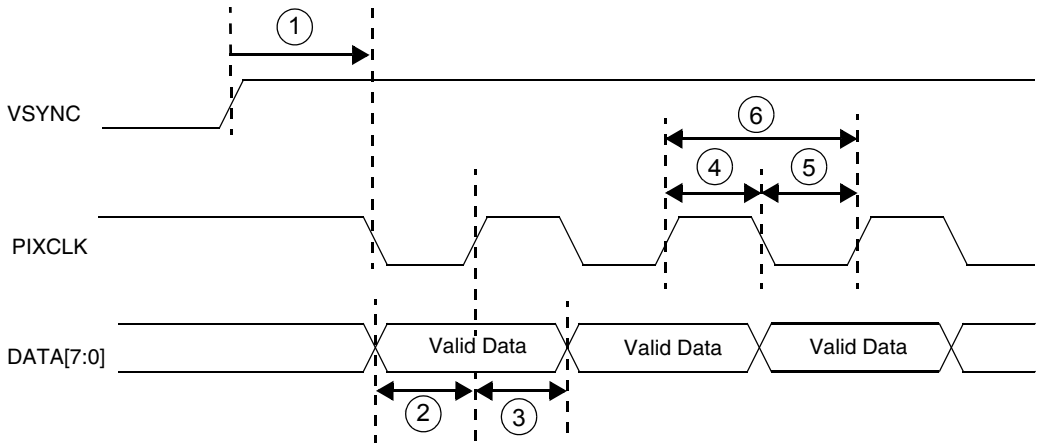


Figure 65. Sensor Output Data on Pixel Clock Falling Edge
CSI Latches Data on Pixel Clock Rising Edge

5 Pin-Out and Package Information

Table 37 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 9.

Table 37. i.MXL 256 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NVSS	SD_DAT3	SD_CLK	NVSS	USBD_ AFE	NVDD4	NVSS	UART1_ RTS	UART1_ RXD	NVDD3	N.C.	N.C.	QVDD4	N.C.	N.C.	N.C.	A
B	A24	SD_DAT1	SD_CMD	PB16	USBD_ ROE	USBD_VP	SSI_ RXCLK	SSI_ TXCLK	SPI1_ SCLK	N.C.	N.C.	N.C.	QVSS	N.C.	N.C.	N.C.	B
C	A23	D31	SD_DAT0	PB15	USBD_ RCV	UART2_ CTS	UART2_ RXD	SSI_ RXFS	UART1_ TXD	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	C
D	A22	D30	D29	PB14	USBD_ SUSPND	USBD_ VPO	USBD_ VMO	SSI_ RXDAT	SPI1_ SPI_RDY	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	D
E	A20	A21	D28	D26	SD_DAT2	USBD_VM	UART2_ RTS	SSI_ TXDAT	SPI1_SS	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	E
F	A18	D27	D25	A19	A16	PB18	UART2_ TXD	SSI_ TXFS	SPI1_ MISO	N.C.	N.C.	REV	N.C.	N.C.	LSCLK	SPL_SPR	F
G	A15	A17	D24	D23	D21	PB17	PB19	UART1_ CTS	SPI1_ MOSI	N.C.	CLS	CONTRAST	ACD/OE	LP/ HSYNC	FLM/ VSYNC	LD1	G
H	A13	D22	A14	D20	NVDD1	NVDD1	NVSS	QVSS	QVDD1	PS	LD0	LD2	LD4	LD5	LD9	LD3	H
J	A12	A11	D18	D19	NVDD1	NVDD1	NVSS	NVDD1	NVSS	NVSS	LD6	LD7	LD8	LD11	QVDD3	QVSS	J
K	A10	D16	A9	D17	NVDD1	NVSS	NVSS	NVDD1	NVDD2	NVDD2	LD10	LD12	LD13	LD14	TMR2OUT	LD15	K
L	A8	A7	D13	D15	D14	NVDD1	NVSS	CAS	TCK	TIN	PWMO	CSI_MCLK	CSI_D0	CSI_D1	CSI_D2	CSI_D3	L
M	A5	D12	D11	A6	SDCLK	NVSS	RW	MA10	RAS	RESET_IN	BIG_ ENDIAN	CSI_D4	CSI_ HSYNC	CSI_VSYNC	CSI_D6	CSI_D5	M
N	A4	EB1	D10	D7	A0	D4	PA17	D1	DQM1	RESET_SF[1]	RESET_ OUT	BOOT2	CSI_ PIXCLK	CSI_D7	TMS	TDI	N
P	A3	D9	EB0	CS3	D6	ECB	D2	D3	DQM3	SDCKE1	BOOT3	BOOT0	TRST	I2C_SCL	I2C_SDA	XTAL32K	P
R	EB2	EB3	A1	CS4	D8	D5	LBA	BCLK[2]	D0	DQM0	SDCKE0	POR	BOOT1	TDO	QVDD2	EXTAL32K	R
T	NVSS	A2	OE	CS5	CS2	CS1	CS0	MA11	DQM2	SDWE	CLKO	AVDD1	TRISTATE	EXTAL16M	XTAL16M	QVSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1 This signal is not used and should be floated in an actual application.

2 burst clock

6 Product Documentation

6.1 Revision History

Table 39 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 39. i.MXL Data Sheet Revision History Rev. 8

Location	Revision
Table 2 on page 4 Signal Names and Descriptions	• Added the DMA_REQ signal to table. • Corrected signal name from $\overline{\text{USBD\_OE}}$ to $\overline{\text{USBD\_ROE}}$
Table 3 on page 9 Signal Multiplex Table i.MXL	Added Signal Multiplex table from Reference Manual with the following changes: • Changed I/O Supply Voltage,PB31–20, from NVDD3 to NVDD4 • Added 225 BGA column. • Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 21	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 9	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

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