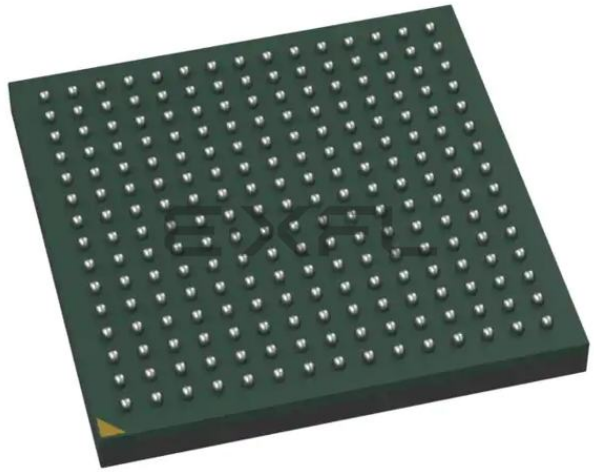

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	-30°C ~ 70°C (TA)
Security Features	-
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxldvp20

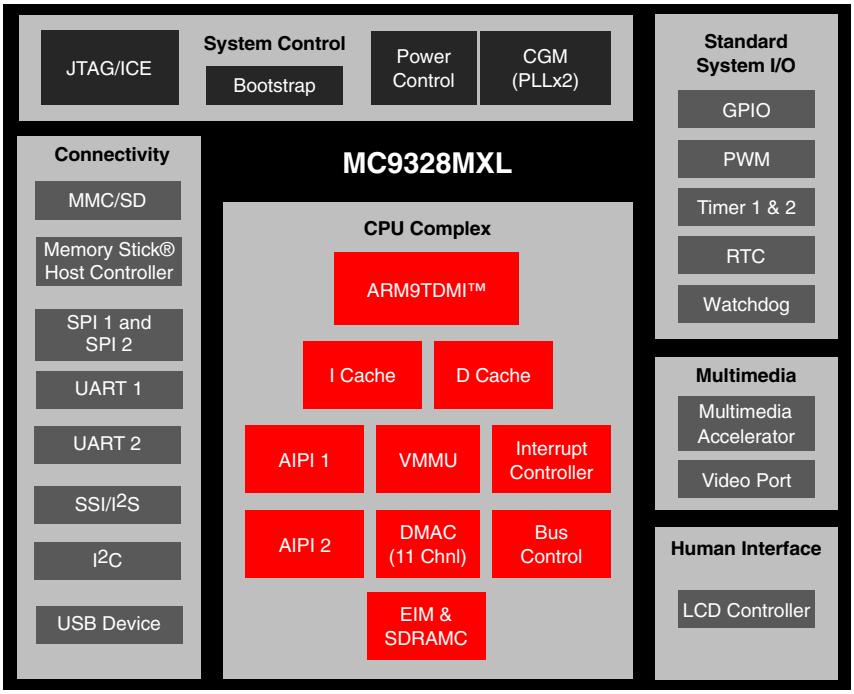


Figure 1. i.MXL Functional Block Diagram

1.1 Features

To support a wide variety of applications, the processor offers a robust array of features, including the following:

- ARM920T™ Microprocessor Core
- AHB to IP Bus Interfaces (AIPIs)
- External Interface Module (EIM)
- SDRAM Controller (SDRAMC)
- DPLL Clock and Power Control Module
- Two Universal Asynchronous Receiver/Transmitters (UART 1 and UART 2)
- Serial Peripheral Interface (SPI)
- Two General-Purpose 32-bit Counters/Timers
- Watchdog Timer
- Real-Time Clock/Sampling Timer (RTC)
- LCD Controller (LCDC)
- Pulse-Width Modulation (PWM) Module
- Universal Serial Bus (USB) Device
- Multimedia Card and Secure Digital (MMC/SD) Host Controller Module
- Memory Stick® Host Controller (MSHC)
- Direct Memory Access Controller (DMAC)
- Synchronous Serial Interface and an Inter-IC Sound (SSI/I^2S) Module
- Inter-IC (I^2C) Bus Module

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD2	H13	N13	CSI_PIXCLK	I				PA14	69K				PA14
NVDD2	G14	M13	CSI_HSYNC	I				PA13	69K				PA13
NVDD2	H12	M14	CSI_VSYNC	I				PA12	69K				PA12
NVDD2	G13	N14	CSI_D7	I				PA11	69K				PA11
NVDD2	J10	M15	CSI_D6	I				PA10	69K				PA10
NVDD2	G15	M16	CSI_D5	I				PA9	69K				PA9
NVDD2	F15	M12	CSI_D4	I				PA8	69K				PA8
NVDD2	G12	L16	CSI_D3	I				PA7	69K				PA7
NVDD2	F14	L15	CSI_D2	I				PA6	69K				PA6
NVDD2	H11	L14	CSI_D1	I				PA5	69K				PA5
NVDD2	E14	L13	CSI_D0	I				PA4	69K				PA4
NVDD2	E15	L12	CSI_MCLK	O				PA3	69K				PA3
NVDD2	G11	L11	PWMO	O				PA2	69K				PA2
NVDD2	E13	L10	TIN	I				PA1	69K			SPI2_RXD_0	PA1
NVDD2	D14	K15	TMR2OUT	O				PD31	69K		SPI2_TXD		PD31
NVDD2	F13	K16	LD15	O				PD30	69K				PD30
NVDD2	F12	K14	LD14	O				PD29	69K				PD29
NVDD2	D15	K13	LD13	O				PD28	69K				PD28
NVDD2	C14	K12	LD12	O				PD27	69K				PD27
NVDD2	D13	J14	LD11	O				PD26	69K				PD26
NVDD2	E12	K11	LD10	O				PD25	69K				PD25
NVDD2	C13	H15	LD9	O				PD24	69K				PD24
NVDD2	C12	J13	LD8	O				PD23	69K				PD23
NVDD2	B15	J12	LD7	O				PD22	69K				PD22
NVDD2	B14	J11	LD6	O				PD21	69K				PD21
NVDD2	A15	H14	LD5	O				PD20	69K				PD20
NVDD2	A14	H13	LD4	O				PD19	69K				PD19
NVDD2	B13	H16	LD3	O				PD18	69K				PD18
NVDD2	A13	H12	LD2	O				PD17	69K				PD17
NVDD2	D12	G16	LD1	O				PD16	69K				PD16
NVDD2	B12	H11	LD0	O				PD15	69K				PD15
NVDD2	C11	G15	FLM/VSYNC	O				PD14	69K				PD14

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD1	F5	J5	NVDD	Static									
	J6	K6	NVSS	Static									
NVDD1	G5	K5	NVDD1	Static									
	K6	M6	NVSS	Static									
NVDD1	J5	H6	NVDD1	Static									
	H7	J7	NVSS	Static									
NVDD1	K5	L6	NVDD1	Static									
	J7	J7	NVSS	Static									
NVDD1	L5	L6	NVDD1	Static									
	G8	K7	NVSS	Static									
NVDD1	L5	J8	NVDD1	Static									
	H8	L7	NVSS	Static									
	K7	T16	QVSS	Static									
NVDD2	H10	K10	NVDD2	Static									
	G9	J10	NVSS	Static									
QVDD3	F11	J15	QVDD3	Static									
	G10	J16	QVSS	Static									
NVDD2	C15	K9	NVDD2	Static									
	H9	J9	NVSS	Static									
QVDD4	D7	A13	QVDD4	Static									
	L13	B13	QVSS	Static									
NVDD3	D9	A10	NVDD3	Static									
	J9	A7	NVSS	Static									
	K9	A4	NVSS	Static									
NVDD4	G7	A6	NVDD4	Static									
NVDD1	F6		NVDD1	Static									
NVDD1	L6		NVDD1	Static									
NVDD1	M6		NVDD1	Static									
NVDD1	K8		NVDD1	Static									
	L10		NVSS	Static									
	L11		NVSS	Static									
	M11		NVSS	Static									

1 Pull down this input with 1KΩ resistor to GND.

2 External circuit required to drive this input.

3 Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

4 Pull up this output with a resistor to NVDD2.

Table 6. Maximum and Minimum DC Characteristics (Continued)

Number or Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	Input high voltage	$0.7V_{DD}$	–	Vdd+0.2	V
V_{IL}	Input low voltage	–	–	0.4	V
V_{OH}	Output high voltage (I_{OH} = 2.0 mA)	$0.7V_{DD}$	–	Vdd	V
V_{OL}	Output low voltage (I_{OL} = -2.5 mA)	–	–	0.4	V
I_{IL}	Input low leakage current (V_{IN} = GND, no pull-up or pull-down)	–	–	±1	µA
I_{IH}	Input high leakage current (V_{IN} = V_{DD}, no pull-up or pull-down)	–	–	±1	µA
I_{OH}	Output high current (V_{OH} = $0.8V_{DD}$, V_{DD} = 1.8V)	4.0	–	–	mA
I_{OL}	Output low current (V_{OL} = 0.4V, V_{DD} = 1.8V)	-4.0	–	–	mA
I_{OZ}	Output leakage current (V_{out} = V_{DD}, output is high impedance)	–	–	±5	µA
C_i	Input capacitance	–	–	5	pF
C_o	Output capacitance	–	–	5	pF

3.5 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency from 0 MHz to 96 MHz (core operating frequency 150 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from T_L to T_H. All timing is measured at 30 pF loading.

Table 7. Tristate Signal Timing

Pin	Parameter	Minimum	Maximum	Unit
TRISTATE	Time from TRISTATE activate until I/O becomes Hi-Z	–	20.8	ns

Table 8. 32k/16M Oscillator Signal Timing

Parameter	Minimum	RMS	Maximum	Unit
EXTAL32k input jitter (peak to peak)	–	5	20	ns
EXTAL32k startup time	800	–	–	ms
EXTAL16M input jitter (peak to peak) [1]	–	TBD	TBD	–
EXTAL16M startup time [1]	TBD	–	–	–

[1] The 16 MHz oscillator is not recommended for use in new designs.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXL.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

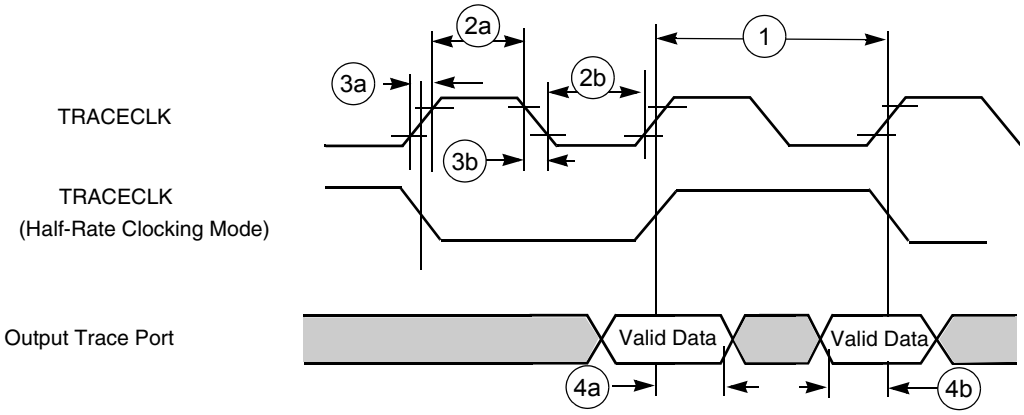


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns

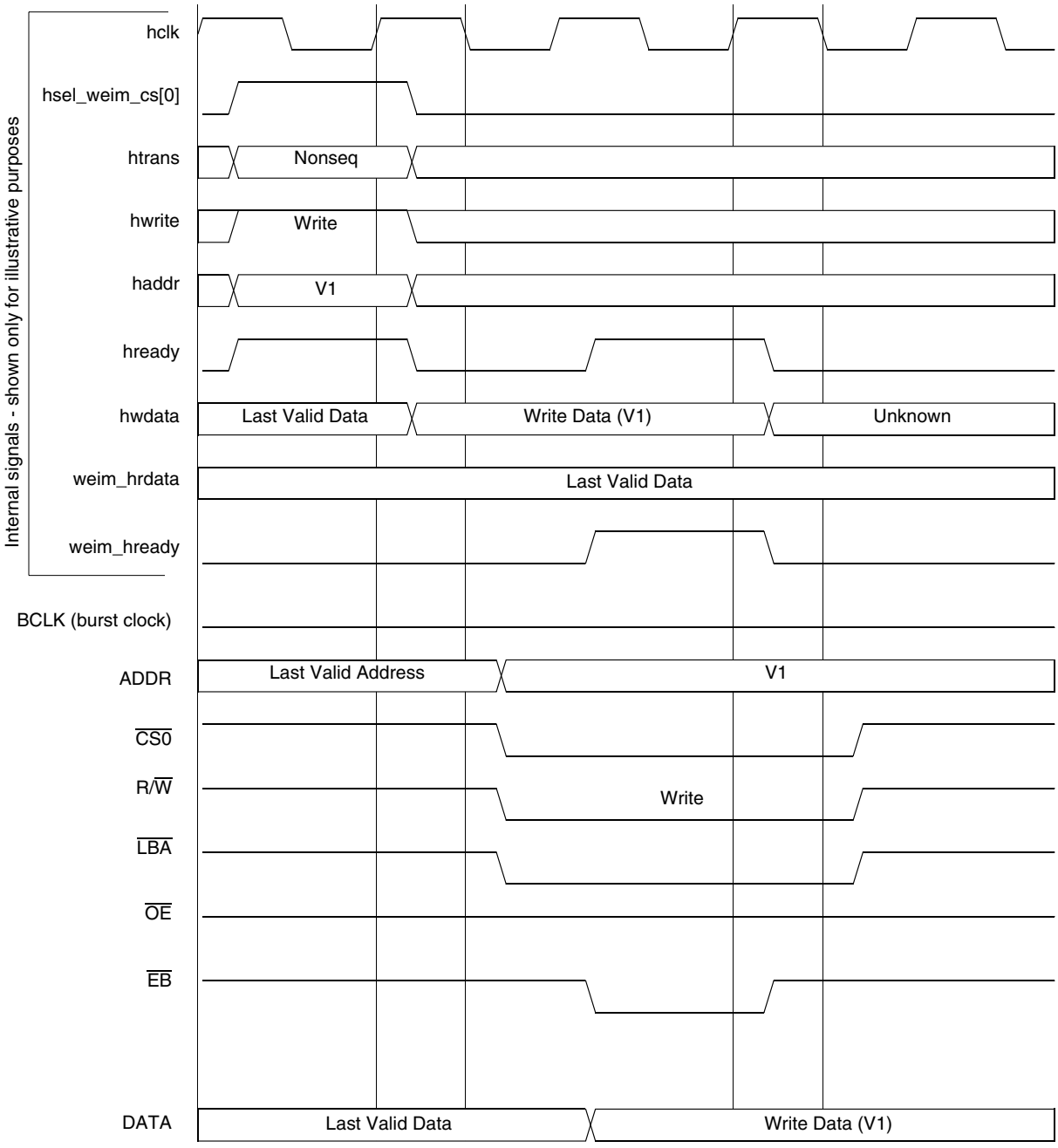
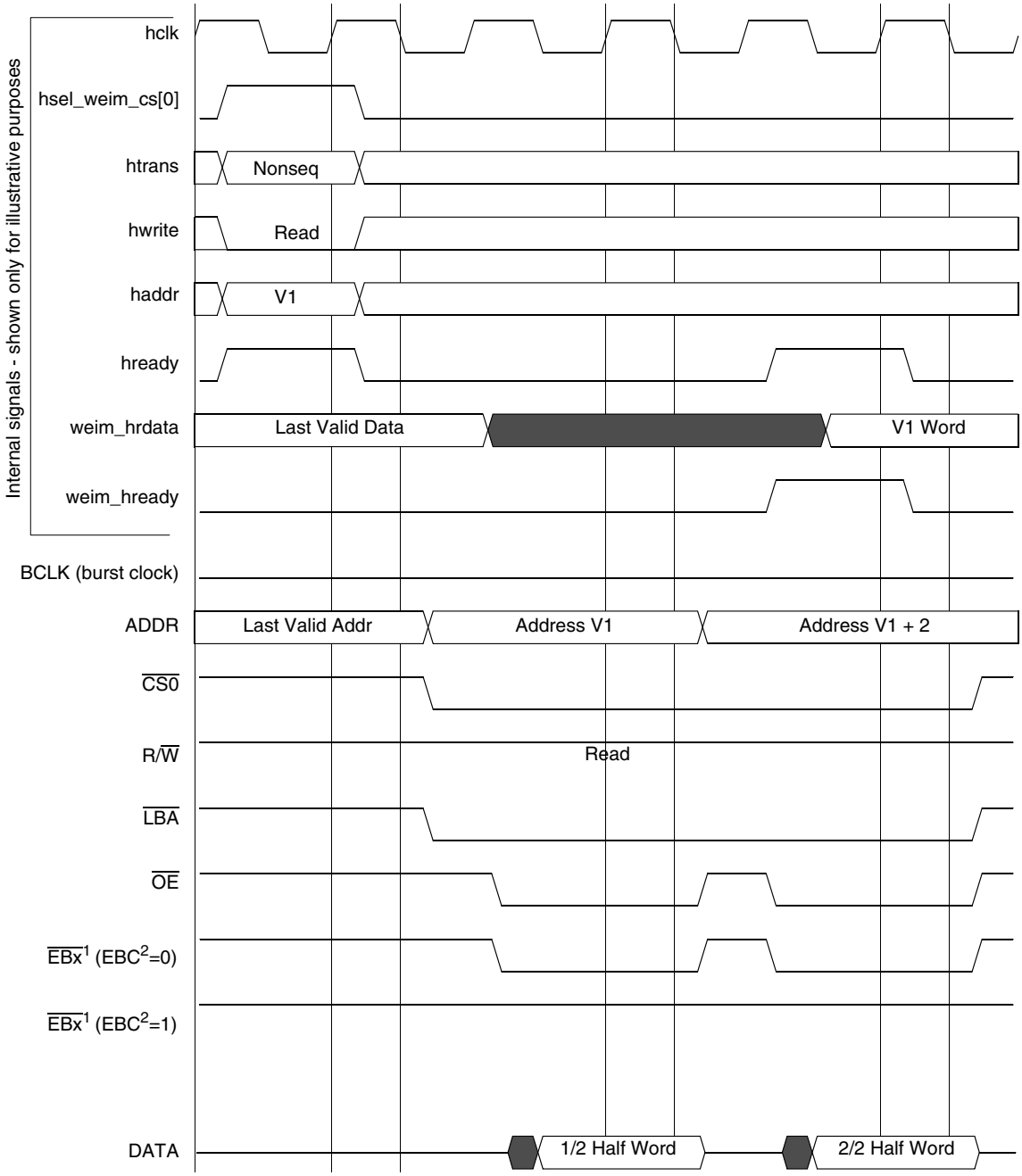
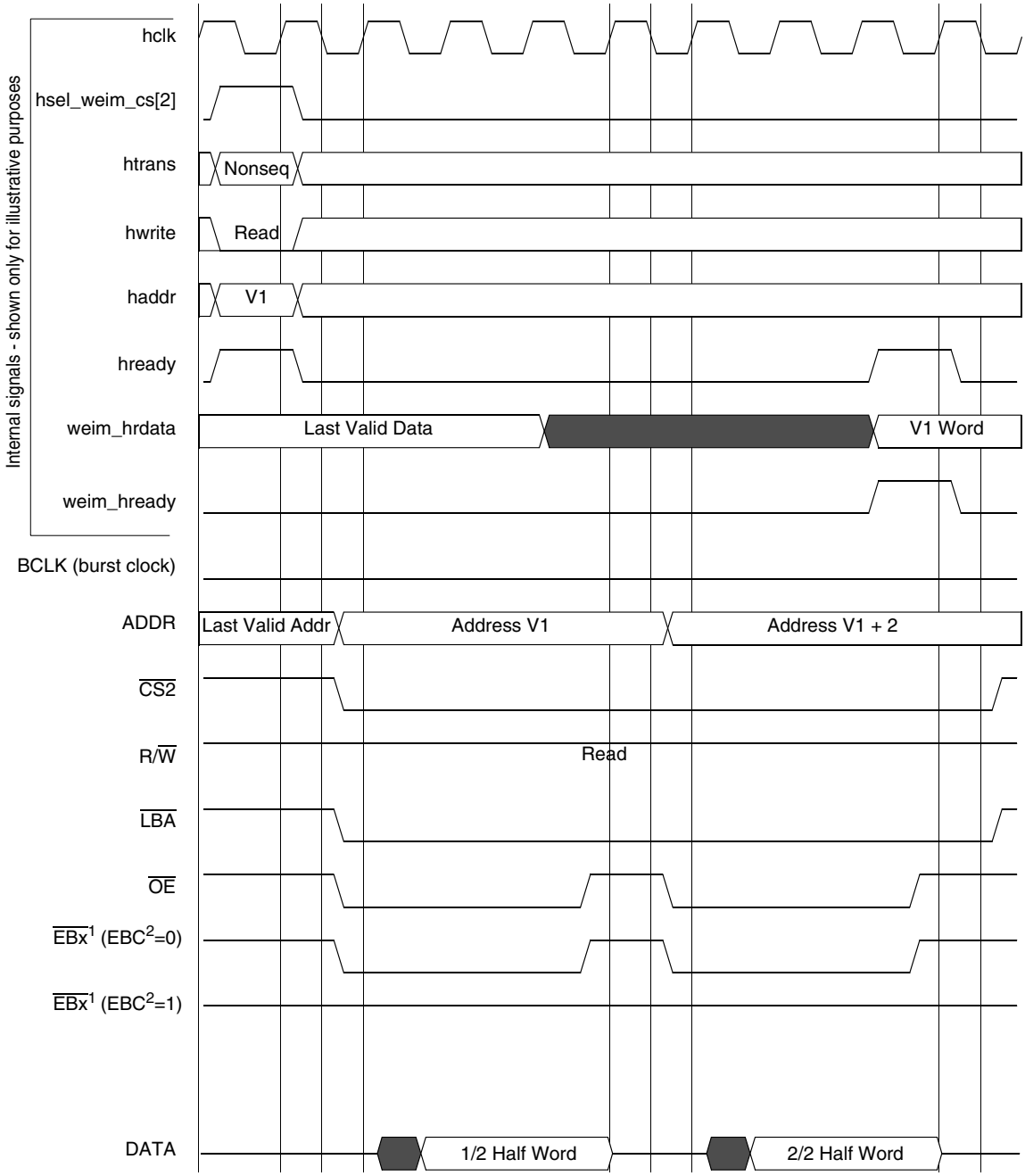


Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 12. WSC = 1, OEA = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF

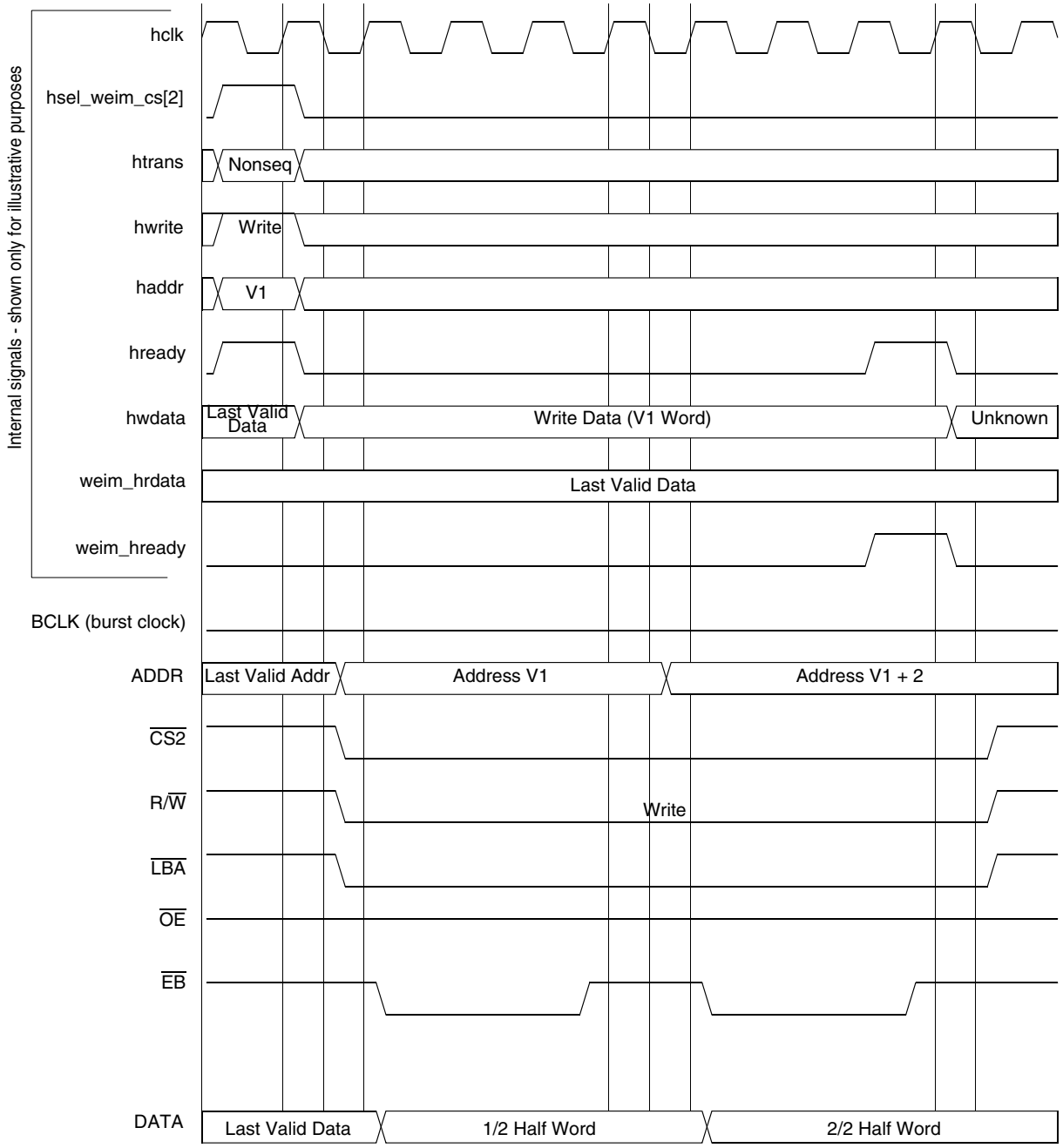
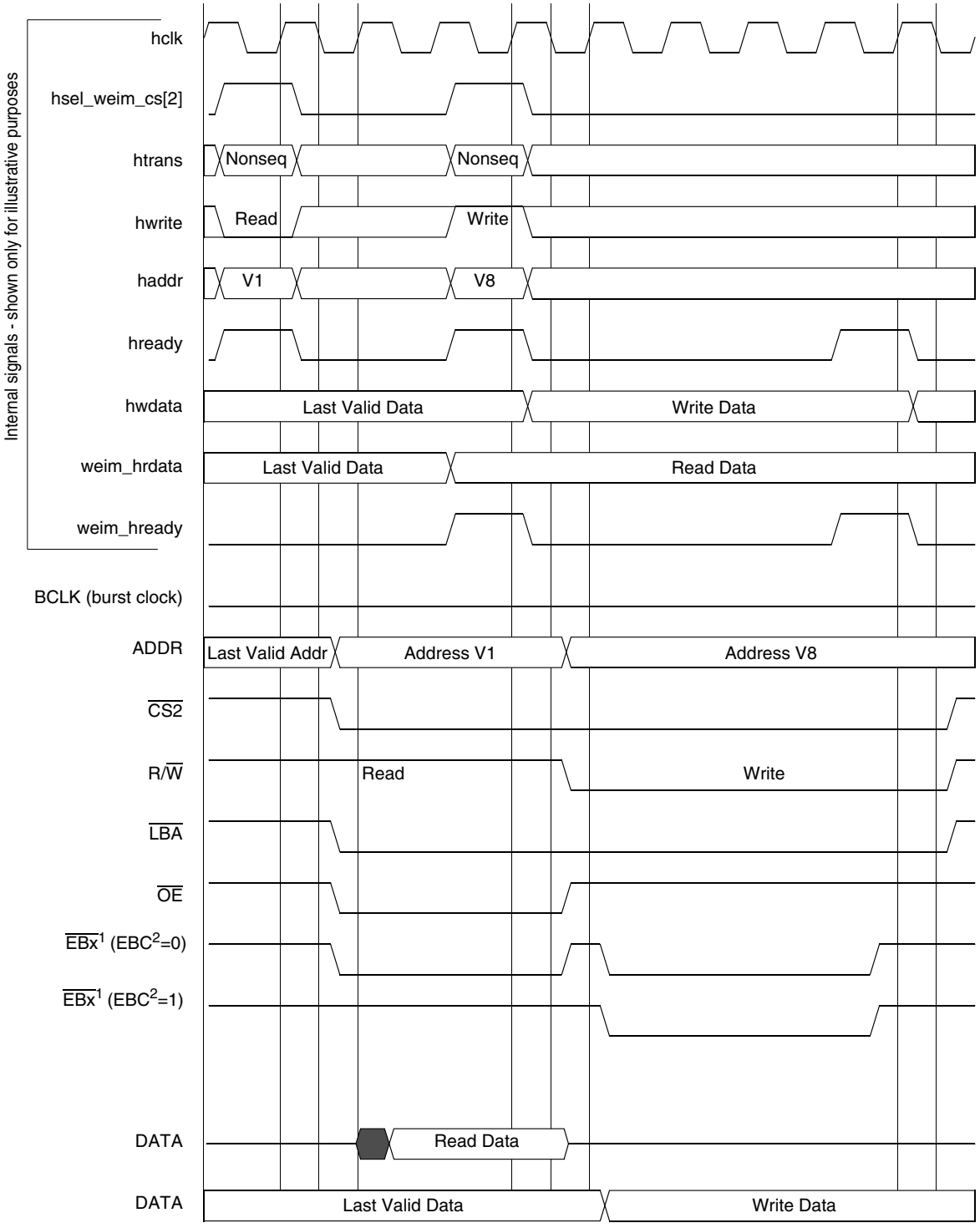
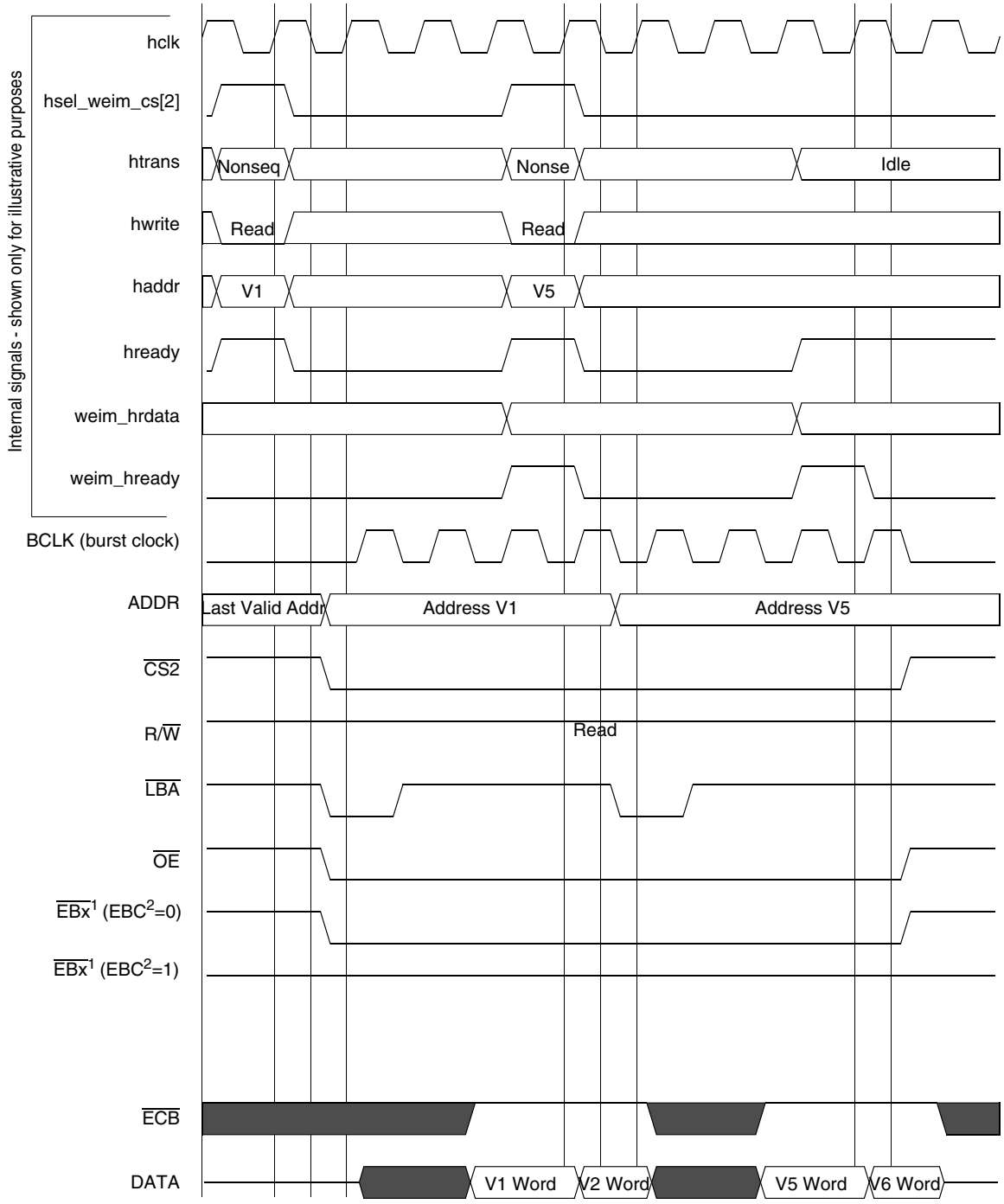


Figure 20. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF



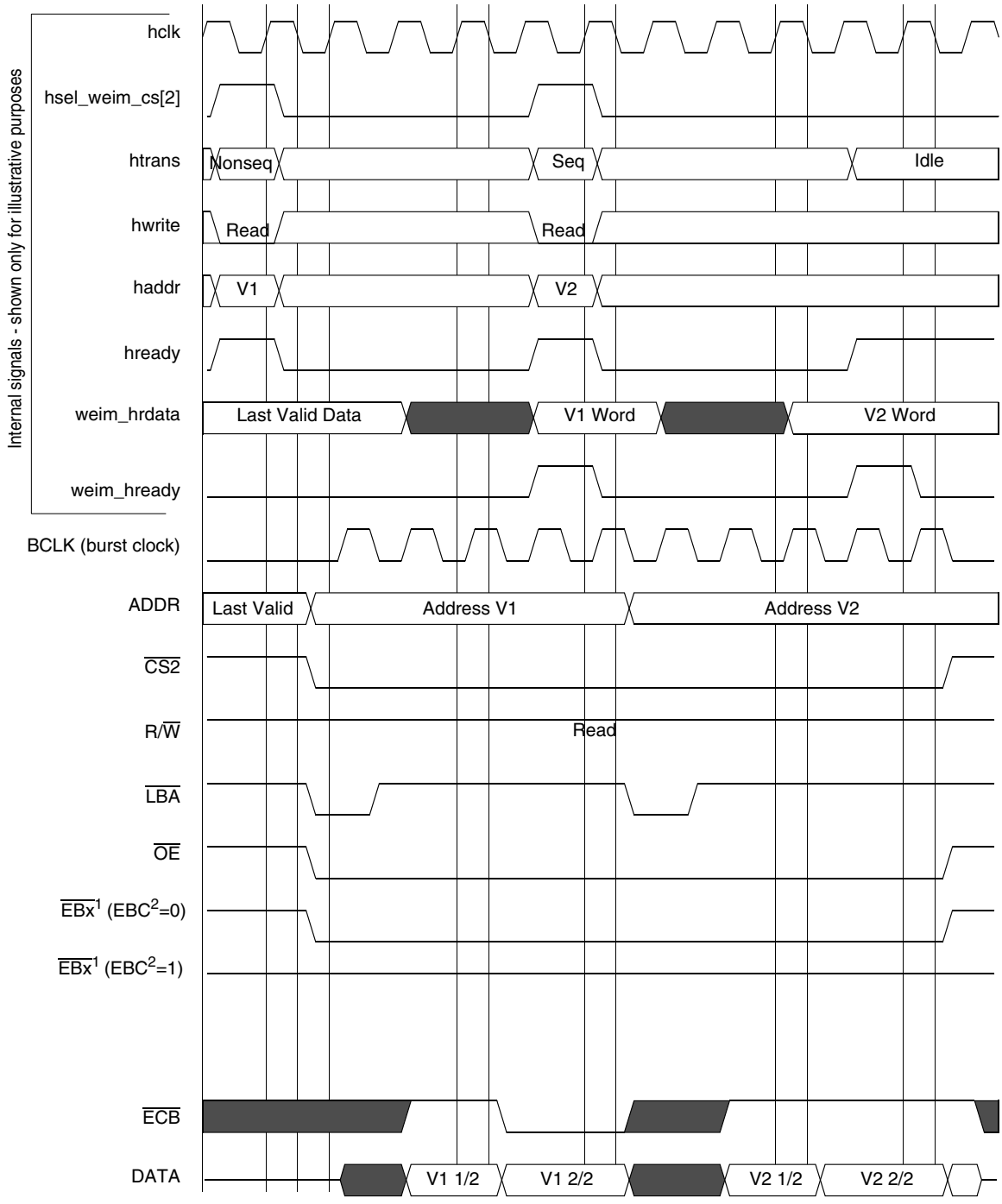
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

4.4.4 Non-TFT Panel Timing

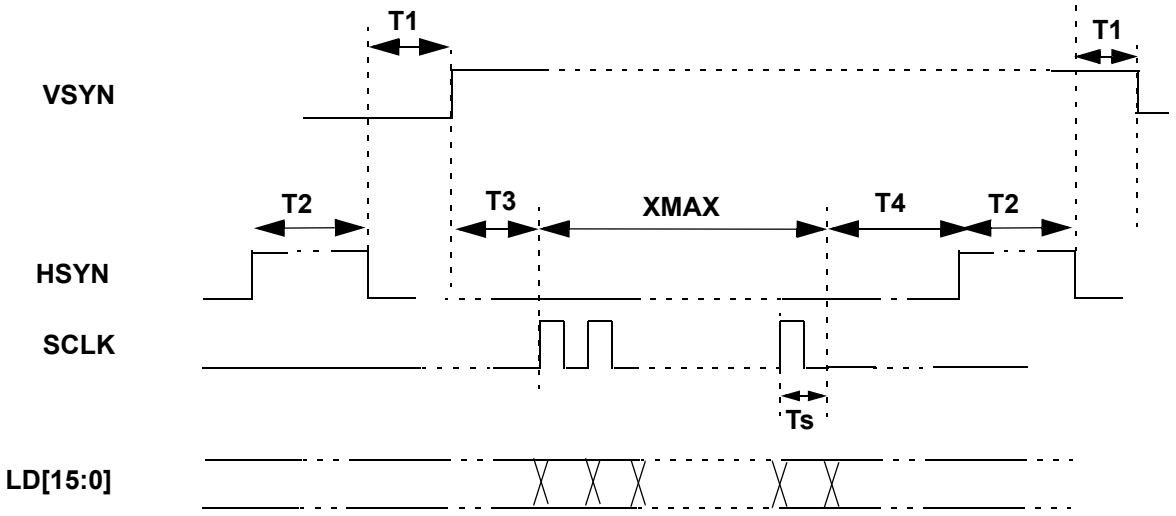


Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

Symbol	Parameter	Allowed Register Minimum Value[1, 2]	Actual Value	Unit
T1	HSYN to VSYN delay[3]	0	HWAIT2+2	Tpix[4]
T2	HSYN pulse width	0	HWIDTH+1	Tpix
T3	VSYN to SCLK	–	0 ≤ T3 ≤ Ts[5]	–
T4	SCLK to HSYN	0	HWAIT1+1	Tpix

1 Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.

2 Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

3 VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.

4 Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).

5 Ts is the shift clock period. Ts = Tpix * (panel data bus width).

4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) and the SPI2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

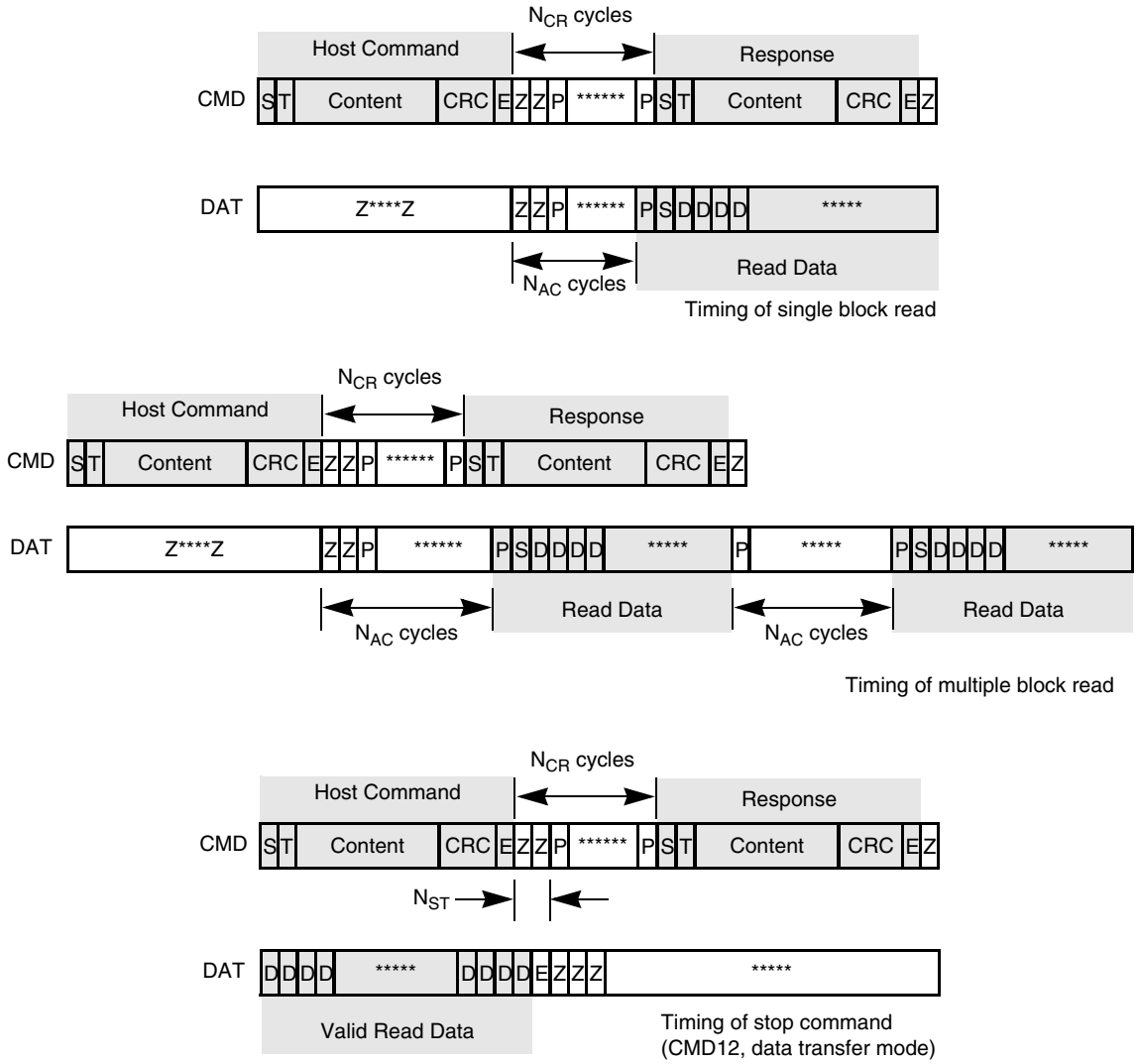


Figure 45. Timing Diagrams at Data Read

Figure 46 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

Table 24. Timing Values for Figure 43 through Figure 47 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]				

4.7.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the “Interrupt Period” during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

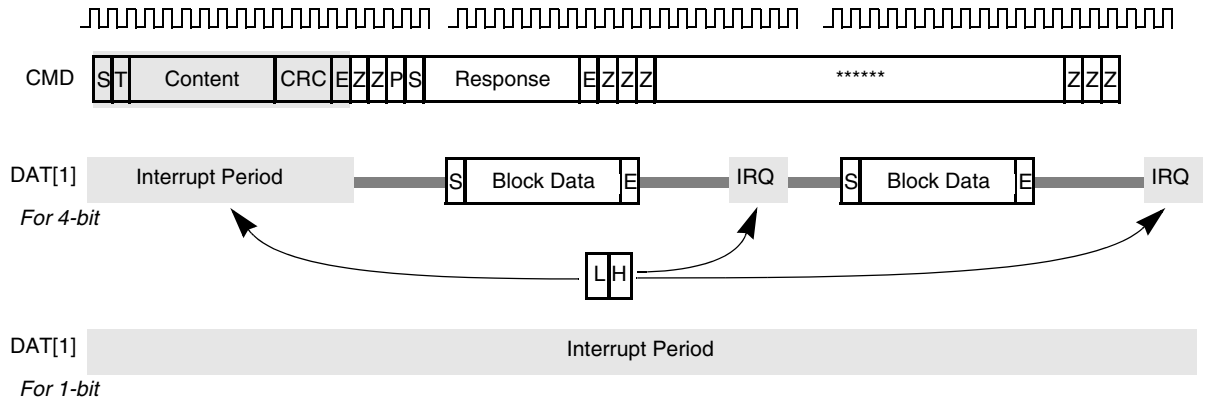


Figure 48. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

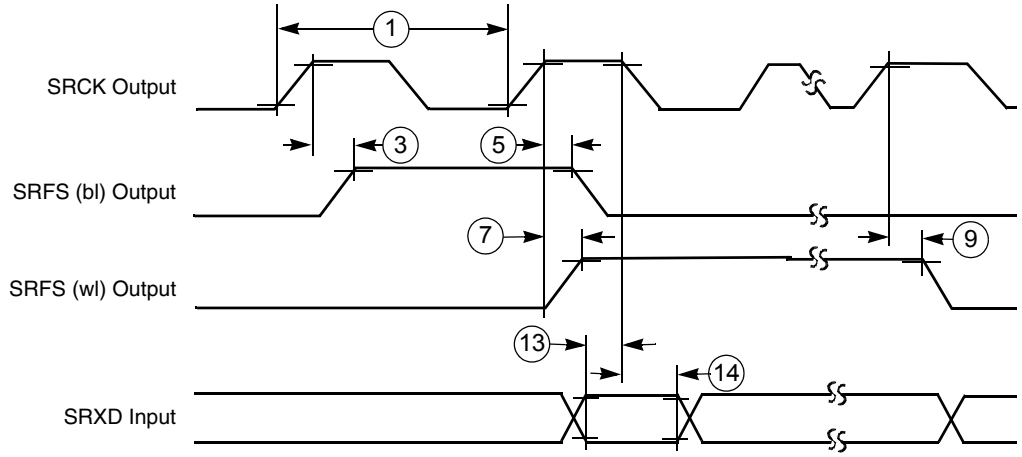
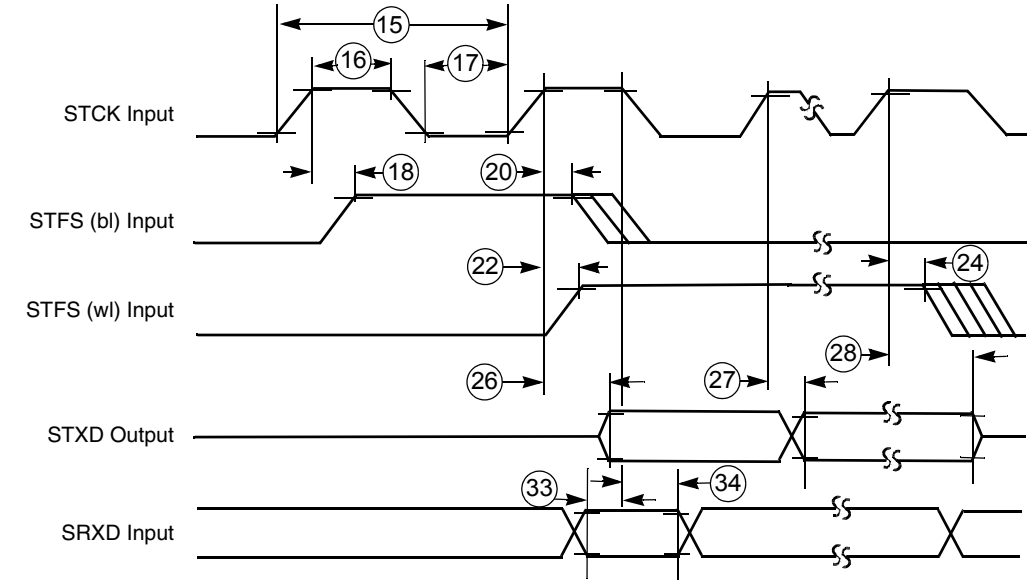


Figure 60. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 61. SSI Transmitter External Clock Timing Diagram

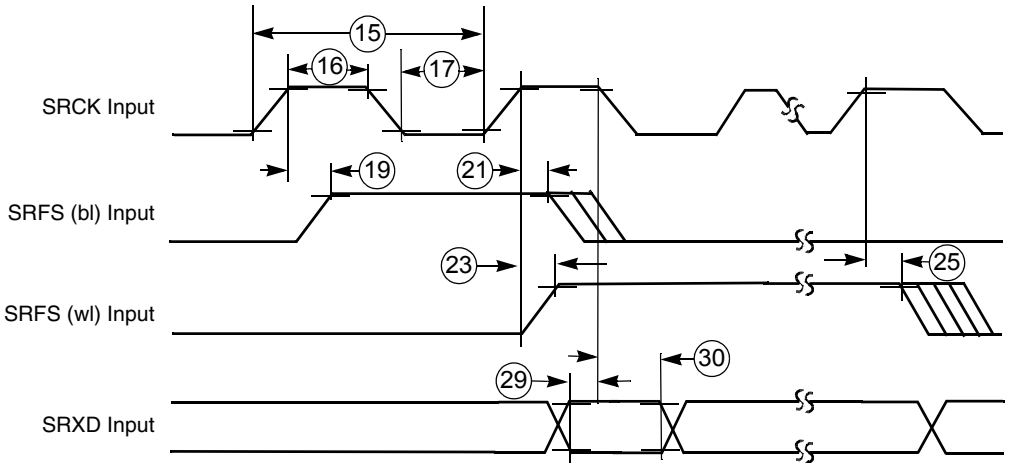


Figure 62. SSI Receiver External Clock Timing Diagram

Table 33. SSI (Port C Primary Function) Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
Internal Clock Operation[1] (Port C Primary Function[2])						
1	STCK/SRCK clock period[1]	95	–	83.3	–	ns
2	STCK high to STFS (bl) high[3]	1.5	4.5	1.3	3.9	ns
3	SRCK high to SRFS (bl) high[3]	-1.2	-1.7	-1.1	-1.5	ns
4	STCK high to STFS (bl) low[3]	2.5	4.3	2.2	3.8	ns
5	SRCK high to SRFS (bl) low[3]	0.1	-0.8	0.1	-0.8	ns
6	STCK high to STFS (wl) high[3]	1.48	4.45	1.3	3.9	ns
7	SRCK high to SRFS (wl) high[3]	-1.1	-1.5	-1.1	-1.5	ns
8	STCK high to STFS (wl) low[3]	2.51	4.33	2.2	3.8	ns
9	SRCK high to SRFS (wl) low[3]	0.1	-0.8	0.1	-0.8	ns
10	STCK high to STXD valid from high impedance	14.25	15.73	12.5	13.8	ns
11a	STCK high to STXD high	0.91	3.08	0.8	2.7	ns
11b	STCK high to STXD low	0.57	3.19	0.5	2.8	ns
12	STCK high to STXD high impedance	12.88	13.57	11.3	11.9	ns
13	SRXD setup time before SRCK low	21.1	–	18.5	–	ns
14	SRXD hold time after SRCK low	0	–	0	–	ns
External Clock Operation (Port C Primary Function[2])						
15	STCK/SRCK clock period[1]	92.8	–	81.4	–	ns
16	STCK/SRCK clock high period	27.1	–	40.7	–	ns
17	STCK/SRCK clock low period	61.1	–	40.7	–	ns

Table 38 illustrates the package pin assignments for the 225-contact MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 9.

Table 38. i.MXL 225 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	SD_CMD	PB15	PB19	USBD_ROE	USBD_SUSPND	USBD_VM	SSI_RXFS	SSI_TXCLK	SPI1_SPI_RDY	SPI1_SCLK	REV	PS	LD2	LD4	LD5	**A**
B	SD_DAT3	SD_CLK	PB16	USBD_AFE	USBD_RCV	USBD_VMO	SSI_RXDAT	UART1_TXD	SPI1_SS	LSCLK	SPL_SPR	LD0	LD3	LD6	LD7	**B**
C	D31	SD_DAT0	PB14	PB18	SD_DAT2	USBD_VPO	UART2_RXD	SSI_TXFS	UART1_RTS	CONTRAST	FLM/VSYNC	LD8	LD9	LD12	NVDD2	**C**
D	A23	A24	SD_DAT1	PB17	NVDD1	USBD_VP	QVDD4	UART2_TXD	NVDD3	SPI1_MOSI	LP/HSYNC	LD1	LD11	TMR2OUT	LD13	**D**
E	A21	A22	D30	D29	NVDD1	QVSS	UART2_RTS	UART1_RXD	UART1_CTS	SPI1_MISO	ACD/OE	LD10	TIN	CSI_D0	CSI_MCLK	**E**
F	A20	A19	D28	D27	NVDD1	NVDD1	UART2_CTS	SSI_RXCLK	SSI_TXDAT	CLS	QVDD3	LD14	LD15	CSI_D2	CSI_D4	**F**
G	A17	A18	D26	D25	NVDD1	NVSS	NVDD4	NVSS	NVSS	QVSS	PWMO	CSI_D3	CSI_D7	CSI_HSYNC	CSI_D5	**G**
H	A15	A16	D23	D24	D22	NVSS	NVSS	NVSS	NVSS	NVDD2	CSI_D1	CSI_VSYNC	CSI_PIXCLK	I2C_SDA	TMS	**H**
J	A14	A12	D21	D20	NVDD1	NVSS	NVSS	QVDD1	NVSS	CSI_D6	I2C_SCL	TCK	TDO	BOOT1	BOOT0	**J**
K	A13	A11	CS2	D19	NVDD1	NVSS	QVSS	NVDD1	NVSS	D1	BOOT2	TDI	BIG_ENDIAN	RESET_OUT	XTAL32K	**K**
L	A10	A9	D17	D18	NVDD1	NVDD1	CS5	D2	ECB	NVSS	NVSS	POR	QVSS	XTAL16M	EXTAL32K	**L**
M	D16	D15	D13	D10	EB3	NVDD1	CS4	CS1	BCLK[1]	RW	NVSS	BOOT3	QVDD2	RESET_IN	EXTAL16M	**M**
N	A8	A7	D12	EB0	D9	D8	CS3	CS0	PA17	D0	DQM2	DQM0	SDCKE0	TRISTATE	TRST	**N**
P	D14	A5	A4	A3	A2	A1	D6	D5	MA10	MA11	DQM1	RAS	SDCKE1	CLKO	RESET_SF[2]	**P**
R	A6	D11	EB1	EB2	OE	D7	A0	SDCLK	D4	LBA	D3	DQM3	CAS	SDWE	AVDD1	**R**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	

1 Burst Clock

2 This signal is not used and should be floated in an actual application.

6 Product Documentation

6.1 Revision History

Table 39 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 39. i.MXL Data Sheet Revision History Rev. 8

Location	Revision
Table 2 on page 4 Signal Names and Descriptions	• Added the DMA_REQ signal to table. • Corrected signal name from $\overline{\text{USBD\_OE}}$ to $\overline{\text{USBD\_ROE}}$
Table 3 on page 9 Signal Multiplex Table i.MXL	Added Signal Multiplex table from Reference Manual with the following changes: • Changed I/O Supply Voltage,PB31–20, from NVDD3 to NVDD4 • Added 225 BGA column. • Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 21	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 9	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.