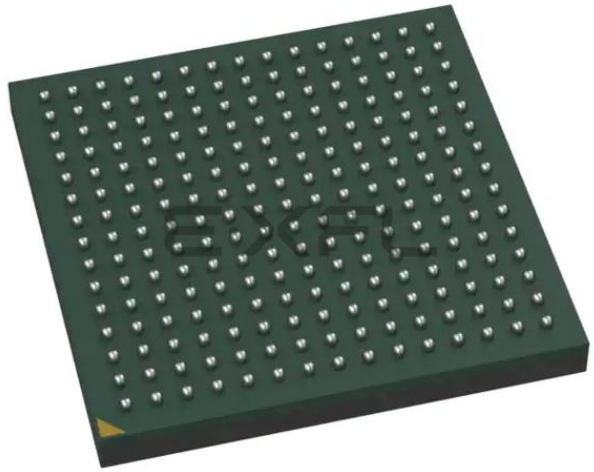

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM920T |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 200MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 3.0V |
| Operating Temperature | -30°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 225-LFBGA |
| Supplier Device Package | 225-MAPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxldvp20r2 |

**Table 2. i.MXL Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **Bootstrap** | |
| BOOT [3:0] | System Boot Mode Select—The operational system boot mode of the i.MXL processor upon system reset is determined by the settings of these pins. |
| **SDRAM Controller** | |
| SDBA [4:0] | SDRAM non-interleave mode bank address multiplexed with address signals A [15:11]. These signals are logically equivalent to core address p_addr [25:21] in SDRAM cycles. |
| SDIBA [3:0] | SDRAM interleave addressing mode bank address multiplexed with address signals A [19:16]. These signals are logically equivalent to core address p_addr [12:9] in SDRAM cycles. |
| MA [11:10] | SDRAM address signals |
| MA [9:0] | SDRAM address signals which are multiplexed with address signals A [10:1]. MA [9:0] are selected on SDRAM cycles. |
| DQM [3:0] | SDRAM data enable |
| $\overline{\text{CSD0}}$ | SDRAM Chip-select signal which is multiplexed with the $\overline{\text{CS2}}$ signal. These two signals are selectable by programming the system control register. |
| $\overline{\text{CSD1}}$ | SDRAM Chip-select signal which is multiplexed with $\overline{\text{CS3}}$ signal. These two signals are selectable by programming the system control register. By default, $\overline{\text{CSD1}}$ is selected, so it can be used as boot chip-select by properly configuring BOOT [3:0] input pins. |
| $\overline{\text{RAS}}$ | SDRAM Row Address Select signal |
| $\overline{\text{CAS}}$ | SDRAM Column Address Select signal |
| $\overline{\text{SDWE}}$ | SDRAM Write Enable signal |
| SDCKE0 | SDRAM Clock Enable 0 |
| SDCKE1 | SDRAM Clock Enable 1 |
| SDCLK | SDRAM Clock |
| $\overline{\text{RESET\_SF}}$ | Not Used |
| **Clocks and Resets** | |
| EXTAL16M | Crystal input (4 MHz to 16 MHz), or a 16 MHz oscillator input when the internal oscillator circuit is shut down. |
| XTAL16M | Crystal output |
| EXTAL32K | 32 kHz crystal input |
| XTAL32K | 32 kHz crystal output |
| CLKO | Clock Out signal selected from internal clock signals. |
| $\overline{\text{RESET\_IN}}$ | Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module and the clock control module) are reset. |
| $\overline{\text{RESET\_OUT}}$ | Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{\text{RESET\_IN}}$), and Watchdog time-out. |
| POR | Power On Reset—Internal active high Schmitt trigger input signal. The POR signal is normally generated by an external RC circuit designed to detect a power-up event. |

**Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | 256 BGA Ball | Primary | | | Alternate | | GPIO | | AIN | BIN | AOUT | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Pull-Up | Signal | Dir | Mux | Pull-Up | | | | |
| NVDD1 | N4 | P3 | $\overline{EB0}$ | O | | | | | | | | | |
| NVDD1 | M4 | N3 | D10 | I/O | 69K | | | | | | | | |
| NVDD1 | P4 | P1 | A3 | O | | | | | | | | | |
| NVDD1 | R3 | N2 | $\overline{EB1}$ | O | | | | | | | | | |
| NVDD1 | N5 | P2 | D9 | I/O | 69K | | | | | | | | |
| NVDD1 | R4 | R1 | $\overline{EB2}$ | O | | | | | | | | | |
| NVDD1 | P5 | T2 | A2 | O | | | | | | | | | |
| NVDD1 | M5 | R2 | $\overline{EB3}$ | O | | | | | | | | | |
| NVDD1 | N6 | R5 | D8 | I/O | 69K | | | | | | | | |
| NVDD1 | R5 | T3 | $\overline{OE}$ | O | | | | | | | | | |
| NVDD1 | P6 | R3 | A1 | O | | | | | | | | | |
| NVDD1 | L7 | T4 | $\overline{CS5}$ | O | | | | PA23 | 69K | | | | PA23 |
| NVDD1 | R6 | N4 | D7 | I/O | 69K | | | | | | | | |
| NVDD1 | M7 | R4 | $\overline{CS4}$ | O | | | | PA22 | 69K | | | | PA22 |
| NVDD1 | R7 | N5 | A0 | O | | | | PA21 | 69K | | | | A0 |
| NVDD1 | N7 | P4 | $\overline{CS3}$ | O | | $\overline{CSD1}$ | | | | | | | $\overline{CSD1}$ |
| NVDD1 | P7 | P5 | D6 | I/O | 69K | | | | | | | | |
| NVDD1 | K3 | T5 | $\overline{CS2}$ | O | | $\overline{CSD0}$ | | | | | | | $\overline{CSD0}$ |
| NVDD1 | R8 | M5 | SDCLK | O | | | | | | | | | |
| NVDD1 | M8 | T6 | $\overline{CS1}$ | O | | | | | | | | | |
| NVDD1 | N8 | T7 | $\overline{CS0}$ | O | | | | | | | | | |
| NVDD1 | P8 | R6 | D5 | I/O | 69K | | | | | | | | |
| NVDD1 | L9 | P6 | $\overline{ECB}$ | I | | ETMTRACEPKT7 | | PA20 | 69K | | | | $\overline{ECB}$ |
| NVDD1 | R9 | N6 | D4 | I/O | 69K | | | | | | | | |
| NVDD1 | R10 | R7 | $\overline{LBA}$ | O | | ETMTRACEPKT6 | | PA19 | 69K | | | | $\overline{LBA}$ |
| NVDD1 | R11 | P8 | D3 | I/O | 69K | | | | | | | | |
| NVDD1 | M9 | R8 | BCLK | | | ETMTRACEPKT5 | | PA18 | 69K | | | | BCLK |
| NVDD1 | L8 | P7 | D2 | I/O | 69K | | | | | | | | |
| NVDD1 | N9 | N7 | PA17 | | | ETMTRACEPKT4 | | PA17 | 69K | SPI2_$\overline{SS}$ | | $\overline{DTACK}$ | PA17 |
| NVDD1 | K10 | N8 | D1 | I/O | 69K | | | | | | | | |
| NVDD1 | M10 | M7 | $\overline{RW}$ | | | | | | | | | | |
| NVDD1 | P10 | T8 | MA11 | O | | | | | | | | | |
| NVDD1 | P9 | M8 | MA10 | O | | | | | | | | | |
| NVDD1 | N10 | R9 | D0 | I/O | 69K | | | | | | | | |
| NVDD1 | R12 | P9 | DQM3 | O | | | | | | | | | |

**Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)**

| I/O Supply Voltage | 225 BGA Ball | 256 BGA Ball | Primary | | | Alternate | | GPIO | | AIN | BIN | AOUT | Default |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Signal | Dir | Pull-Up | Signal | Dir | Mux | Pull-Up | | | | |
| NVDD1 | N11 | T9 | DQM2 | O | | | | | | | | | |
| NVDD1 | P11 | N9 | DQM1 | O | | | | | | | | | |
| NVDD1 | N12 | R10 | DQM0 | O | | | | | | | | | |
| NVDD1 | P12 | M9 | $\overline{RAS}$ | O | | | | | | | | | |
| NVDD1 | R13 | L8 | $\overline{CAS}$ | O | | | | | | | | | |
| NVDD1 | R14 | T10 | $\overline{SDWE}$ | O | | | | | | | | | |
| NVDD1 | N13 | R11 | SDCKE0 | O | | | | | | | | | |
| NVDD1 | P13 | P10 | SDCKE1 | O | | | | | | | | | |
| NVDD1 | P15 | N10 | $\overline{RESET\_SF}$ | O | | | | | | | | | |
| NVDD1 | P14 | T11 | CLKO | O | | | | | | | | | |
| AVDD1 | R15 | T12 | AVDD1 | Static | | | | | | | | | |
| QVDD2 | M13 | R15 | QVDD2 | Static | | | | | | | | | |
| AVDD1 | N15 | P13 | $\overline{TRST}$ | I | 69K | | | | | | | | |
| AVDD1 | N14 | T13 | TRISTATE[1] | I | | | | | | | | | |
| AVDD1 | M15 | T14 | EXTAL16M | I | | | | | | | | | |
| AVDD1 | L14 | T15 | XTAL16M | O | | | | | | | | | |
| AVDD1 | L15 | R16 | EXTAL32K | I | | | | | | | | | |
| AVDD1 | K15 | P16 | XTAL32K | O | | | | | | | | | |
| AVDD1 | M14 | M10 | $\overline{RESET\_IN}$[2] | I | 69K | | | | | | | | |
| AVDD1 | K14 | N11 | $\overline{RESET\_OUT}$ | O | | | | | | | | | |
| AVDD1 | L12 | R12 | POR[2] | I | | | | | | | | | |
| AVDD1 | K13 | M11 | BIG_ENDIAN[3] | I | | | | | | | | | |
| AVDD1 | M12 | P11 | BOOT3[3] | I | | | | | | | | | |
| AVDD1 | K11 | N12 | BOOT2[3] | I | | | | | | | | | |
| AVDD1 | J14 | R13 | BOOT1[3] | I | | | | | | | | | |
| AVDD1 | J15 | P12 | BOOT0[3] | I | | | | | | | | | |
| NVDD2 | J13 | R14 | $\overline{TDO}$[4] | O | | | | | | | | | |
| NVDD2 | H15 | N15 | TMS | I | 69K | | | | | | | | |
| NVDD2 | J12 | L9 | TCK | I | 69K | | | | | | | | |
| NVDD2 | K12 | N16 | TDI | I | 69K | | | | | | | | |
| NVDD2 | J11 | P14 | I2C_SCL | O | | | | PA16 | 69K | | | | PA16 |
| NVDD2 | H14 | P15 | I2C_SDA | I/O | | | | PA15 | 69K | | | | PA15 |

### 4.4.2.1 WAIT Read Cycle without DMA

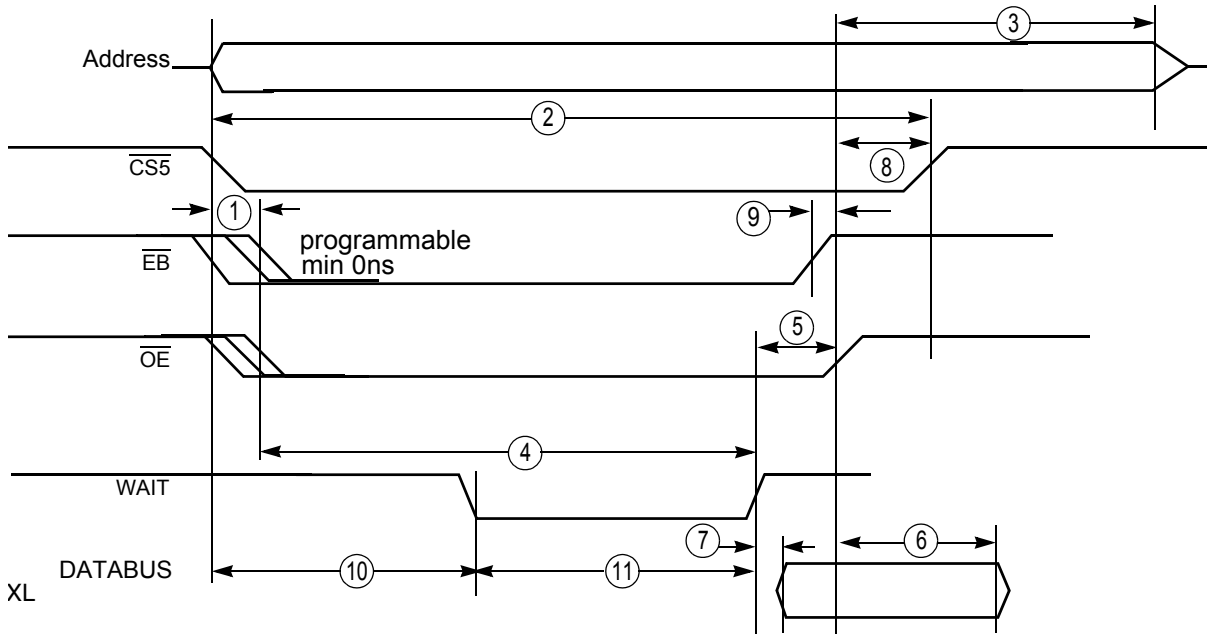



**Figure 6. WAIT Read Cycle without DMA**

**Table 13. WAIT Read Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz**

| Number | Characteristic | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{OE}$ and $\overline{EB}$ assertion time | See note 2 | – | ns |
| 2 | $\overline{CS5}$ pulse width | 3T | – | ns |
| 3 | $\overline{OE}$ negated to address inactive | 56.81 | 57.28 | ns |
| 4 | Wait asserted after $\overline{OE}$ asserted | – | 1020T | ns |
| 5 | Wait asserted to $\overline{OE}$ negated | 2T+1.57 | 3T+7.33 | ns |
| 6 | Data hold timing after $\overline{OE}$ negated | T-1.49 | – | ns |
| 7 | Data ready after wait asserted | 0 | T | ns |
| 8 | OE negated to CS negated | 1.5T-0.68 | 1.5T-0.06 | ns |
| 9 | OE negated after EB negated | 0.06 | 0.18 | ns |
| 10 | Become low after CS5 asserted | 0 | 1019T | ns |
| 11 | Wait pulse width | 1T | 1020T | ns |

**Note**:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

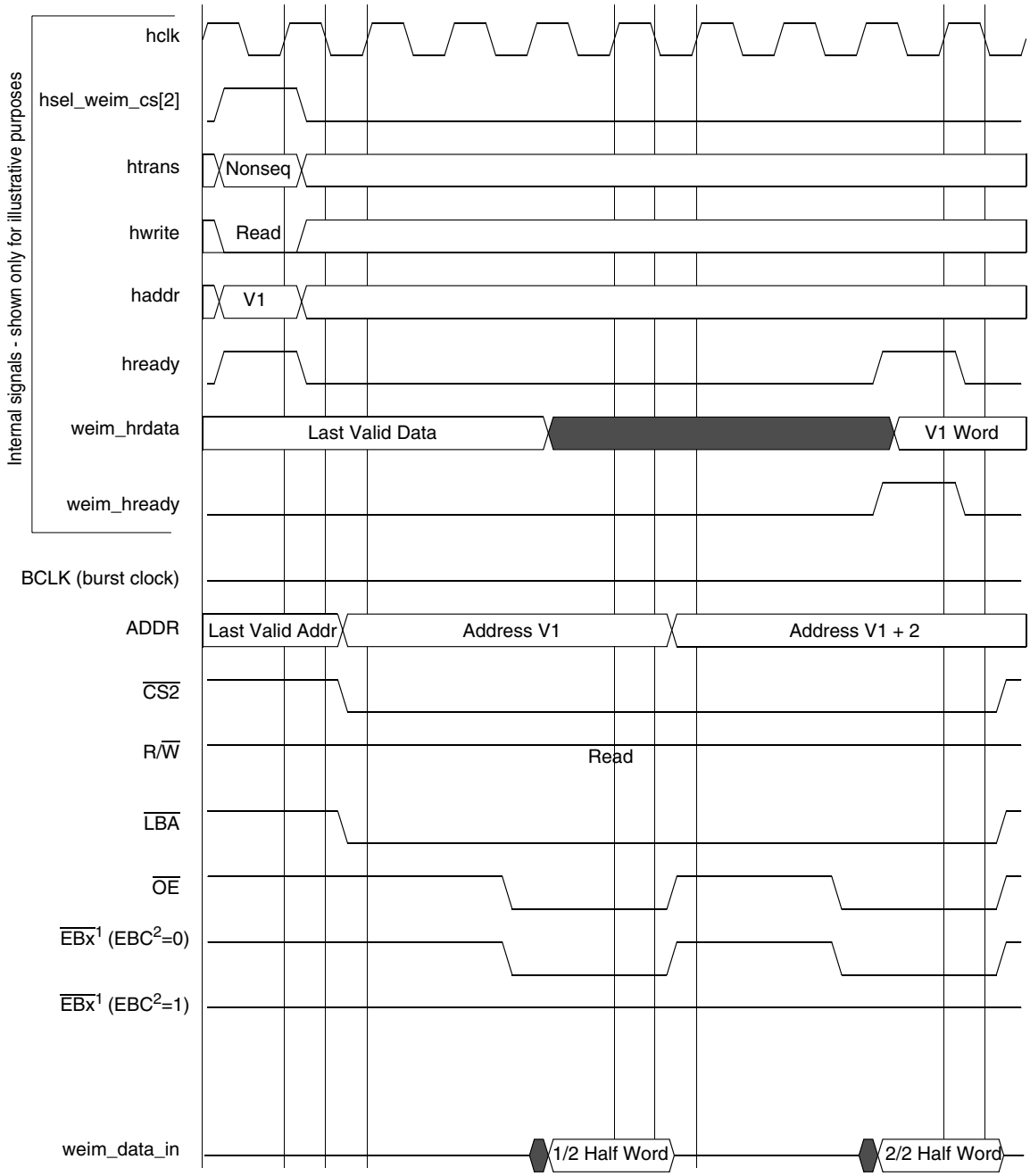
**Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz**

| Number | Characteristic | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $\overline{CS5}$ assertion time | See note 2 | – | ns |
| 2 | $\overline{EB}$ assertion time | See note 2 | – | ns |
| 3 | $\overline{CS5}$ pulse width | 3T | – | ns |
| 4 | $\overline{RW}$ negated before $\overline{CS5}$ is negated | 2.5T-3.63 | 2.5T-1.16 | ns |
| 5 | Address inactived after $\overline{CS}$ negated | – | 0.09 | ns |
| 6 | Wait asserted after $\overline{CS5}$ asserted | – | 1020T | ns |
| 7 | Wait asserted to $\overline{RW}$ negated | T+2.66 | 2T+7.96 | ns |
| 8 | Data hold timing after $\overline{RW}$ negated | 2T+0.03 | – | ns |
| 9 | Data ready after $\overline{CS5}$ is asserted | – | T | ns |
| 10 | $\overline{CS}$ deactive to next $\overline{CS}$ active | T | – | ns |
| 11 | $\overline{EB}$ negate after $\overline{CS}$ negate | 0.5T | 0.5T+0.5 | |
| 12 | Wait becomes low after $\overline{CS5}$ asserted | 0 | 1019T | ns |
| 13 | Wait pulse width | 1T | 1020T | ns |

**Note**:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

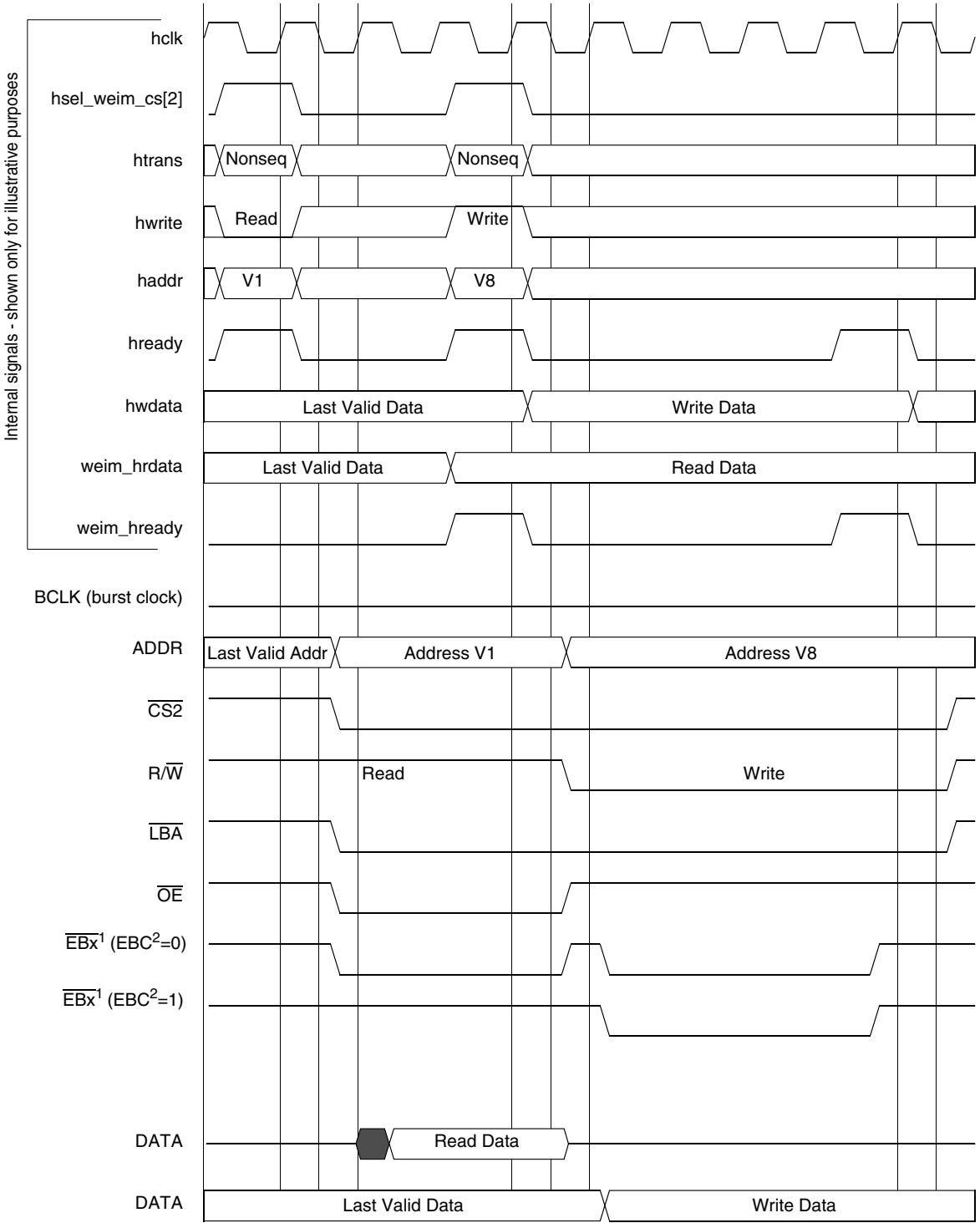
## 4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MXL, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.



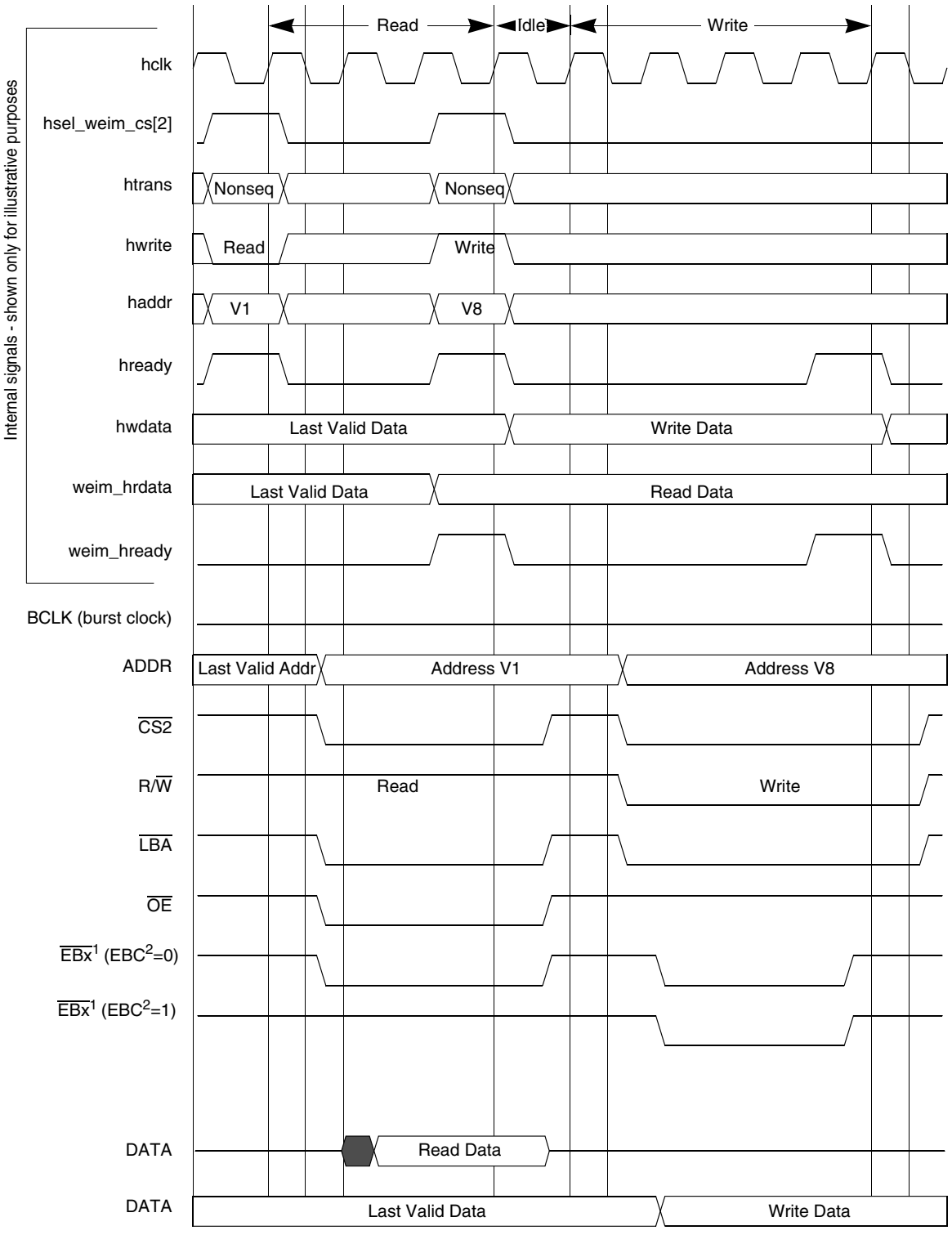

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 16. WSC = 3, OEA = 4, A.WORD/E.HALF**



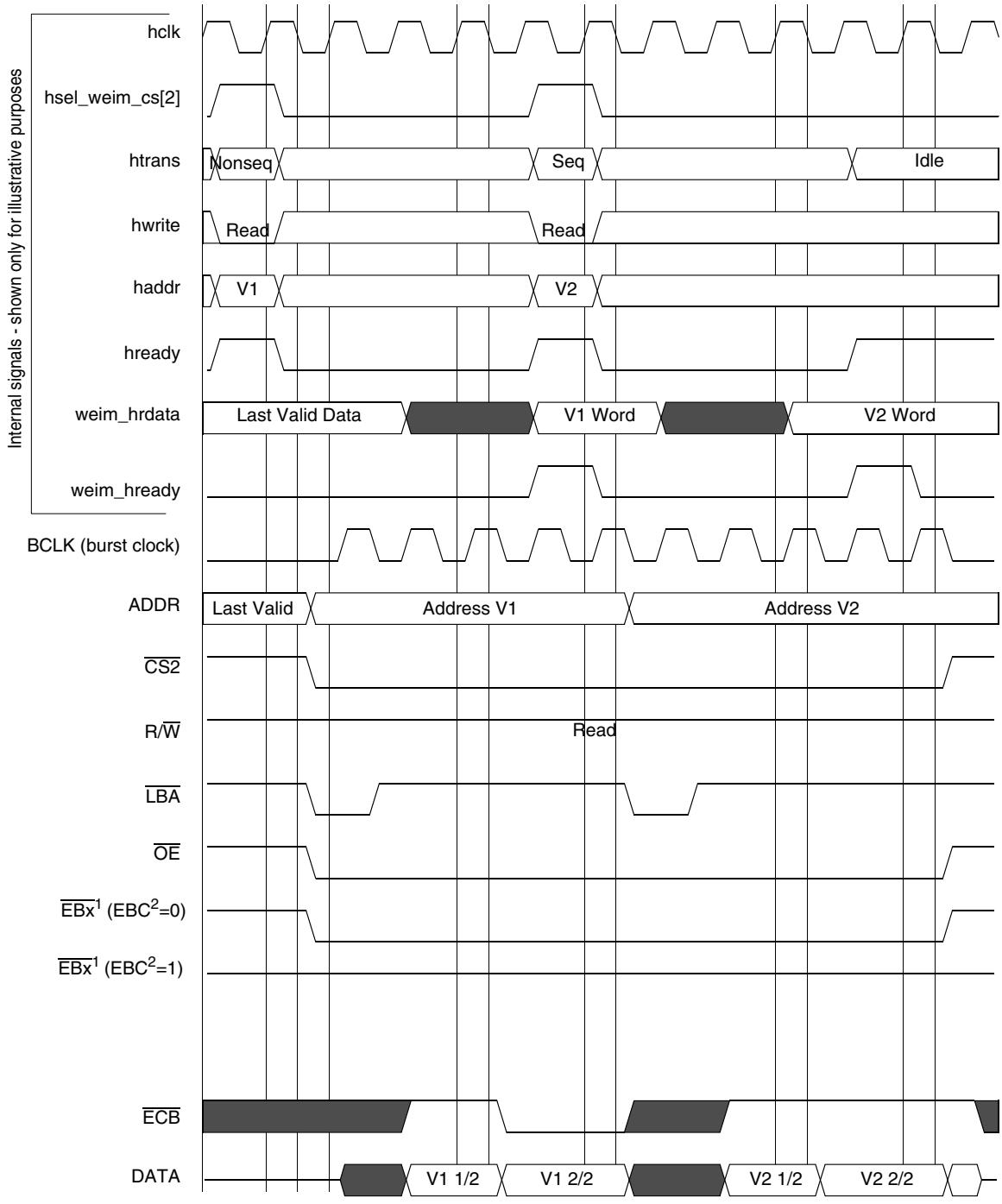

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF**



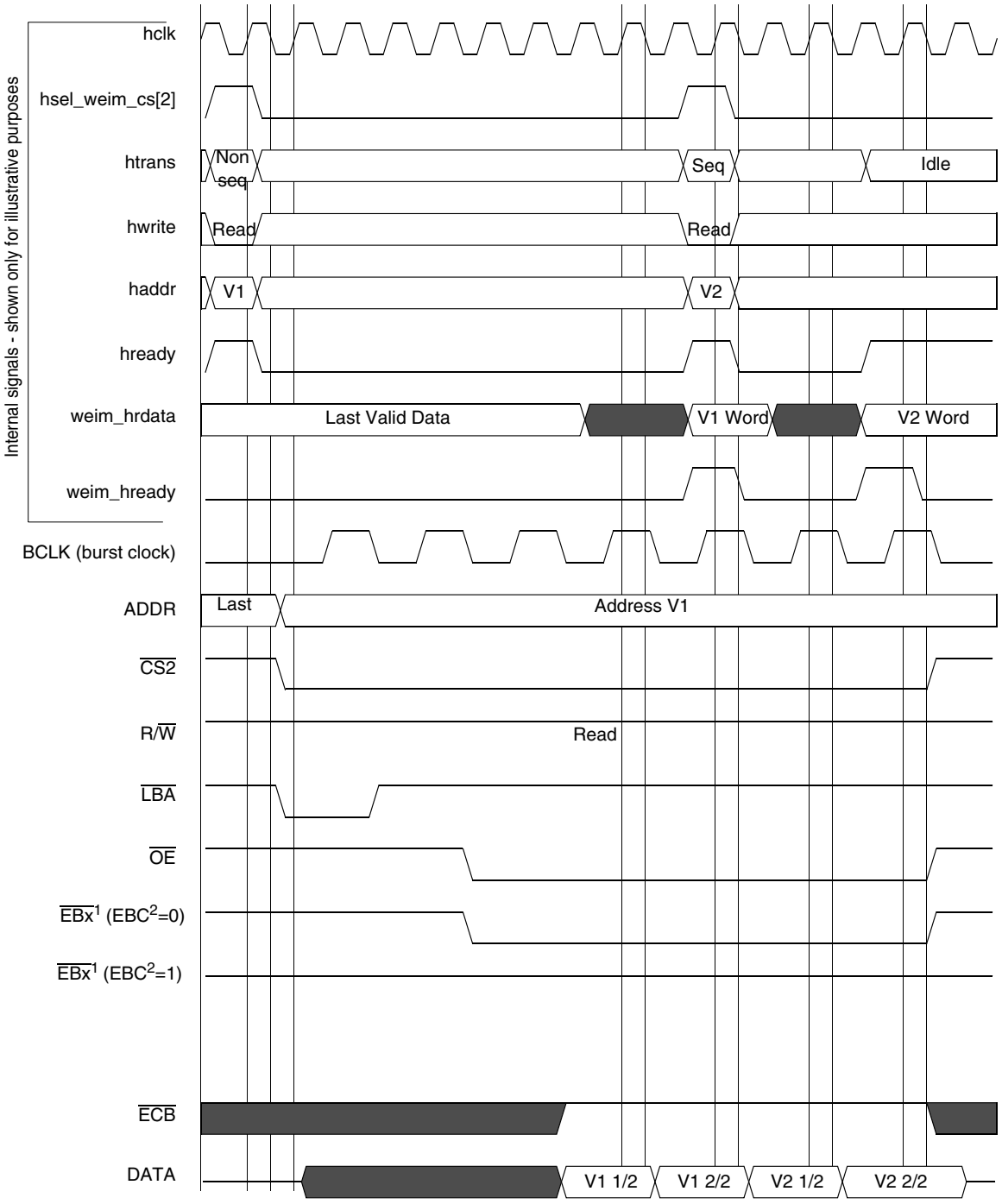

Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 23. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF**




Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

**Figure 32. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF**

### 4.4.4 Non-TFT Panel Timing

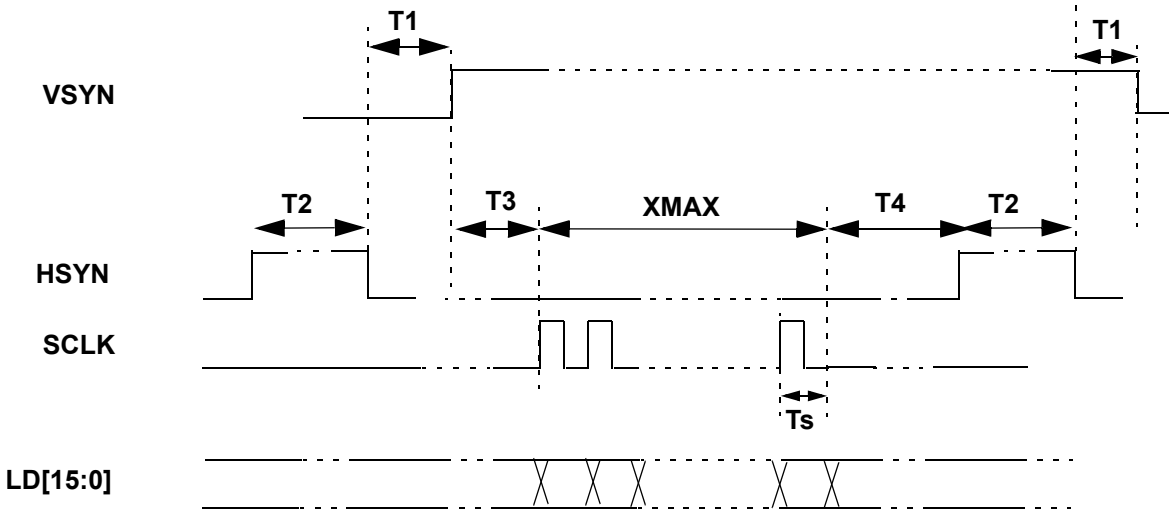



Figure 33. Non-TFT Panel Timing

Table 17. Non TFT Panel Timing Diagram

| Symbol | Parameter | Allowed Register Minimum Value[1, 2] | Actual Value | Unit |
|---|---|---|---|---|
| T1 | HSYN to VSYN delay[3] | 0 | HWAIT2+2 | Tpix[4] |
| T2 | HSYN pulse width | 0 | HWIDTH+1 | Tpix |
| T3 | VSYN to SCLK | – | 0 ≤ T3 ≤ Ts[5] | – |
| T4 | SCLK to HSYN | 0 | HWAIT1+1 | Tpix |

1 Maximum frequency of LCDC_CLK is 48 MHz, which is controlled by Peripheral Clock Divider Register.

2 Maximum frequency of SCLK is HCLK / 5, otherwise LD output will be wrong.

3 VSYN, HSYN and SCLK can be programmed as active high or active low. In the above timing diagram, all these 3 signals are active high.

4 Tpix is the pixel clock period which equals LCDC_CLK period * (PCD + 1).

5 Ts is the shift clock period. Ts = Tpix * (panel data bus width).

## 4.5 SPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the SPI 1 module is configured as a master, two control signals are used for data transfer rate control: the $\overline{SS}$ signal (output) and the $\overline{SPI\_RDY}$ signal (input). The SPI1 Sample Period Control Register (PERIODREG1) and the SPI2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either SPI 1 or SPI 2. When the SPI 1 module is configured as a slave, the user can configure the SPI1 Control Register (CONTROLREG1) to match the external SPI master's timing. In this configuration, $\overline{SS}$ becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO. Figure 34 through Figure 38 show the timing relationship of the master SPI using different triggering mechanisms.

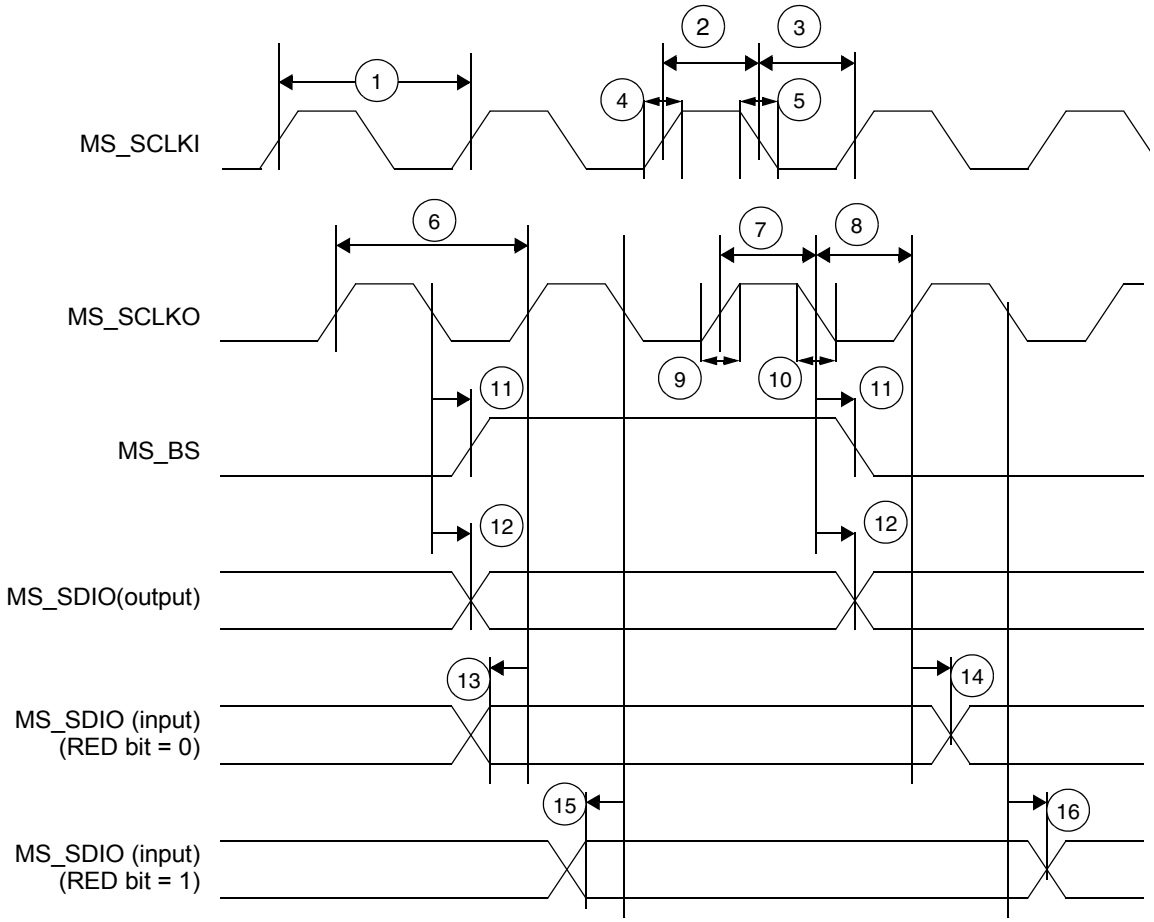



**Figure 50. MSHC Signal Timing Diagram**

**Table 25. MSHC Signal Timing Parameter Table**

| Ref No. | Parameter | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | MS_SCLKI frequency | – | 25 | MHz |
| 2 | MS_SCLKI high pulse width | 20 | – | ns |
| 3 | MS_SCLKI low pulse width | 20 | – | ns |
| 4 | MS_SCLKI rise time | – | 3 | ns |
| 5 | MS_SCLKI fall time | – | 3 | ns |
| 6 | MS_SCLKO frequency[1] | – | 25 | MHz |
| 7 | MS_SCLKO high pulse width[1] | 20 | – | ns |
| 8 | MS_SCLKO low pulse width[1] | 15 | – | ns |
| 9 | MS_SCLKO rise time[1] | – | 5 | ns |
| 10 | MS_SCLKO fall time[1] | – | 5 | ns |
| 11 | MS_BS delay time[1] | – | 3 | ns |

**Table 27. SDRAM Read Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 2.67 | – | 4 | – | ns |
| 2 | SDRAM clock low-level width | 6 | – | 4 | – | ns |
| 3 | SDRAM clock cycle time | 11.4 | – | 10 | – | ns |
| 3S | CS, RAS, CAS, WE, DQM setup time | 3.42 | – | 3 | – | ns |
| 3H | CS, RAS, CAS, WE, DQM hold time | 2.28 | – | 2 | – | ns |
| 4S | Address setup time | 3.42 | – | 3 | – | ns |
| 4H | Address hold time | 2.28 | – | 2 | – | ns |
| 5 | SDRAM access time (CL = 3) | – | 6.84 | – | 6 | ns |
| 5 | SDRAM access time (CL = 2) | – | 6.84 | – | 6 | ns |
| 5 | SDRAM access time (CL = 1) | – | 22 | – | 22 | ns |
| 6 | Data out hold time | 2.85 | – | 2.5 | – | ns |
| 7 | Data out high-impedance time (CL = 3) | – | 6.84 | – | 6 | ns |
| 7 | Data out high-impedance time (CL = 2) | – | 6.84 | – | 6 | ns |
| 7 | Data out high-impedance time (CL = 1) | – | 22 | – | 22 | ns |
| 8 | Active to read/write command period (RC = 1) | $t_{RCD}$[1] | – | $t_{RCD1}$ | – | ns |

[1] $t_{RCD}$ = SDRAM clock cycle time. This settings can be found in the *MC9328MXL reference manual*.

**Table 34. SSI (Port B Alternate Function) Timing Parameter Table**

| Ref No. | Parameter | 1.8 ± 0.1 V | | 3.0 ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (Port B Alternate Function[2])** | | | | | | |
| 1 | STCK/SRCK clock period[1] | 95 | – | 83.3 | – | ns |
| 2 | STCK high to STFS (bl) high[3] | 1.7 | 4.8 | 1.5 | 4.2 | ns |
| 3 | SRCK high to SRFS (bl) high[3] | -0.1 | 1.0 | -0.1 | 1.0 | ns |
| 4 | STCK high to STFS (bl) low[3] | 3.08 | 5.24 | 2.7 | 4.6 | ns |
| 5 | SRCK high to SRFS (bl) low[3] | 1.25 | 2.28 | 1.1 | 2.0 | ns |
| 6 | STCK high to STFS (wl) high[3] | 1.71 | 4.79 | 1.5 | 4.2 | ns |
| 7 | SRCK high to SRFS (wl) high[3] | -0.1 | 1.0 | -0.1 | 1.0 | ns |
| 8 | STCK high to STFS (wl) low[3] | 3.08 | 5.24 | 2.7 | 4.6 | ns |
| 9 | SRCK high to SRFS (wl) low[3] | 1.25 | 2.28 | 1.1 | 2.0 | ns |
| 10 | STCK high to STXD valid from high impedance | 14.93 | 16.19 | 13.1 | 14.2 | ns |
| 11a | STCK high to STXD high | 1.25 | 3.42 | 1.1 | 3.0 | ns |
| 11b | STCK high to STXD low | 2.51 | 3.99 | 2.2 | 3.5 | ns |
| 12 | STCK high to STXD high impedance | 12.43 | 14.59 | 10.9 | 12.8 | ns |
| 13 | SRXD setup time before SRCK low | 20 | – | 17.5 | – | ns |
| 14 | SRXD hold time after SRCK low | 0 | – | 0 | – | ns |
| **External Clock Operation (Port B Alternate Function[2])** | | | | | | |
| 15 | STCK/SRCK clock period[1] | 92.8 | – | 81.4 | – | ns |
| 16 | STCK/SRCK clock high period | 27.1 | – | 40.7 | – | ns |
| 17 | STCK/SRCK clock low period | 61.1 | – | 40.7 | – | ns |
| 18 | STCK high to STFS (bl) high[3] | – | 92.8 | 0 | 81.4 | ns |
| 19 | SRCK high to SRFS (bl) high[3] | – | 92.8 | 0 | 81.4 | ns |
| 20 | STCK high to STFS (bl) low[3] | – | 92.8 | 0 | 81.4 | ns |
| 21 | SRCK high to SRFS (bl) low[3] | – | 92.8 | 0 | 81.4 | ns |
| 22 | STCK high to STFS (wl) high[3] | – | 92.8 | 0 | 81.4 | ns |
| 23 | SRCK high to SRFS (wl) high[3] | – | 92.8 | 0 | 81.4 | ns |
| 24 | STCK high to STFS (wl) low[3] | – | 92.8 | 0 | 81.4 | ns |
| 25 | SRCK high to SRFS (wl) low[3] | – | 92.8 | 0 | 81.4 | ns |
| 26 | STCK high to STXD valid from high impedance | 18.9 | 29.07 | 16.6 | 25.5 | ns |
| 27a | STCK high to STXD high | 9.23 | 20.75 | 8.1 | 18.2 | ns |
| 27b | STCK high to STXD low | 10.60 | 21.32 | 9.3 | 18.7 | ns |

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

### 4.14.2 Non-Gated Clock Mode

Figure 65 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 66 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 36.

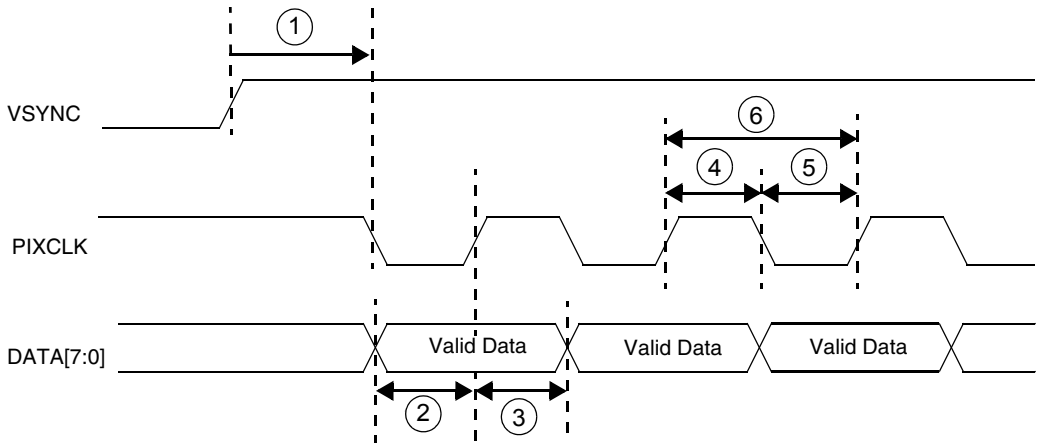



**Figure 65. Sensor Output Data on Pixel Clock Falling Edge**
**CSI Latches Data on Pixel Clock Rising Edge**

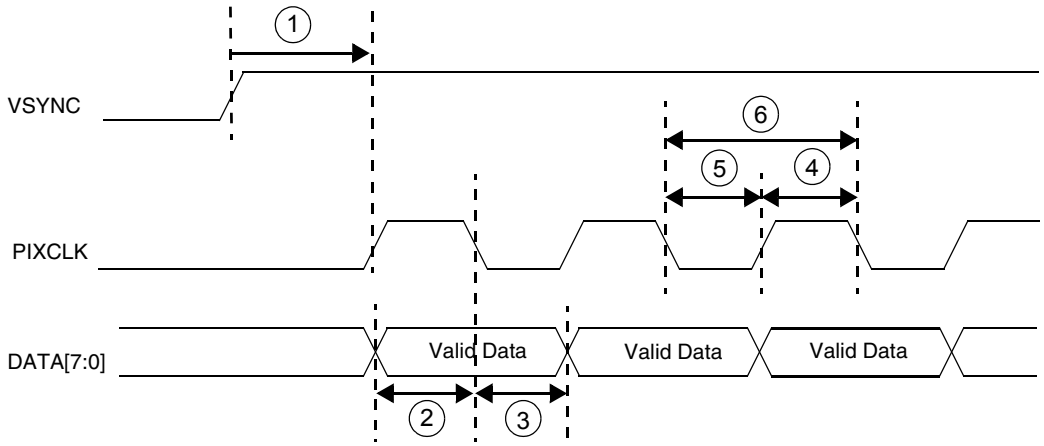



**Figure 66. Sensor Output Data on Pixel Clock Rising Edge**
**CSI Latches Data on Pixel Clock Falling Edge**

**Table 36. Non-Gated Clock Mode Parameters**

| Ref No. | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| 1 | csi_vsync to csi_pixclk | 180 | – | ns |
| 2 | csi_d setup time | 1 | – | ns |
| 3 | csi_d hold time | 1 | – | ns |
| 4 | csi_pixclk high time | 10.42 | – | ns |
| 5 | csi_pixclk low time | 10.42 | – | ns |
| 6 | csi_pixclk frequency | 0 | 48 | MHz |

The limitation on pixel clock rise time / fall time are not specified. It should be calculated from the hold time and setup time, according to:

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
=> max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
=> max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

# 5 Pin-Out and Package Information

Table 37 illustrates the package pin assignments for the 256-pin MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 9.

**Table 37. i.MXL 256 MAPBGA Pin Assignments**

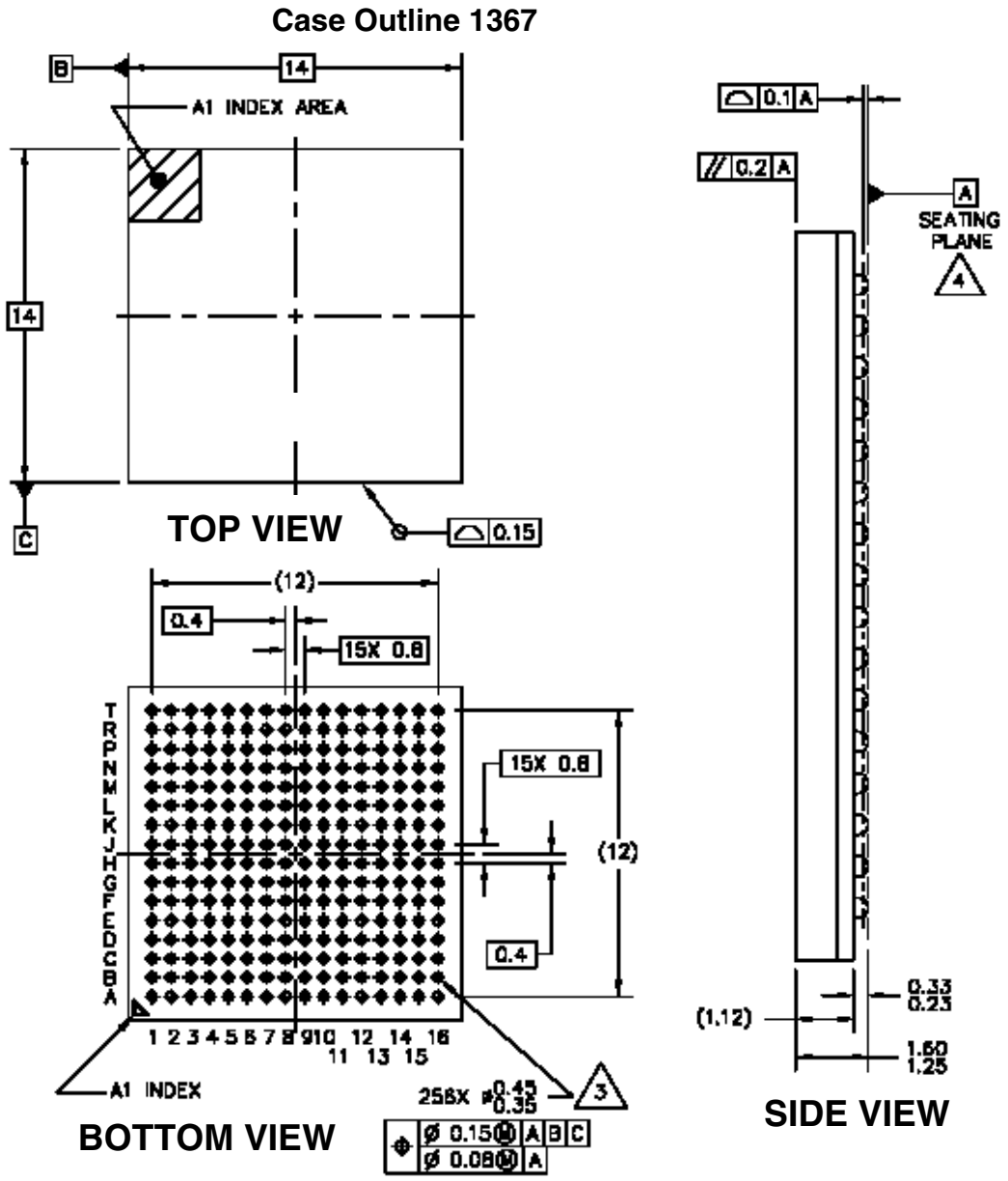
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NVSS | SD_DAT3 | SD_CLK | NVSS | USBD_ AFE | NVDD4 | NVSS | UART1_ RTS | UART1_ RXD | NVDD3 | N.C. | N.C. | QVDD4 | N.C. | N.C. | N.C. | A |
| B | A24 | SD_DAT1 | SD_CMD | PB16 | USBD_ ROE | USBD_VP | SSI_ RXCLK | SSI_ TXCLK | SPI1_ SCLK | N.C. | N.C. | N.C. | QVSS | N.C. | N.C. | N.C. | B |
| C | A23 | D31 | SD_DAT0 | PB15 | USBD_ RCV | UART2_ CTS | UART2_ RXD | SSI_ RXFS | UART1_ TXD | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | C |
| D | A22 | D30 | D29 | PB14 | USBD_ SUSPND | USBD_ VPO | USBD_ VMO | SSI_ RXDAT | SPI1_ SPI_RDY | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | D |
| E | A20 | A21 | D28 | D26 | SD_DAT2 | USBD_VM | UART2_ RTS | SSI_ TXDAT | SPI1_SS | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. | E |
| F | A18 | D27 | D25 | A19 | A16 | PB18 | UART2_ TXD | SSI_ TXFS | SPI1_ MISO | N.C. | N.C. | REV | N.C. | N.C. | LSCLK | SPL_SPR | F |
| G | A15 | A17 | D24 | D23 | D21 | PB17 | PB19 | UART1_ CTS | SPI1_ MOSI | N.C. | CLS | CONTRAST | ACD/OE | LP/ HSYNC | FLM/ VSYNC | LD1 | G |
| H | A13 | D22 | A14 | D20 | NVDD1 | NVDD1 | NVSS | QVSS | QVDD1 | PS | LD0 | LD2 | LD4 | LD5 | LD9 | LD3 | H |
| J | A12 | A11 | D18 | D19 | NVDD1 | NVDD1 | NVSS | NVDD1 | NVSS | NVSS | LD6 | LD7 | LD8 | LD11 | QVDD3 | QVSS | J |
| K | A10 | D16 | A9 | D17 | NVDD1 | NVSS | NVSS | NVDD1 | NVDD2 | NVDD2 | LD10 | LD12 | LD13 | LD14 | TMR2OUT | LD15 | K |
| L | A8 | A7 | D13 | D15 | D14 | NVDD1 | NVSS | CAS | TCK | TIN | PWMO | CSI_MCLK | CSI_D0 | CSI_D1 | CSI_D2 | CSI_D3 | L |
| M | A5 | D12 | D11 | A6 | SDCLK | NVSS | RW | MA10 | RAS | RESET_IN | BIG_ ENDIAN | CSI_D4 | CSI_ HSYNC | CSI_VSYNC | CSI_D6 | CSI_D5 | M |
| N | A4 | EB1 | D10 | D7 | A0 | D4 | PA17 | D1 | DQM1 | RESET_SF[1] | RESET_ OUT | BOOT2 | CSI_ PIXCLK | CSI_D7 | TMS | TDI | N |
| P | A3 | D9 | EB0 | CS3 | D6 | ECB | D2 | D3 | DQM3 | SDCKE1 | BOOT3 | BOOT0 | TRST | I2C_SCL | I2C_SDA | XTAL32K | P |
| R | EB2 | EB3 | A1 | CS4 | D8 | D5 | LBA | BCLK[2] | D0 | DQM0 | SDCKE0 | POR | BOOT1 | TDO | QVDD2 | EXTAL32K | R |
| T | NVSS | A2 | OE | CS5 | CS2 | CS1 | CS0 | MA11 | DQM2 | SDWE | CLKO | AVDD1 | TRISTATE | EXTAL16M | XTAL16M | QVSS | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

1 This signal is not used and should be floated in an actual application.

2 burst clock

## 5.1 MAPBGA 256 Package Dimensions

Figure 67 illustrates the 256 MAPBGA 14 mm × 14 mm × 1.30 mm package, with an 0.8 mm pad pitch. The device designator for the MAPBGA package is VH.



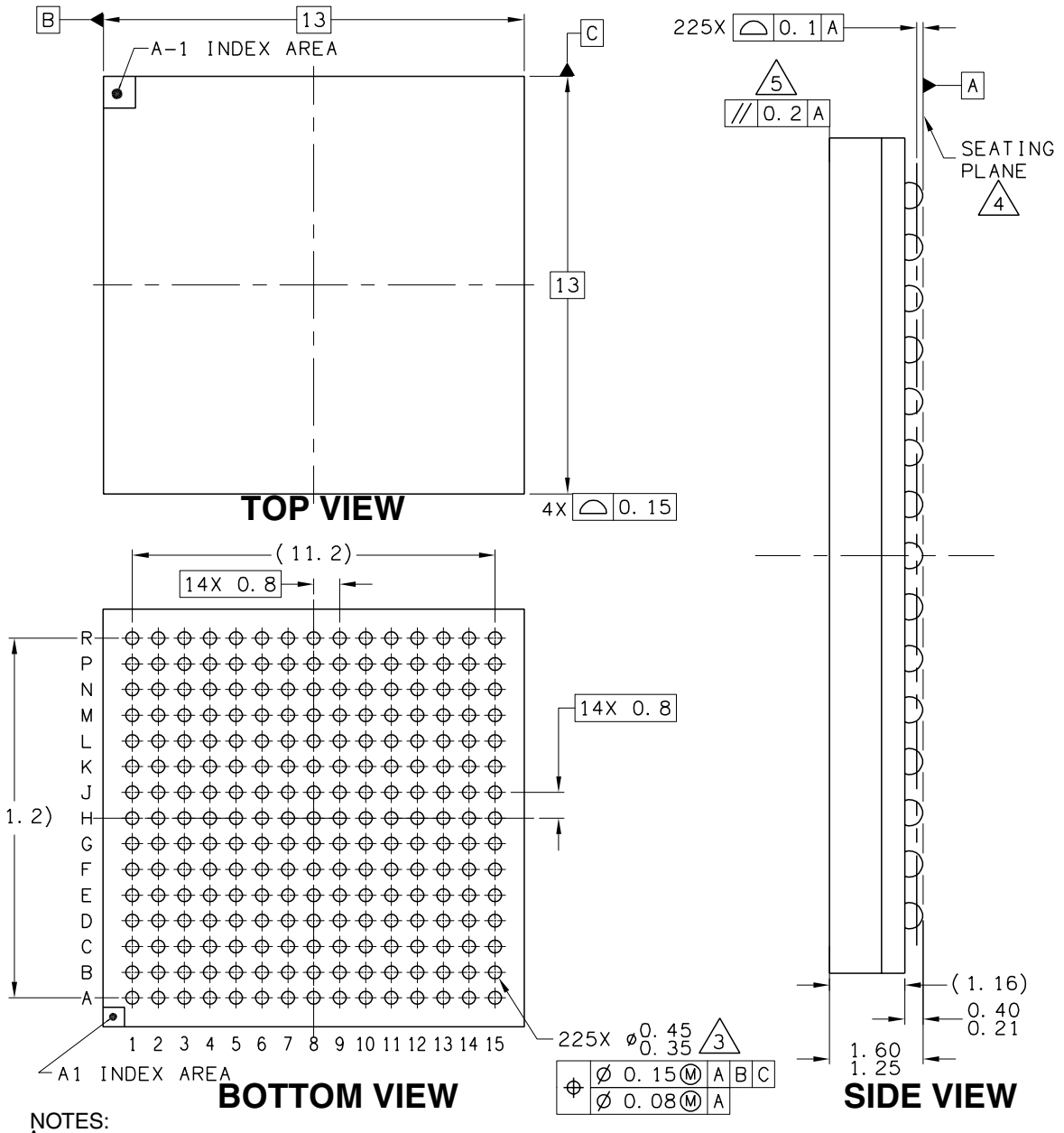

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2.INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3.MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.

**Figure 67. i.MXL 256 MAPBGA Mechanical Drawing**

## 5.2 MAPBGA 225 Package Dimensions

Figure 68 illustrates the 225 MAPBGA 13 mm × 13 mm package.

**Case Outline 1304B**




NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES PER ASME Y14 5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE IS DEFINED BY SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

**Figure 68. i.MXL 225 MAPBGA Mechanical Drawing**

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