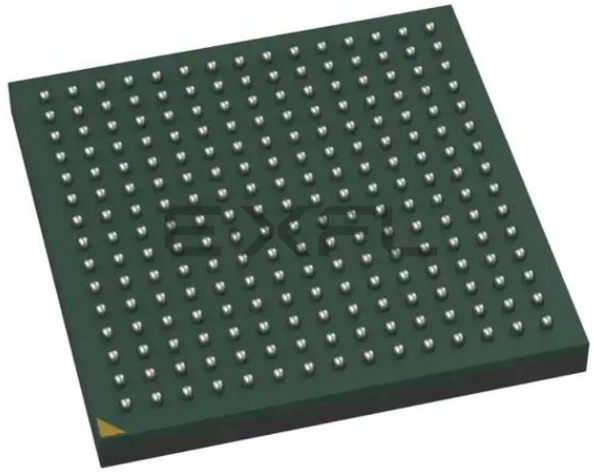

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxlvp20

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD2	H13	N13	CSI_PIXCLK	I				PA14	69K				PA14
NVDD2	G14	M13	CSI_HSYNC	I				PA13	69K				PA13
NVDD2	H12	M14	CSI_VSYNC	I				PA12	69K				PA12
NVDD2	G13	N14	CSI_D7	I				PA11	69K				PA11
NVDD2	J10	M15	CSI_D6	I				PA10	69K				PA10
NVDD2	G15	M16	CSI_D5	I				PA9	69K				PA9
NVDD2	F15	M12	CSI_D4	I				PA8	69K				PA8
NVDD2	G12	L16	CSI_D3	I				PA7	69K				PA7
NVDD2	F14	L15	CSI_D2	I				PA6	69K				PA6
NVDD2	H11	L14	CSI_D1	I				PA5	69K				PA5
NVDD2	E14	L13	CSI_D0	I				PA4	69K				PA4
NVDD2	E15	L12	CSI_MCLK	O				PA3	69K				PA3
NVDD2	G11	L11	PWMO	O				PA2	69K				PA2
NVDD2	E13	L10	TIN	I				PA1	69K			SPI2_RXD_0	PA1
NVDD2	D14	K15	TMR2OUT	O				PD31	69K		SPI2_TXD		PD31
NVDD2	F13	K16	LD15	O				PD30	69K				PD30
NVDD2	F12	K14	LD14	O				PD29	69K				PD29
NVDD2	D15	K13	LD13	O				PD28	69K				PD28
NVDD2	C14	K12	LD12	O				PD27	69K				PD27
NVDD2	D13	J14	LD11	O				PD26	69K				PD26
NVDD2	E12	K11	LD10	O				PD25	69K				PD25
NVDD2	C13	H15	LD9	O				PD24	69K				PD24
NVDD2	C12	J13	LD8	O				PD23	69K				PD23
NVDD2	B15	J12	LD7	O				PD22	69K				PD22
NVDD2	B14	J11	LD6	O				PD21	69K				PD21
NVDD2	A15	H14	LD5	O				PD20	69K				PD20
NVDD2	A14	H13	LD4	O				PD19	69K				PD19
NVDD2	B13	H16	LD3	O				PD18	69K				PD18
NVDD2	A13	H12	LD2	O				PD17	69K				PD17
NVDD2	D12	G16	LD1	O				PD16	69K				PD16
NVDD2	B12	H11	LD0	O				PD15	69K				PD15
NVDD2	C11	G15	FLM/VSYNC	O				PD14	69K				PD14

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD4	D8	F7	UART2_TXD	O				PB30	69K				PB30
NVDD4	E7	E7	$\overline{\text{UART2\_RTS}}$	I				PB29	69K				PB29
NVDD4	F7	C6	$\overline{\text{UART2\_CTS}}$	O				PB28	69K				PB28
NVDD4	B6	D7	USBD_VMO	O				PB27	69K				PB27
NVDD4	C6	D6	USBD_VPO	O				PB26	69K				PB26
NVDD4	A6	E6	USBD_VM	I				PB25	69K				PB25
NVDD4	D6	B6	USBD_VP	I				PB24	69K				PB24
NVDD4	A5	D5	USBD_SUSPND	O				PB23	69K				PB23
NVDD4	B5	C5	USBD_RCV	I/O				PB22	69K				PB22
NVDD4	A4	B5	$\overline{\text{USBD\_ROE}}$	O				PB21	69K				PB21
NVDD4	B4	A5	USBD_AFE	O				PB20	69K				PB20
NVDD4	A3	G7	PB19	I/O					69K				PB19
NVDD4	C4	F6	PB18	I/O					69K				PB18
NVDD4	D4	G6	PB17	O					69K				PB17
NVDD4	B3	B4	PB16	I					69K				PB16
NVDD4	A2	C4	PB15	I					69K				PB15
NVDD4	C3	D4	PB14	I					69K				PB14
NVDD4	A1	B3	SD_CMD	I/O		MS_BS		PB13	69K				PB13
NVDD4	B2	A3	SD_CLK	O		MS_SCLKO		PB12	69K				PB12
NVDD4	B1	A2	SD_DAT3	I/O		MS_SDIO		PB11	69K (pull down)				PB11
NVDD4	C5	E5	SD_DAT2	I/O		MS_SCLKI		PB10	69K				PB10
NVDD4	D3	B2	SD_DAT1	I/O		MS_PI1		PB9	69K				PB9
NVDD4	C2	C3	SD_DAT0	I/O		MS_PI0		PB8	69K				PB8
NVDD1	D5	K8	NVDD1	Static									
	G6	A1	NVSS	Static									
NVDD1	E5	H5	NVDD1	Static									
	H6	T1	NVSS	Static									
QVDD1	J8	H9	QVDD1	Static									
	E6	H8	QVSS	Static									

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD1	F5	J5	NVDD	Static									
	J6	K6	NVSS	Static									
NVDD1	G5	K5	NVDD1	Static									
	K6	M6	NVSS	Static									
NVDD1	J5	H6	NVDD1	Static									
	H7	J7	NVSS	Static									
NVDD1	K5	L6	NVDD1	Static									
	J7	J7	NVSS	Static									
NVDD1	L5	L6	NVDD1	Static									
	G8	K7	NVSS	Static									
NVDD1	L5	J8	NVDD1	Static									
	H8	L7	NVSS	Static									
	K7	T16	QVSS	Static									
NVDD2	H10	K10	NVDD2	Static									
	G9	J10	NVSS	Static									
QVDD3	F11	J15	QVDD3	Static									
	G10	J16	QVSS	Static									
NVDD2	C15	K9	NVDD2	Static									
	H9	J9	NVSS	Static									
QVDD4	D7	A13	QVDD4	Static									
	L13	B13	QVSS	Static									
NVDD3	D9	A10	NVDD3	Static									
	J9	A7	NVSS	Static									
	K9	A4	NVSS	Static									
NVDD4	G7	A6	NVDD4	Static									
NVDD1	F6		NVDD1	Static									
NVDD1	L6		NVDD1	Static									
NVDD1	M6		NVDD1	Static									
NVDD1	K8		NVDD1	Static									
	L10		NVSS	Static									
	L11		NVSS	Static									
	M11		NVSS	Static									

1 Pull down this input with 1KΩ resistor to GND.

2 External circuit required to drive this input.

3 Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

4 Pull up this output with a resistor to NVDD2.

4.3 Reset Module

The timing relationships of the Reset module with the POR and RESET_IN are shown in Figure 3 and Figure 4.

NOTE

Be aware that NVDD must ramp up to at least 1.8V before QVDD is powered up to prevent forward biasing.

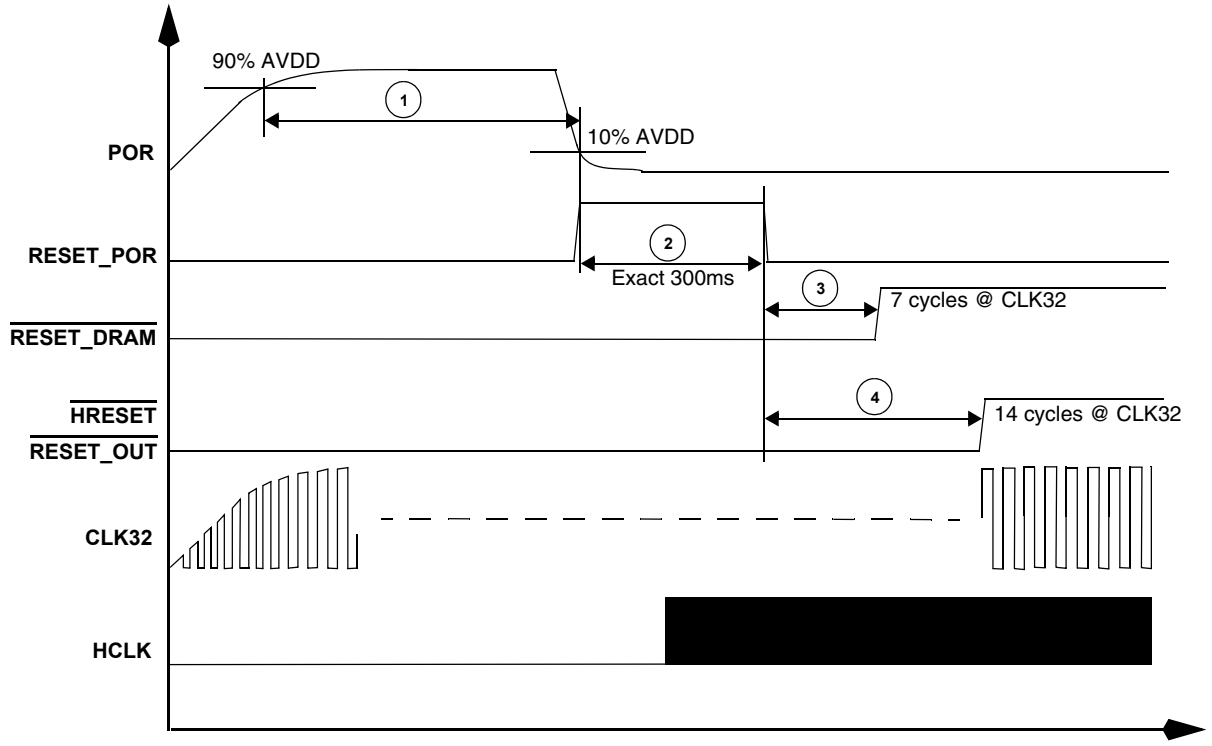


Figure 3. Timing Relationship with POR

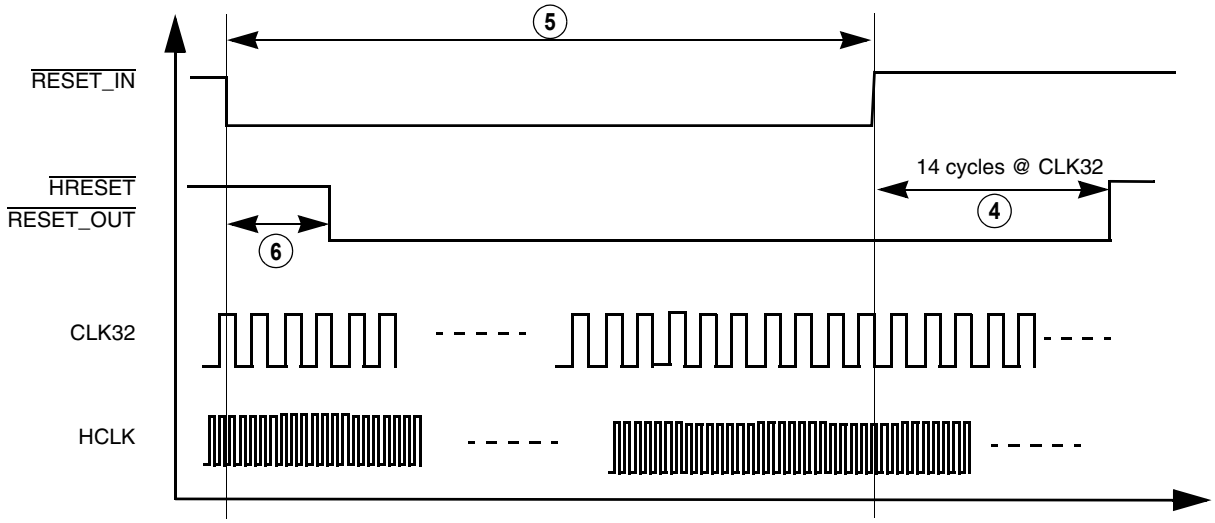


Figure 4. Timing Relationship with RESET_IN

Table 11. Reset Module Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Min	Max	Min	Max	
1	Width of input POWER_ON_RESET	note[1]	–	note[1]	–	–
2	Width of internal $\overline{\text{POWER\_ON\_RESET}}$ (CLK32 at 32 kHz)	300	300	300	300	ms
3	7K to 32K-cycle stretcher for SDRAM reset	7	7	7	7	Cycles of CLK32
4	14K to 32K-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET\_OUT}}$	14	14	14	14	Cycles of CLK32
5	Width of external hard-reset $\overline{\text{RESET\_IN}}$	4	–	4	–	Cycles of CLK32
6	4K to 32K-cycle qualifier	4	4	4	4	Cycles of CLK32

[1] POR width is dependent on the 32 or 32.768 kHz crystal oscillator start-up time. Design margin should allow for crystal tolerance, i.MX chip variations, temperature impact, and supply voltage influence. Through the process of supplying crystals for use with CMOS oscillators, crystal manufacturers have developed a working knowledge of start-up time of their crystals. Typically, start-up times range from 400 ms to 1.2 seconds for this type of crystal.
If an external stable clock source (already running) is used instead of a crystal, the width of POR should be ignored in calculating timing for the start-up process.

4.4 External Interface Module

The External Interface Module (EIM) handles the interface to devices external to the i.MXL processor, including the generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.

Table 12. EIM Bus Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V			3.0 ± 0.3 V			Unit
		Min	Typical	Max	Min	Typical	Max	
4a	Clock[1] rise to Output Enable Valid	2.32	2.62	6.85	2.3	2.6	6.8	ns
4b	Clock[1] rise to Output Enable Invalid	2.11	2.52	6.55	2.1	2.5	6.5	ns
4c	Clock[1] fall to Output Enable Valid	2.38	2.69	7.04	2.3	2.6	6.8	ns
4d	Clock[1] fall to Output Enable Invalid	2.17	2.59	6.73	2.1	2.5	6.5	ns
5a	Clock[1] rise to Enable Bytes Valid	1.91	2.52	5.54	1.9	2.5	5.5	ns
5b	Clock[1] rise to Enable Bytes Invalid	1.81	2.42	5.24	1.8	2.4	5.2	ns
5c	Clock[1] fall to Enable Bytes Valid	1.97	2.59	5.69	1.9	2.5	5.5	ns
5d	Clock[1] fall to Enable Bytes Invalid	1.76	2.48	5.38	1.7	2.4	5.2	ns
6a	Clock[1] fall to Load Burst Address Valid	2.07	2.79	6.73	2.0	2.7	6.5	ns
6b	Clock[1] fall to Load Burst Address Invalid	1.97	2.79	6.83	1.9	2.7	6.6	ns
6c	Clock[1] rise to Load Burst Address Invalid	1.91	2.62	6.45	1.9	2.6	6.4	ns
7a	Clock[1] rise to Burst Clock rise	1.61	2.62	5.64	1.6	2.6	5.6	ns
7b	Clock[1]rise to Burst Clock fall	1.61	2.62	5.84	1.6	2.6	5.8	ns
7c	Clock[1] fall to Burst Clock rise	1.55	2.48	5.59	1.5	2.4	5.4	ns
7d	Clock[1] fall to Burst Clock fall	1.55	2.59	5.80	1.5	2.5	5.6	ns
8a	Read Data setup time	5.54	–	–	5.5	–	–	ns
8b	Read Data hold time	0	–	–	0	–	–	ns
9a	Clock[1] rise to Write Data Valid	1.81	2.72	6.85	1.8	2.7	6.8	ns
9b	Clock[1] fall to Write Data Invalid	1.45	2.48	5.69	1.4	2.4	5.5	ns
9c	Clock[1] rise to Write Data Invalid	1.63	–	–	1.62	–	–	ns
10a	$\overline{\text{DTACK}}$ setup time	2.52	–	–	2.5	–	–	ns

[1] Clock refers to the system clock signal, HCLK, generated from the System DPLL

4.4.1 $\overline{\text{DTACK}}$ Signal Description

The $\overline{\text{DTACK}}$ signal is the external input data acknowledge signal. When using the external $\overline{\text{DTACK}}$ signal as a data acknowledge signal, the bus time-out monitor generates a bus error when a bus cycle is not terminated by the external $\overline{\text{DTACK}}$ signal after 1022 HCLK counts have elapsed. Only the CS5 group supports DTACK signal function when the external DTACK signal is used for data acknowledgement.

4.4.2 $\overline{\text{DTACK}}$ Signal Timing

Figure 6 through Figure 9 show the access cycle timing used by chip-select 5. The signal values and units of measure for this figure are found in the associated tables.

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
7	Wait asserted to $\overline{RW}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{RW}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{EB}$ negated after $\overline{CS5}$ is negated	0.5T	0.5T+0.5	ns
11	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion can also be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.4 WAIT Write Cycle DMA Enabled

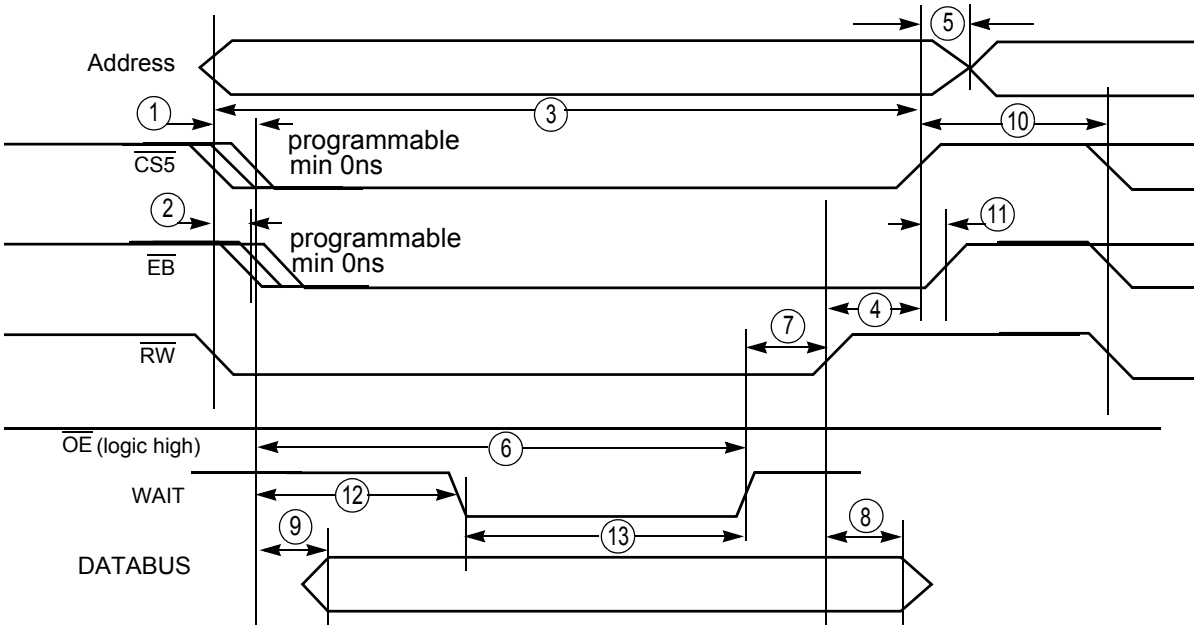


Figure 9. WAIT Write Cycle DMA Enabled

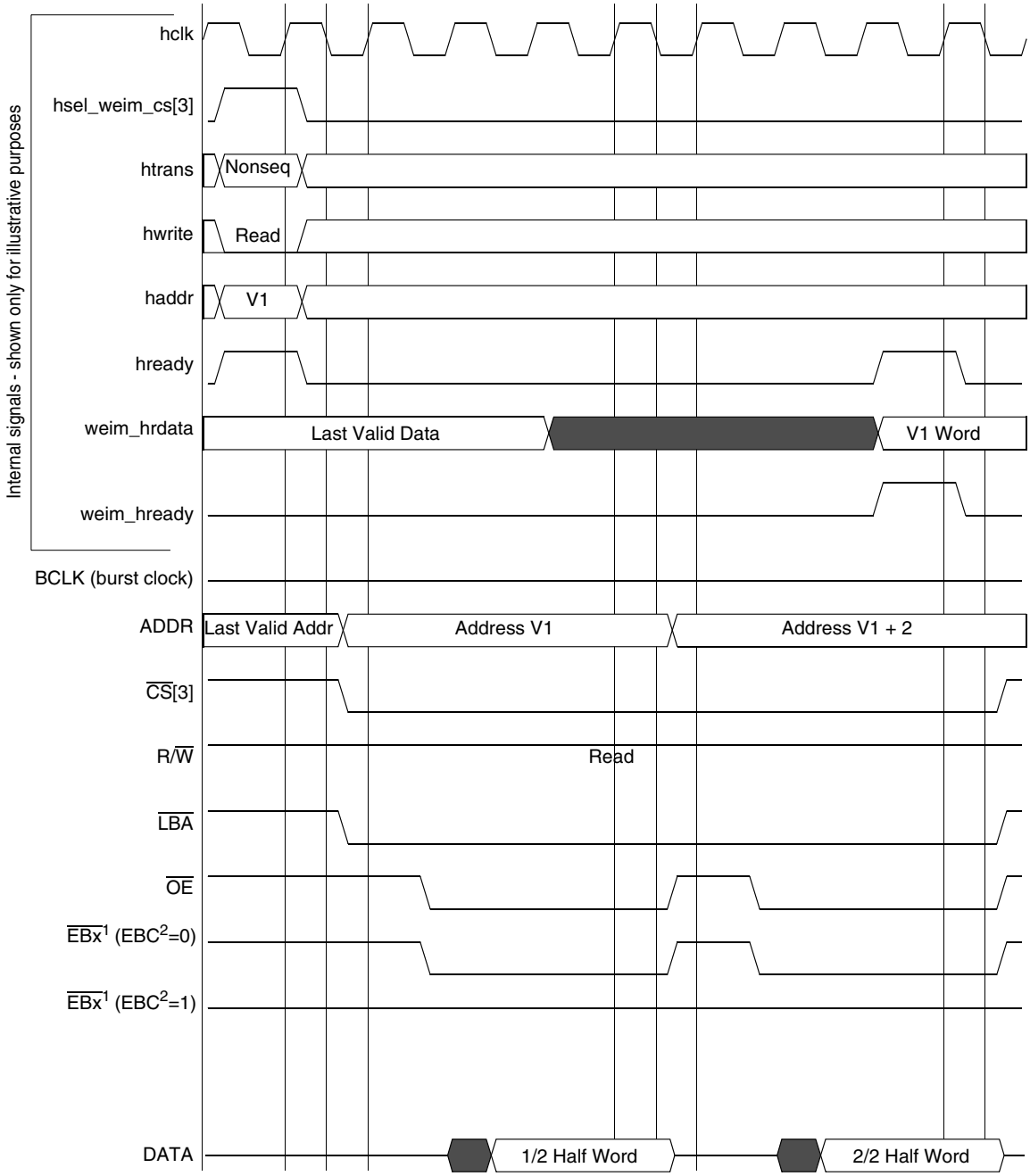
Table 16. WAIT Write Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	Address inactived after $\overline{CS}$ negated	–	0.09	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns
7	Wait asserted to $\overline{RW}$ negated	T+2.66	2T+7.96	ns
8	Data hold timing after $\overline{RW}$ negated	2T+0.03	–	ns
9	Data ready after $\overline{CS5}$ is asserted	–	T	ns
10	$\overline{CS}$ deactive to next $\overline{CS}$ active	T	–	ns
11	$\overline{EB}$ negate after $\overline{CS}$ negate	0.5T	0.5T+0.5	
12	Wait becomes low after $\overline{CS5}$ asserted	0	1019T	ns
13	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{CS5}$ assertion can be controlled by CSA bits. $\overline{EB}$ assertion also can be programmable by WEA bits in CS5L register.
3. Address becomes valid and $\overline{RW}$ asserts at the start of write access cycle.
4.The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.3 EIM External Bus Timing

The External Interface Module (EIM) is the interface to devices external to the i.MXL, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 5, and Table 12 defines the parameters of signals.



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF

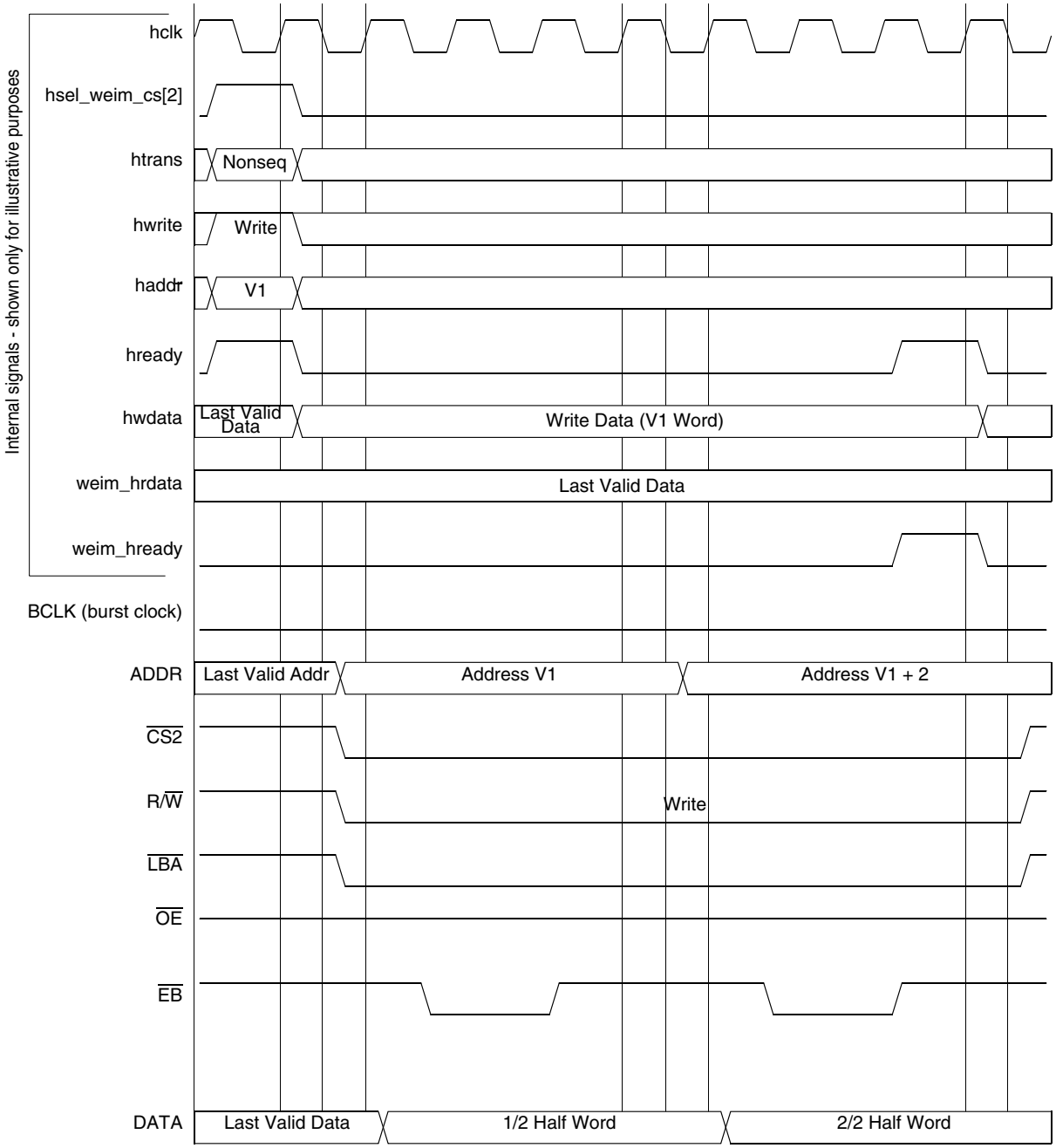
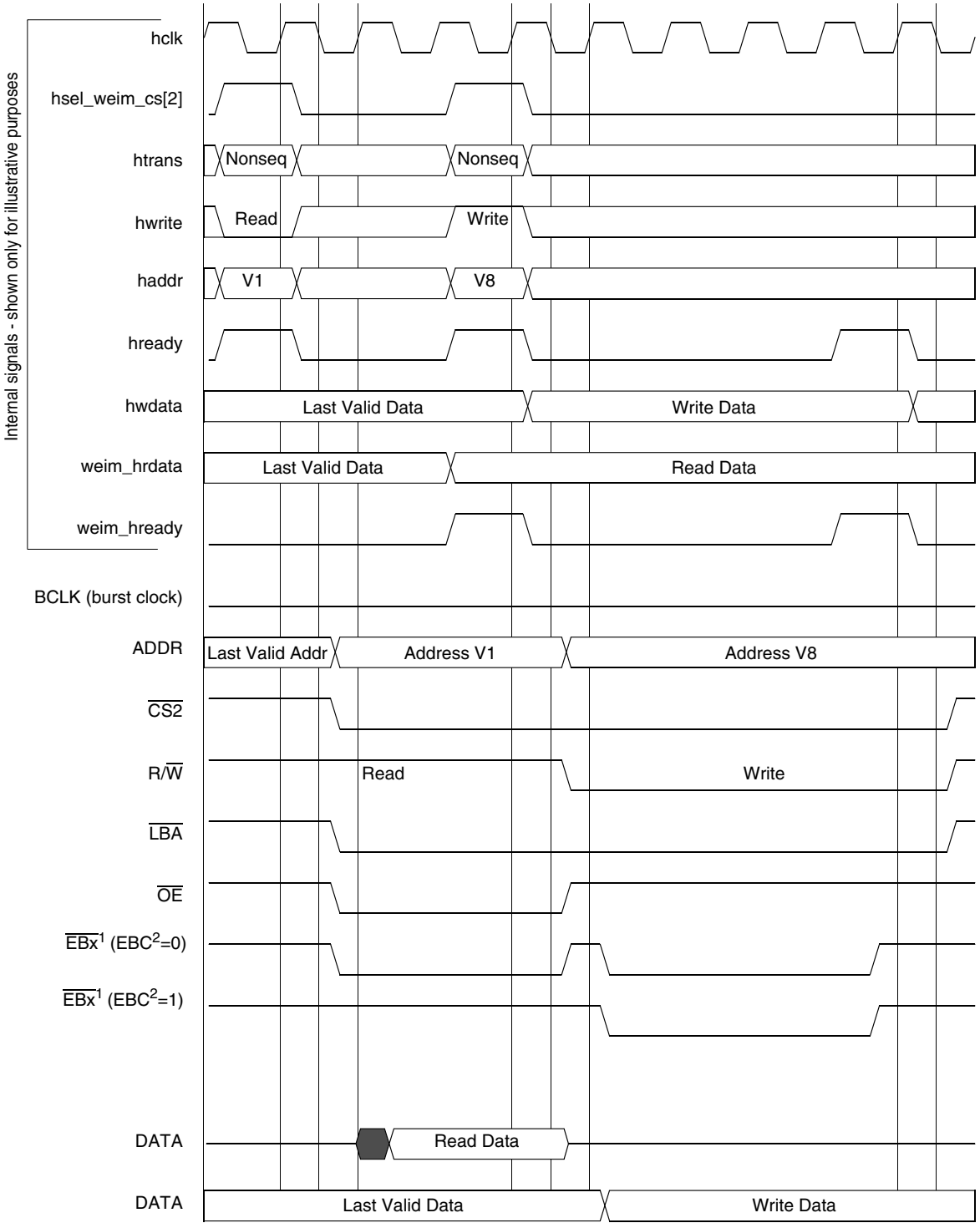


Figure 17. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 22. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF

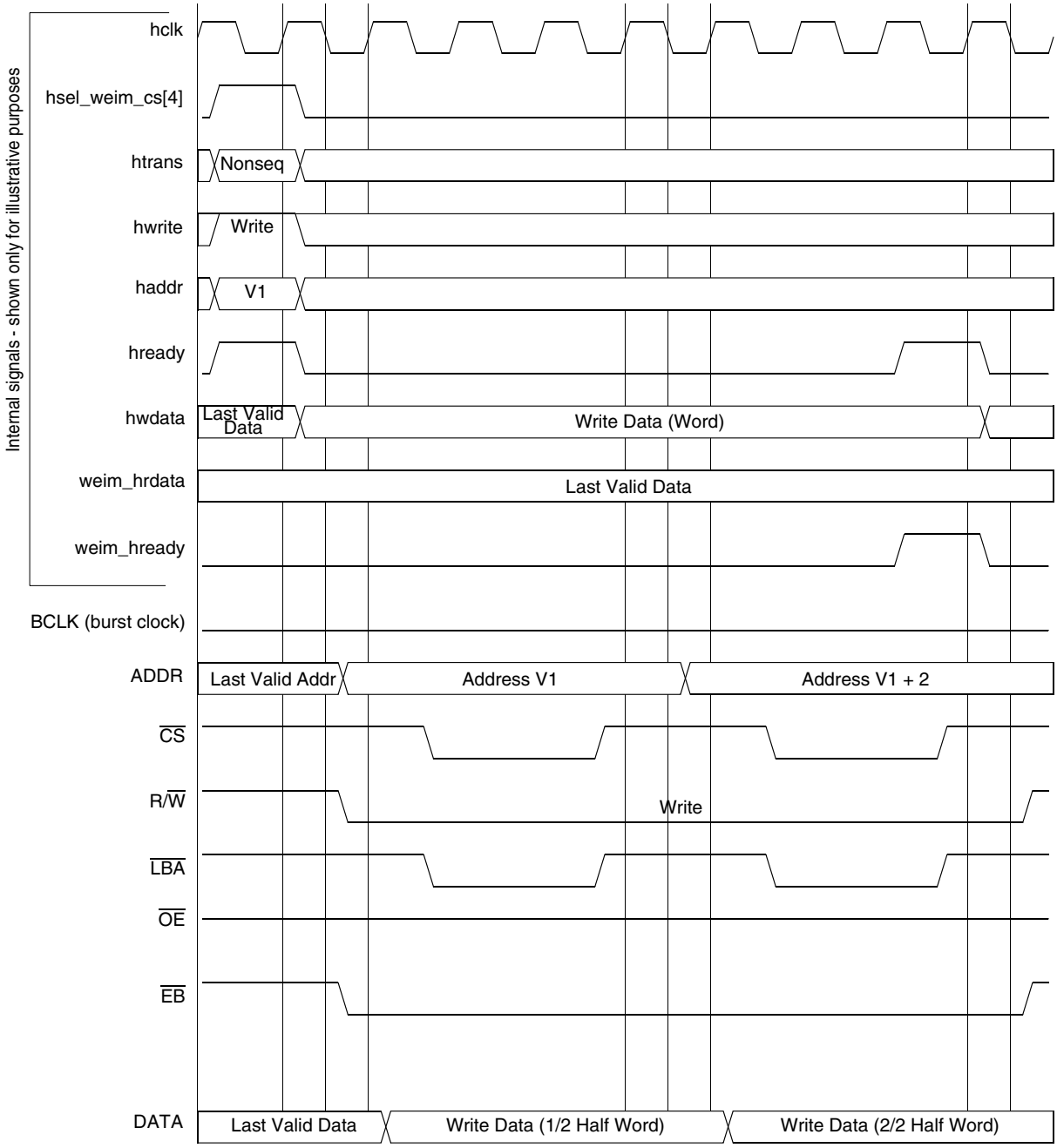
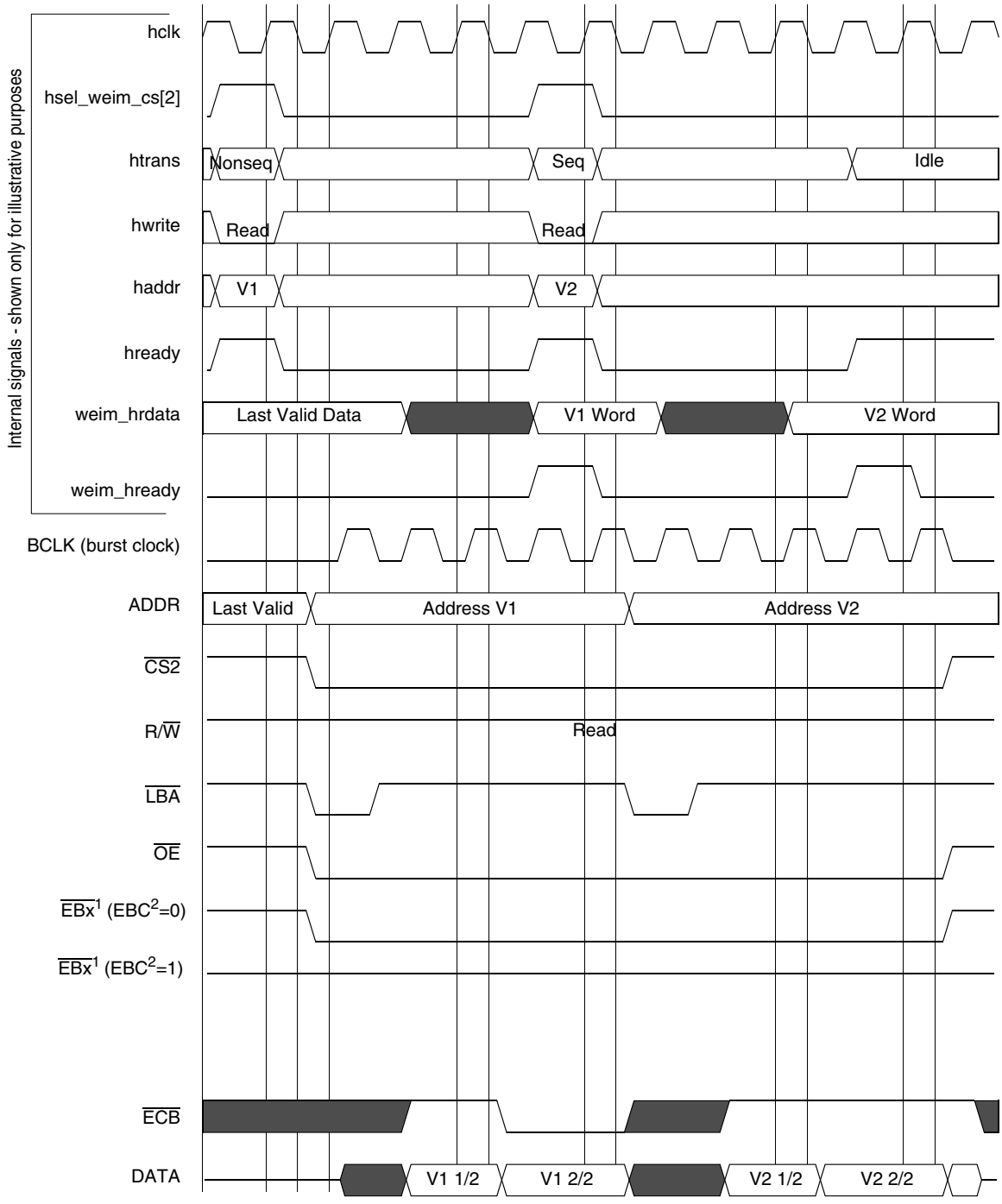


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 30. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF

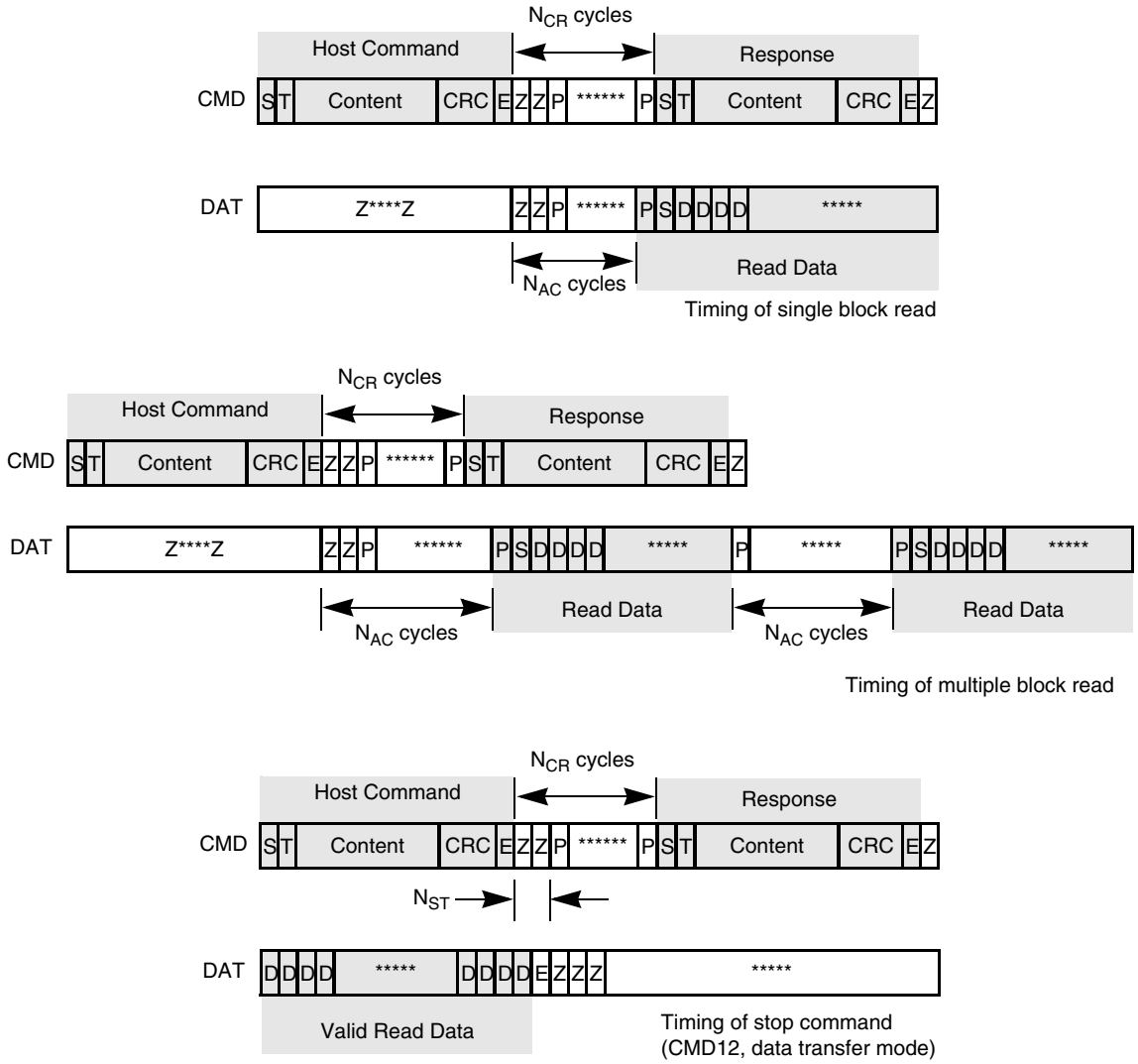


Figure 45. Timing Diagrams at Data Read

Figure 46 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after N_{WR} cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

Table 24. Timing Values for Figure 43 through Figure 47 (Continued)

Parameter	Symbol	Minimum	Maximum	Unit
Command read cycle	NRC	8	–	Clock cycles
Command-command cycle	NCC	8	–	Clock cycles
Command write cycle	NWR	2	–	Clock cycles
Stop transmission cycle	NST	2	2	Clock cycles
TAAC: Data read access time -1 defined in CSD register bit[119:112] NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104]				

4.7.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the “Interrupt Period” during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

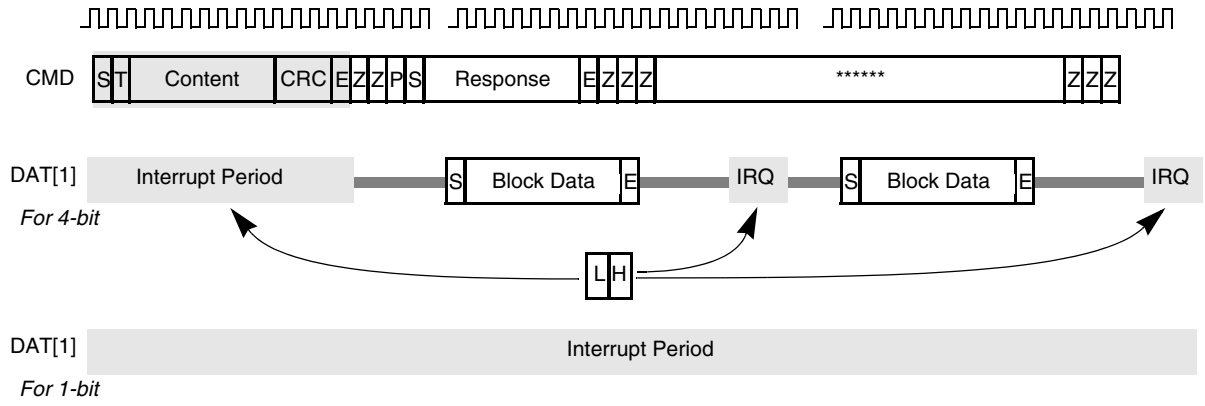


Figure 48. SDIO IRQ Timing Diagram

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

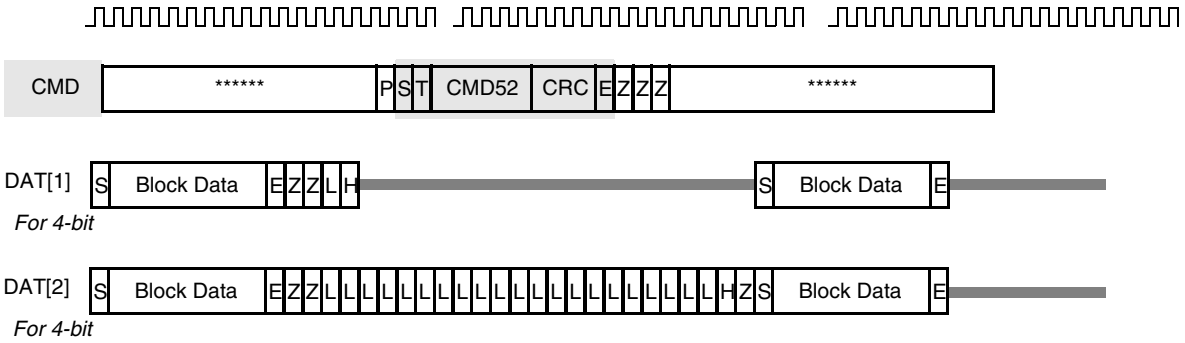


Figure 49. SDIO ReadWait Timing Diagram

4.8 Memory Stick Host Controller

The Memory Stick protocol requires three interface signal line connections for data transfers: MS_BS, MS_SDIO, and MS_SCLKO. Communication is always initiated by the MSHC and operates the bus in either four-state or two-state access mode.

The MS_BS signal classifies data on the SDIO into one of four states (BS0, BS1, BS2, or BS3) according to its attribute and transfer direction. BS0 is the INT transfer state, and during this state no packet transmissions occur. During the BS1, BS2, and BS3 states, packet communications are executed. The BS1, BS2, and BS3 states are regarded as one packet length and one communication transfer is always completed within one packet length (in four-state access mode).

The Memory Stick usually operates in four state access mode and in BS1, BS2, and BS3 bus states. When an error occurs during packet communication, the mode is shifted to two-state access mode, and the BS0 and BS1 bus states are automatically repeated to avoid a bus collision on the SDIO.

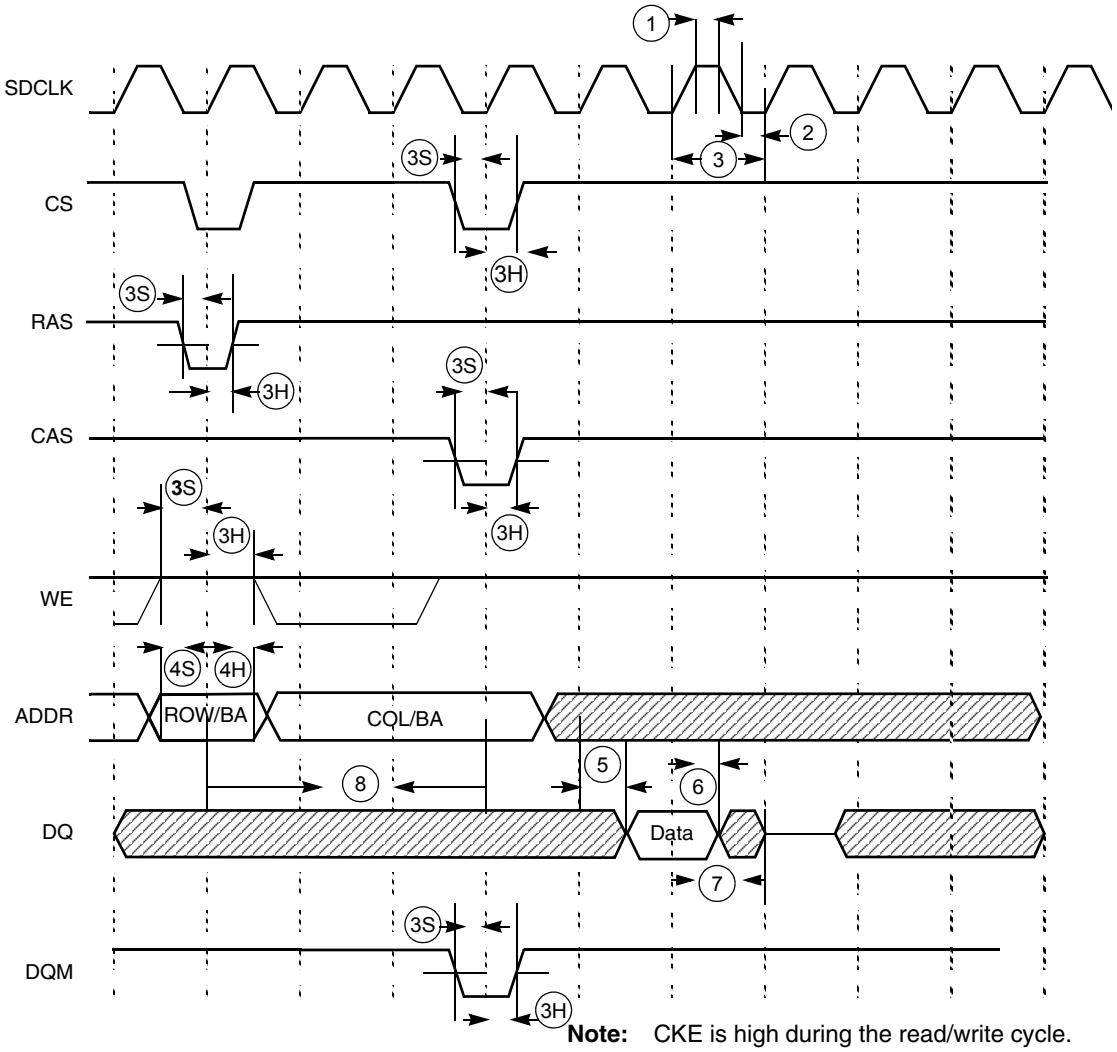
Table 26. PWM Output Timing Parameter Table (Continued)

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
3b	Clock rise time[1]	–	6.67	–	5/10	ns
4a	Output delay time[1]	5.7	–	5	–	ns
4b	Output setup time[1]	5.7	–	5	–	ns

[1] C_L of PWMO = 30 pF

4.10 SDRAM Controller

This section shows timing diagrams and parameters associated with the SDRAM (synchronous dynamic random access memory) Controller.



Note: CKE is high during the read/write cycle.

Figure 52. SDRAM Read Cycle Timing Diagram

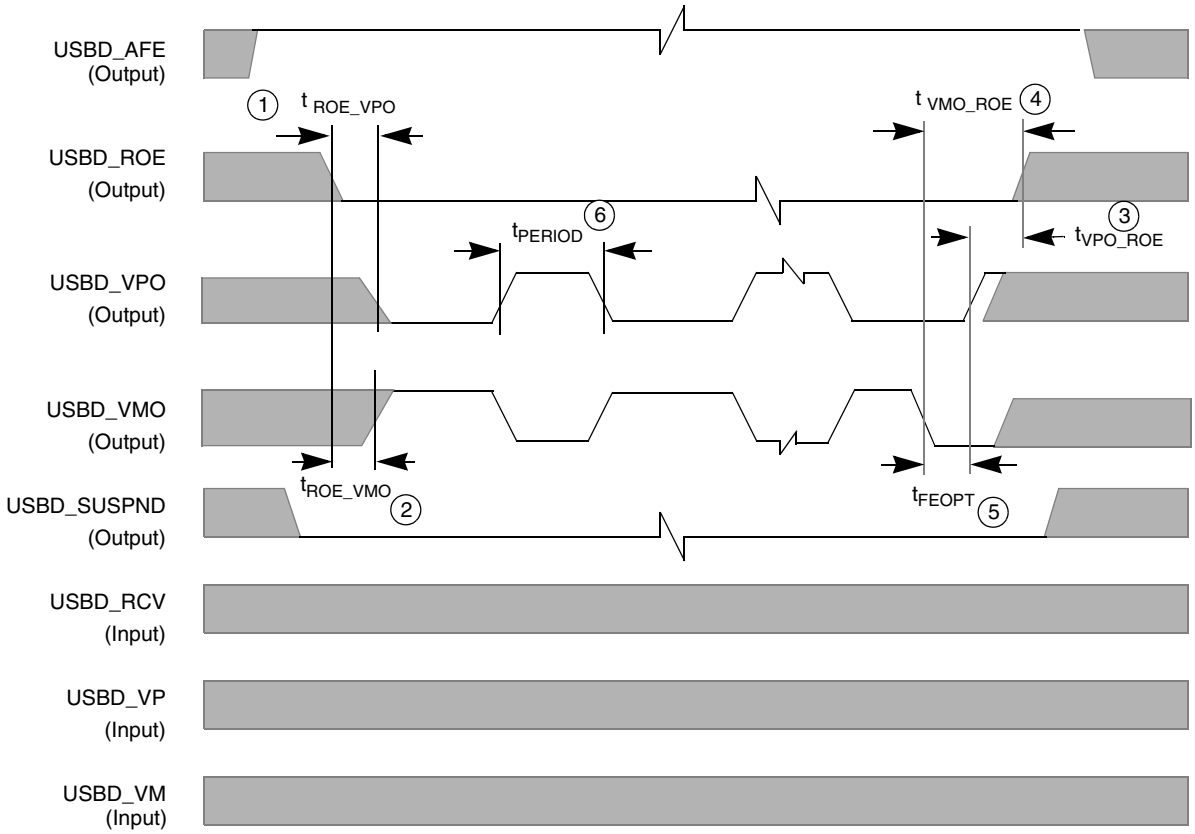


Figure 56. USB Device Timing Diagram for Data Transfer to USB Transceiver (TX)

Table 30. USB Device Timing Parameters for Data Transfer to USB Transceiver (TX)

Ref No.	Parameter	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	t_{ROE_VPO}; USBD_ROE active to USBD_VPO low	83.14	83.47	ns
2	t_{ROE_VMO}; USBD_ROE active to USBD_VMO high	81.55	81.98	ns
3	t_{VPO_ROE}; USBD_VPO high to USBD_ROE deactivated	83.54	83.80	ns
4	t_{VMO_ROE}; USBD_VMO low to USBD_ROE deactivated (includes SE0)	248.90	249.13	ns
5	t_{FEOPT}; SE0 interval of EOP	160.00	175.00	ns
6	t_{PERIOD}; Data transfer rate	11.97	12.03	Mb/s

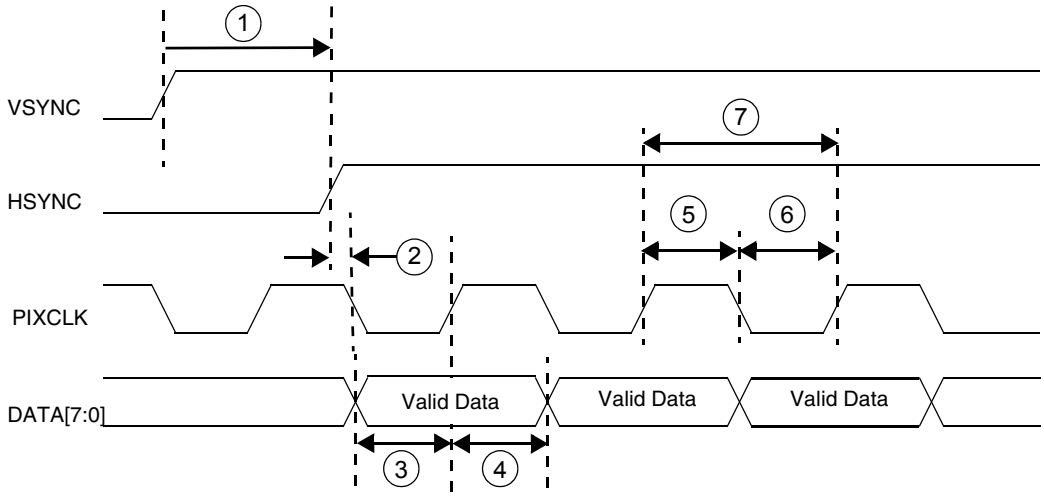


Figure 63. Sensor Output Data on Pixel Clock Falling Edge CSI Latches Data on Pixel Clock Rising Edge

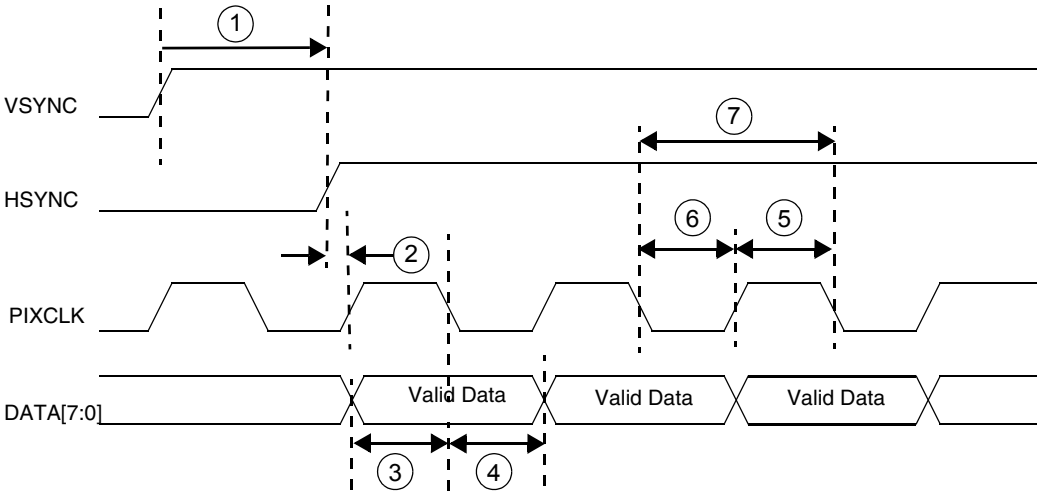


Figure 64. Sensor Output Data on Pixel Clock Rising Edge CSI Latches Data on Pixel Clock Falling Edge

Table 35. Gated Clock Mode Timing Parameters

Ref No.	Parameter	Min	Max	Unit
1	csi_vsync to csi_hsync	180	–	ns
2	csi_hsync to csi_pixclk	1	–	ns
3	csi_d setup time	1	–	ns
4	csi_d hold time	1	–	ns
5	csi_pixclk high time	10.42	–	ns
6	csi_pixclk low time	10.42	–	ns
7	csi_pixclk frequency	0	48	MHz

Table 38 illustrates the package pin assignments for the 225-contact MAPBGA package. For a complete listing of signals, see the Signal Multiplexing Table 3 on page 9.

Table 38. i.MXL 225 MAPBGA Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	SD_CMD	PB15	PB19	USBD_ROE	USBD_SUSPND	USBD_VM	SSI_RXFS	SSI_TXCLK	SPI1_SPI_RDY	SPI1_SCLK	REV	PS	LD2	LD4	LD5	**A**
B	SD_DAT3	SD_CLK	PB16	USBD_AFE	USBD_RCV	USBD_VMO	SSI_RXDAT	UART1_TXD	SPI1_SS	LSCLK	SPL_SPR	LD0	LD3	LD6	LD7	**B**
C	D31	SD_DAT0	PB14	PB18	SD_DAT2	USBD_VPO	UART2_RXD	SSI_TXFS	UART1_RTS	CONTRAST	FLM/VSYNC	LD8	LD9	LD12	NVDD2	**C**
D	A23	A24	SD_DAT1	PB17	NVDD1	USBD_VP	QVDD4	UART2_TXD	NVDD3	SPI1_MOSI	LP/HSYNC	LD1	LD11	TMR2OUT	LD13	**D**
E	A21	A22	D30	D29	NVDD1	QVSS	UART2_RTS	UART1_RXD	UART1_CTS	SPI1_MISO	ACD/OE	LD10	TIN	CSI_D0	CSI_MCLK	**E**
F	A20	A19	D28	D27	NVDD1	NVDD1	UART2_CTS	SSI_RXCLK	SSI_TXDAT	CLS	QVDD3	LD14	LD15	CSI_D2	CSI_D4	**F**
G	A17	A18	D26	D25	NVDD1	NVSS	NVDD4	NVSS	NVSS	QVSS	PWMO	CSI_D3	CSI_D7	CSI_HSYNC	CSI_D5	**G**
H	A15	A16	D23	D24	D22	NVSS	NVSS	NVSS	NVSS	NVDD2	CSI_D1	CSI_VSYNC	CSI_PIXCLK	I2C_SDA	TMS	**H**
J	A14	A12	D21	D20	NVDD1	NVSS	NVSS	QVDD1	NVSS	CSI_D6	I2C_SCL	TCK	TDO	BOOT1	BOOT0	**J**
K	A13	A11	CS2	D19	NVDD1	NVSS	QVSS	NVDD1	NVSS	D1	BOOT2	TDI	BIG_ENDIAN	RESET_OUT	XTAL32K	**K**
L	A10	A9	D17	D18	NVDD1	NVDD1	CS5	D2	ECB	NVSS	NVSS	POR	QVSS	XTAL16M	EXTAL32K	**L**
M	D16	D15	D13	D10	EB3	NVDD1	CS4	CS1	BCLK[1]	RW	NVSS	BOOT3	QVDD2	RESET_IN	EXTAL16M	**M**
N	A8	A7	D12	EB0	D9	D8	CS3	CS0	PA17	D0	DQM2	DQM0	SDCKE0	TRISTATE	TRST	**N**
P	D14	A5	A4	A3	A2	A1	D6	D5	MA10	MA11	DQM1	RAS	SDCKE1	CLKO	RESET_SF[2]	**P**
R	A6	D11	EB1	EB2	OE	D7	A0	SDCLK	D4	LBA	D3	DQM3	CAS	SDWE	AVDD1	**R**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	

1 Burst Clock

2 This signal is not used and should be floated in an actual application.