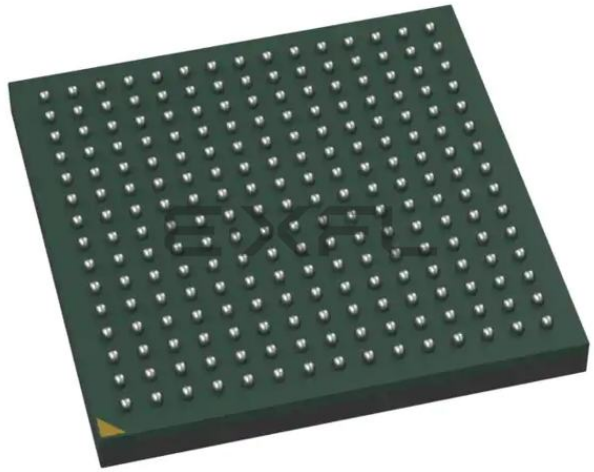

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM920T
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD
Ethernet	-
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 3.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	225-LFBGA
Supplier Device Package	225-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9328mxlvp20r2

- Video Port
- General-Purpose I/O (GPIO) Ports
- Bootstrap Mode
- Multimedia Accelerator (MMA)
- Power Management Features
- Operating Voltage Range: 1.7 V to 1.9 V core, 1.7 V to 3.3 V I/O
- 256-pin MAPBGA Package
- 225-contact MAPBGA Package

1.2 Target Applications

The i.MXL processor is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers, and messaging applications.

1.3 Ordering Information

Table 1 provides ordering information.

Table 1. i.MXL Ordering Information

Package Type	Frequency	Temperature	Solderball Type	Order Number
256-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MXLVM20(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVM20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MXLVM15(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVM15(R2)
		-40°C to 85°C	Pb-free	MC9328MXLCVM15(R2)
225-lead MAPBGA	200 MHz	0°C to 70°C	Pb-free	MC9328MXLVP20(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVP20(R2)
	150 MHz	0°C to 70°C	Pb-free	MC9328MXLVP15(R2)
		-30°C to 70°C	Pb-free	MC9328MXLDVP15(R2)
		-40°C to 85°C	Pb-free	MC9328MXLCVP15(R2)

1.4 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
CLS	Start signal output for gate driver. This signal is an inverted version of PS (Sharp panel dedicated signal).
REV	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
SPI 1 and SPI 2	
SPI1_MOSI	Master Out/Slave In
SPI1_MISO	Slave In/Master Out
SPI1_$\overline{SS}$	Slave Select (Selectable polarity)
SPI1_SCLK	Serial Clock
SPI1_$\overline{SPI_RDY}$	Serial Data Ready
SPI2_TXD	SPI2 Master TxData Output—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MXL Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_RXD	SPI2 Master RxData Input—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MXL Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_$\overline{SS}$	SPI2 Slave Select—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MXL Reference Manual* for information about how to bring this signal to the assigned pin.
SPI2_SCLK	SPI2 Serial Clock—This signal is multiplexed with a GPI/O pin yet shows up as a primary or alternative signal in the signal multiplex scheme table. Please refer to the SPI and GPIO chapters in the *MC9328MXL Reference Manual* for information about how to bring this signal to the assigned pin.
General Purpose Timers	
TIN	Timer Input Capture or Timer Input Clock—The signal on this input is applied to both timers simultaneously.
TMR2OUT	Timer 2 Output
USB Device	
USBD_VMO	USB Minus Output
USBD_VPO	USB Plus Output
USBD_VM	USB Minus Input
USBD_VP	USB Plus Input
USBD_SUSPND	USB Suspend Output
USBD_RCV	USB Receive Data
$\overline{USBD\_ROE}$	USB $\overline{OE}$
USBD_AFE	USB Analog Front End Enable
Secure Digital Interface	
SD_CMD	SD Command—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 4.7K–69K external pull up resistor must be added.
SD_CLK	MMC Output Clock

Table 2. i.MXL Signal Descriptions (Continued)

Signal Name	Function/Notes
SD_DAT [3:0]	Data—If the system designer does not wish to make use of the internal pull-up, via the Pull-up enable register, a 50K–69K external pull up resistor must be added.
Memory Stick Interface	
MS_BS	Memory Stick Bus State (Output)—Serial bus control signal
MS_SDIO	Memory Stick Serial Data (Input/Output)
MS_SCLKO	Memory Stick Serial Clock (Input)—Serial protocol clock source for SCLK Divider
MS_SCLKI	Memory Stick External Clock (Output)—Test clock input pin for SCLK divider. This pin is only for test purposes, not for use in application mode.
MS_PI0	General purpose Input0—Can be used for Memory Stick Insertion/Extraction detect
MS_PI1	General purpose Input1—Can be used for Memory Stick Insertion/Extraction detect
UARTs – IrDA/Auto-Bauding	
UART1_RXD	Receive Data
UART1_TXD	Transmit Data
$\overline{\text{UART1\_RTS}}$	Request to Send
$\overline{\text{UART1\_CTS}}$	Clear to Send
UART2_RXD	Receive Data
UART2_TXD	Transmit Data
$\overline{\text{UART2\_RTS}}$	Request to Send
$\overline{\text{UART2\_CTS}}$	Clear to Send
$\overline{\text{UART2\_DSR}}$	Data Set Ready
$\overline{\text{UART2\_RI}}$	Ring Indicator
$\overline{\text{UART2\_DCD}}$	Data Carrier Detect
$\overline{\text{UART2\_DTR}}$	Data Terminal Ready
Serial Audio Port – SSI (configurable to I^2S protocol)	
SSI_TXDAT	Transmit Data
SSI_RXDAT	Receive Data
SSI_TXCLK	Transmit Serial Clock
SSI_RXCLK	Receive Serial Clock
SSI_TXFS	Transmit Frame Sync
SSI_RXFS	Receive Frame Sync
I^2C	
I2C_SCL	I^2C Clock
I2C_SDA	I^2C Data

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull-Up				
NVDD1	N11	T9	DQM2	O									
NVDD1	P11	N9	DQM1	O									
NVDD1	N12	R10	DQM0	O									
NVDD1	P12	M9	$\overline{RAS}$	O									
NVDD1	R13	L8	$\overline{CAS}$	O									
NVDD1	R14	T10	$\overline{SDWE}$	O									
NVDD1	N13	R11	SDCKE0	O									
NVDD1	P13	P10	SDCKE1	O									
NVDD1	P15	N10	$\overline{RESET\_SF}$	O									
NVDD1	P14	T11	CLKO	O									
AVDD1	R15	T12	AVDD1	Static									
QVDD2	M13	R15	QVDD2	Static									
AVDD1	N15	P13	$\overline{TRST}$	I	69K								
AVDD1	N14	T13	TRISTATE[1]	I									
AVDD1	M15	T14	EXTAL16M	I									
AVDD1	L14	T15	XTAL16M	O									
AVDD1	L15	R16	EXTAL32K	I									
AVDD1	K15	P16	XTAL32K	O									
AVDD1	M14	M10	$\overline{RESET\_IN}$[2]	I	69K								
AVDD1	K14	N11	$\overline{RESET\_OUT}$	O									
AVDD1	L12	R12	POR[2]	I									
AVDD1	K13	M11	BIG_ENDIAN[3]	I									
AVDD1	M12	P11	BOOT3[3]	I									
AVDD1	K11	N12	BOOT2[3]	I									
AVDD1	J14	R13	BOOT1[3]	I									
AVDD1	J15	P12	BOOT0[3]	I									
NVDD2	J13	R14	$\overline{TDO}$[4]	O									
NVDD2	H15	N15	TMS	I	69K								
NVDD2	J12	L9	TCK	I	69K								
NVDD2	K12	N16	TDI	I	69K								
NVDD2	J11	P14	I2C_SCL	O				PA16	69K				PA16
NVDD2	H14	P15	I2C_SDA	I/O				PA15	69K				PA15

Table 3. MC9328MXLMC9328MXS Signal Multiplexing Scheme (Continued)

I/O Supply Voltage	225 BGA Ball	256 BGA Ball	Primary			Alternate		GPIO		AIN	BIN	AOUT	Default
			Signal	Dir	Pull-Up	Signal	Dir	Mux	Pull -Up				
NVDD1	F5	J5	NVDD	Static									
	J6	K6	NVSS	Static									
NVDD1	G5	K5	NVDD1	Static									
	K6	M6	NVSS	Static									
NVDD1	J5	H6	NVDD1	Static									
	H7	J7	NVSS	Static									
NVDD1	K5	L6	NVDD1	Static									
	J7	J7	NVSS	Static									
NVDD1	L5	L6	NVDD1	Static									
	G8	K7	NVSS	Static									
NVDD1	L5	J8	NVDD1	Static									
	H8	L7	NVSS	Static									
	K7	T16	QVSS	Static									
NVDD2	H10	K10	NVDD2	Static									
	G9	J10	NVSS	Static									
QVDD3	F11	J15	QVDD3	Static									
	G10	J16	QVSS	Static									
NVDD2	C15	K9	NVDD2	Static									
	H9	J9	NVSS	Static									
QVDD4	D7	A13	QVDD4	Static									
	L13	B13	QVSS	Static									
NVDD3	D9	A10	NVDD3	Static									
	J9	A7	NVSS	Static									
	K9	A4	NVSS	Static									
NVDD4	G7	A6	NVDD4	Static									
NVDD1	F6		NVDD1	Static									
NVDD1	L6		NVDD1	Static									
NVDD1	M6		NVDD1	Static									
NVDD1	K8		NVDD1	Static									
	L10		NVSS	Static									
	L11		NVSS	Static									
	M11		NVSS	Static									

1 Pull down this input with 1KΩ resistor to GND.

2 External circuit required to drive this input.

3 Tie this input high (to AVDD) or pull down with 1KΩ resistor to GND.

4 Pull up this output with a resistor to NVDD2.

4 Functional Description and Application Information

This section provides the electrical information including and timing diagrams for the individual modules of the i.MXL.

4.1 Embedded Trace Macrocell

All registers in the ETM9 are programmed through a JTAG interface. The interface is an extension of the ARM920T processor's TAP controller, and is assigned scan chain 6. The scan chain consists of a 40-bit shift register comprised of the following:

- 32-bit data field
- 7-bit address field
- A read/write bit

The data to be written is scanned into the 32-bit data field, the address of the register into the 7-bit address field, and a 1 into the read/write bit.

A register is read by scanning its address into the address field and a 0 into the read/write bit. The 32-bit data field is ignored. A read or a write takes place when the TAP controller enters the UPDATE-DR state. The timing diagram for the ETM9 is shown in Figure 2. See Table 9 for the ETM9 timing parameters used in Figure 2.

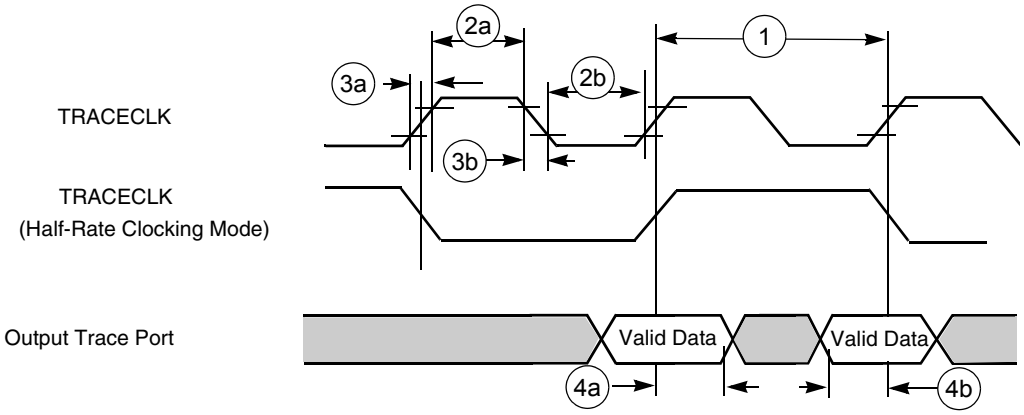


Figure 2. Trace Port Timing Diagram

Table 9. Trace Port Timing Diagram Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	CLK frequency	0	85	0	100	MHz
2a	Clock high time	1.3	–	2	–	ns
2b	Clock low time	3	–	2	–	ns
3a	Clock rise time	–	4	–	3	ns
3b	Clock fall time	–	3	–	3	ns

Table 14. DTACK WAIT Read Cycle DMA Enabled: WSC = 111111, DTACK_SEL=1, HCLK=96MHz (Continued)

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
12	Wait pulse width	1T	1020T	ns

Note:
1. T is the system clock period. (For 96 MHz system clock, T=10.42 ns)
2. $\overline{OE}$ and $\overline{EB}$ assertion time is programmable by OEA bit in CS5L register. $\overline{EB}$ assertion in read cycle will occur only when EBC bit in CS5L register is clear.
3. Address becomes valid and $\overline{CS}$ asserts at the start of read access cycle.
4. The external wait input requirement is eliminated when $\overline{CS5}$ is programmed to use internal wait state.

4.4.2.3 WAIT Write Cycle without DMA

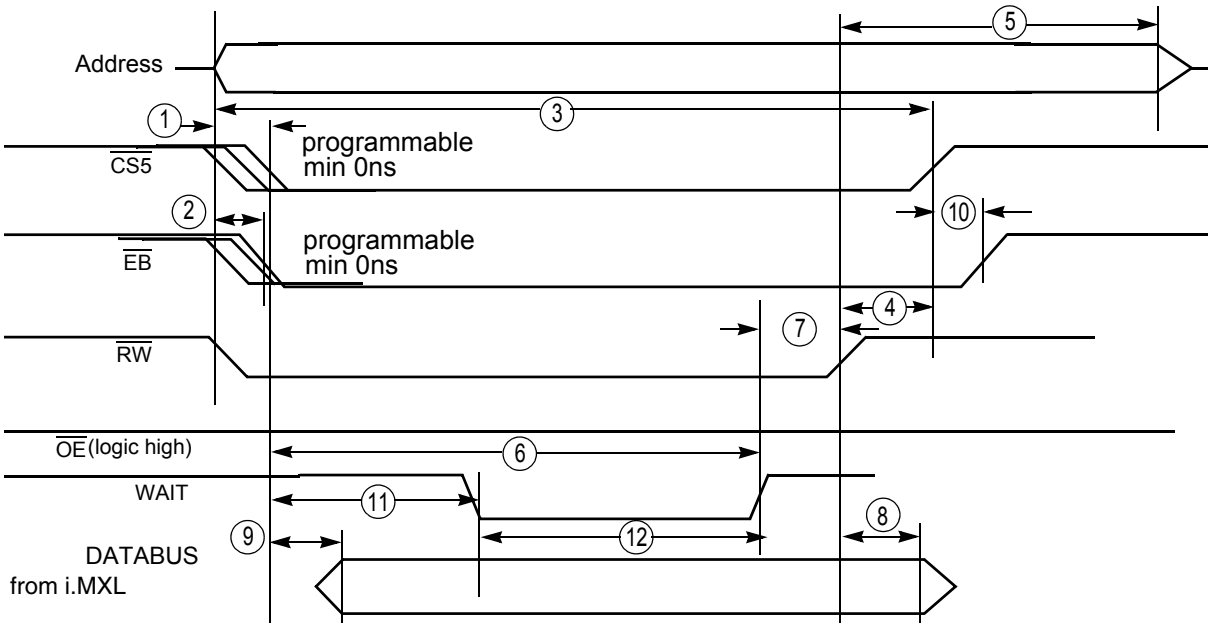
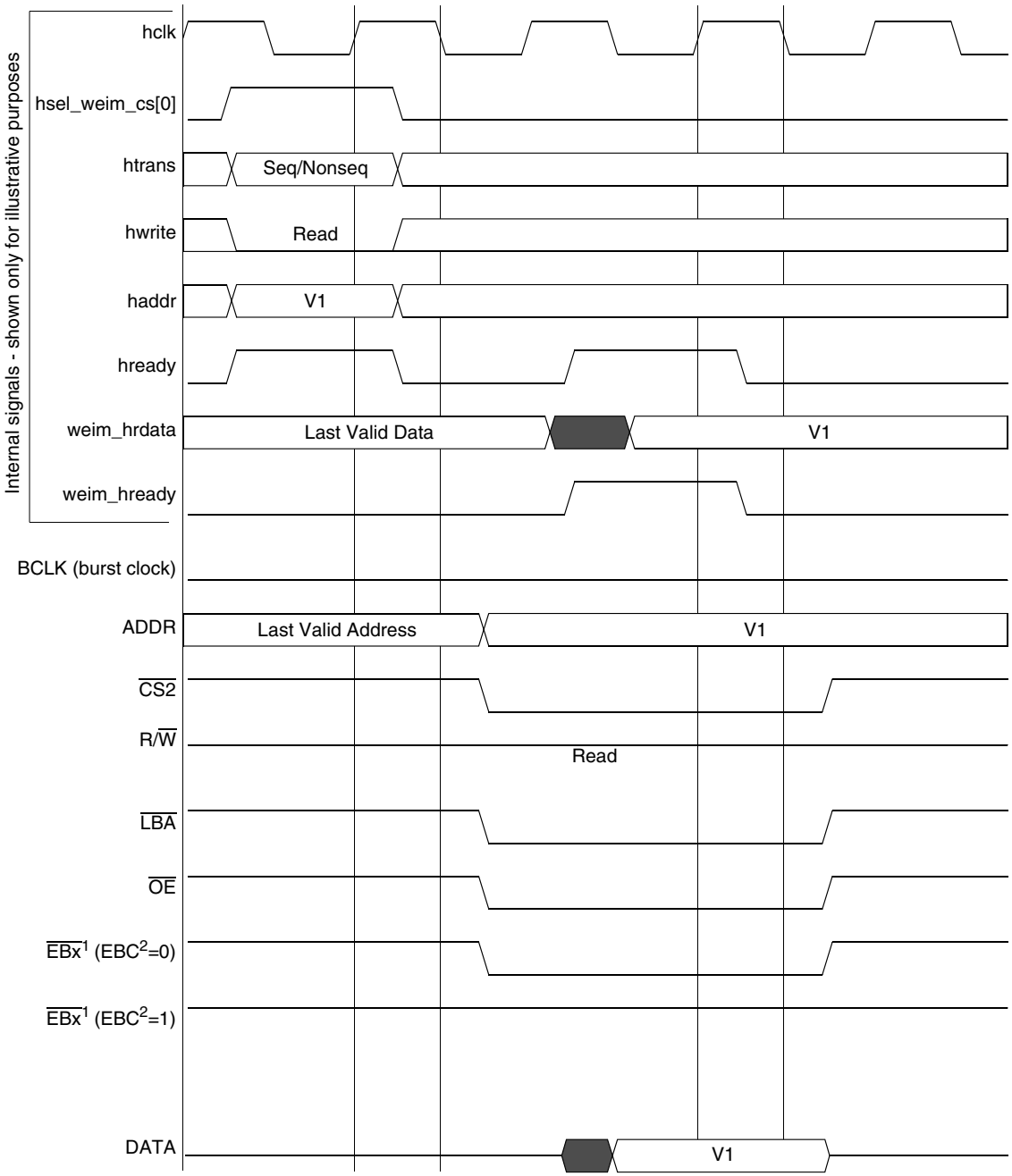


Figure 8. WAIT Write Cycle without DMA

Table 15. WAIT Write Cycle without DMA: WSC = 111111, DTACK_SEL=1, HCLK=96MHz

Number	Characteristic	3.0 ± 0.3 V		Unit
		Minimum	Maximum	
1	$\overline{CS5}$ assertion time	See note 2	–	ns
2	$\overline{EB}$ assertion time	See note 2	–	ns
3	$\overline{CS5}$ pulse width	3T	–	ns
4	$\overline{RW}$ negated before $\overline{CS5}$ is negated	2.5T-3.63	2.5T-1.16	ns
5	$\overline{RW}$ negated to Address inactive	64.22	–	ns
6	Wait asserted after $\overline{CS5}$ asserted	–	1020T	ns



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 10. WSC = 1, A.HALF/E.HALF

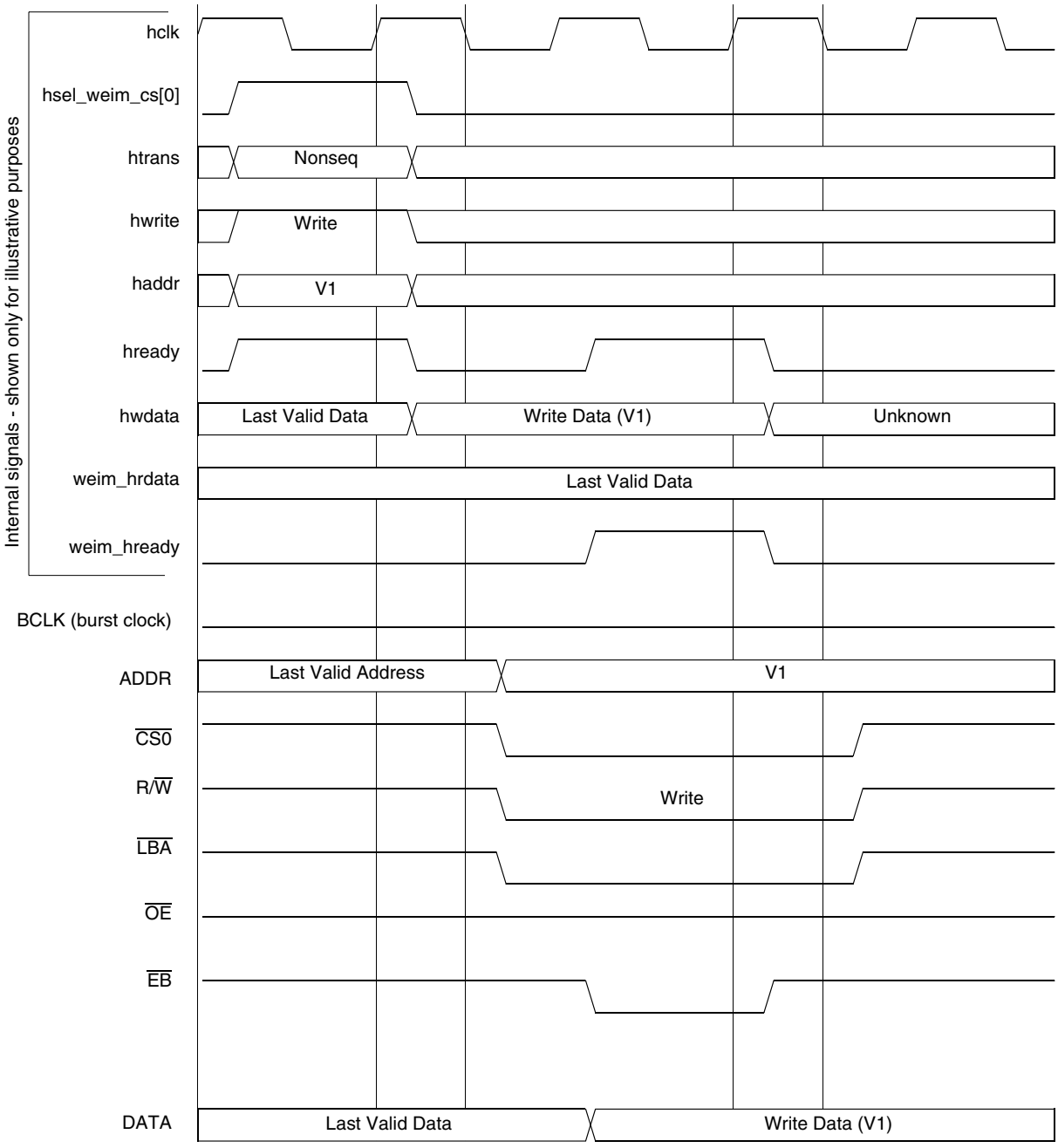
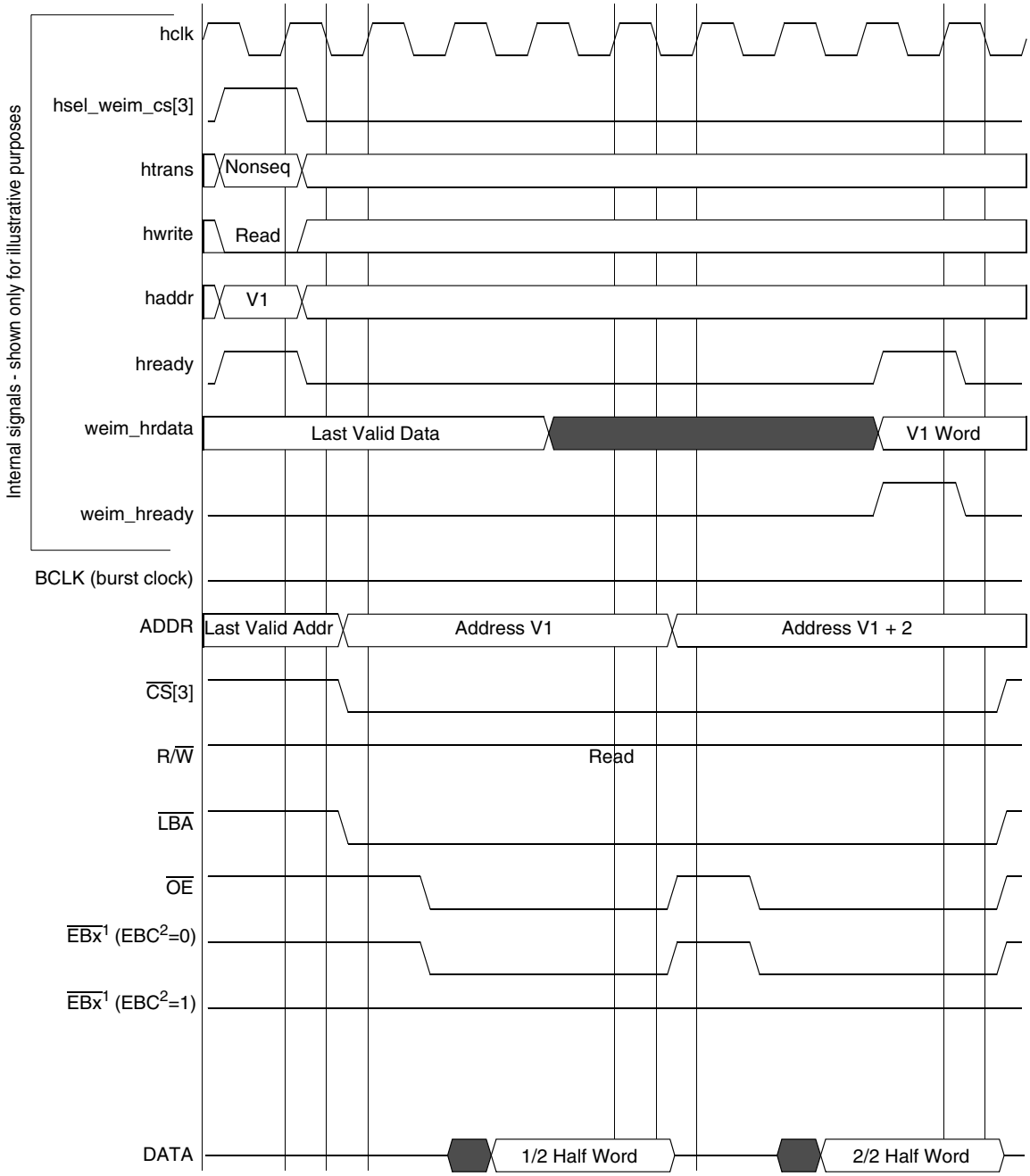


Figure 11. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 14. WSC = 3, OEA = 2, A.WORD/E.HALF

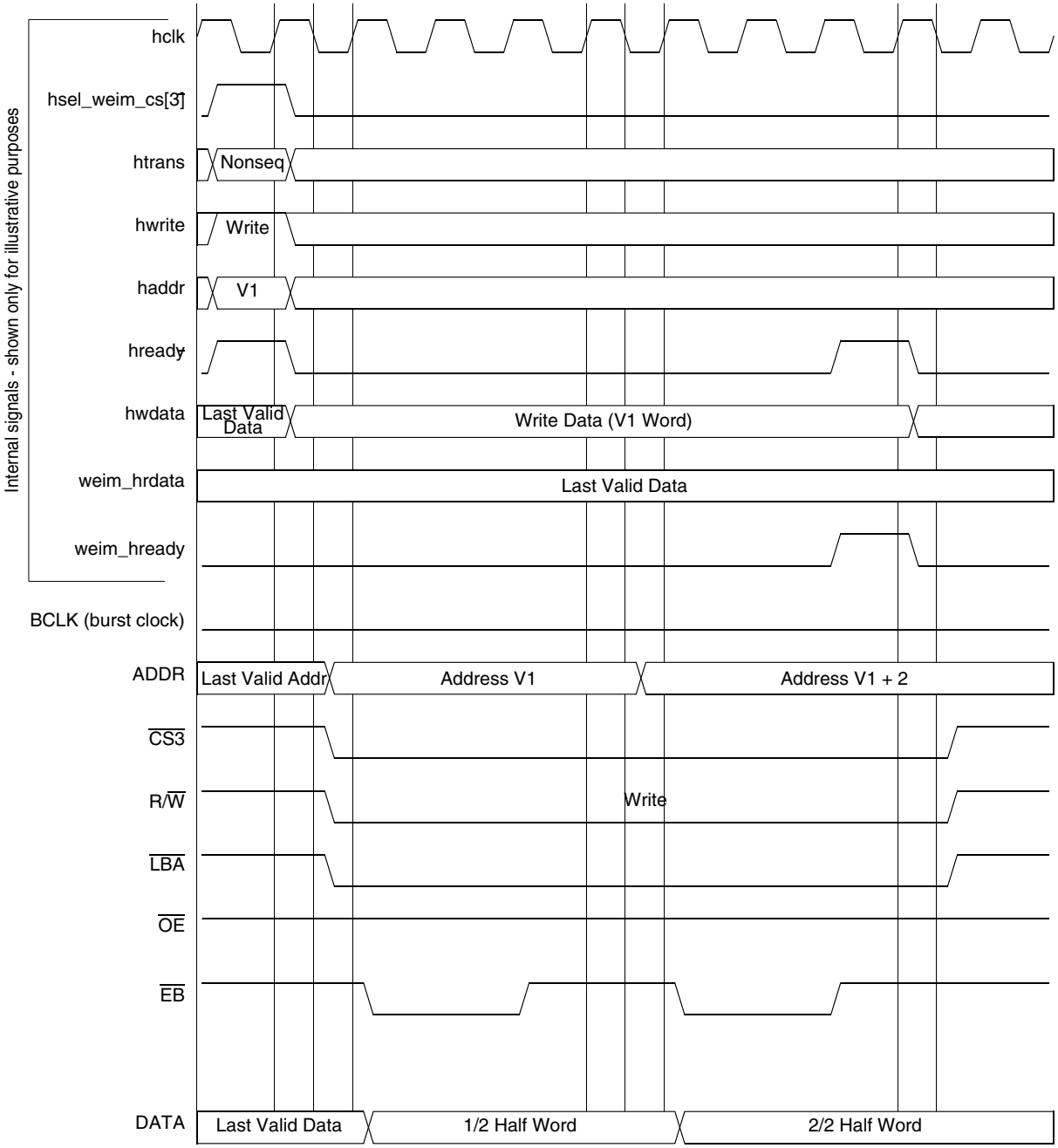
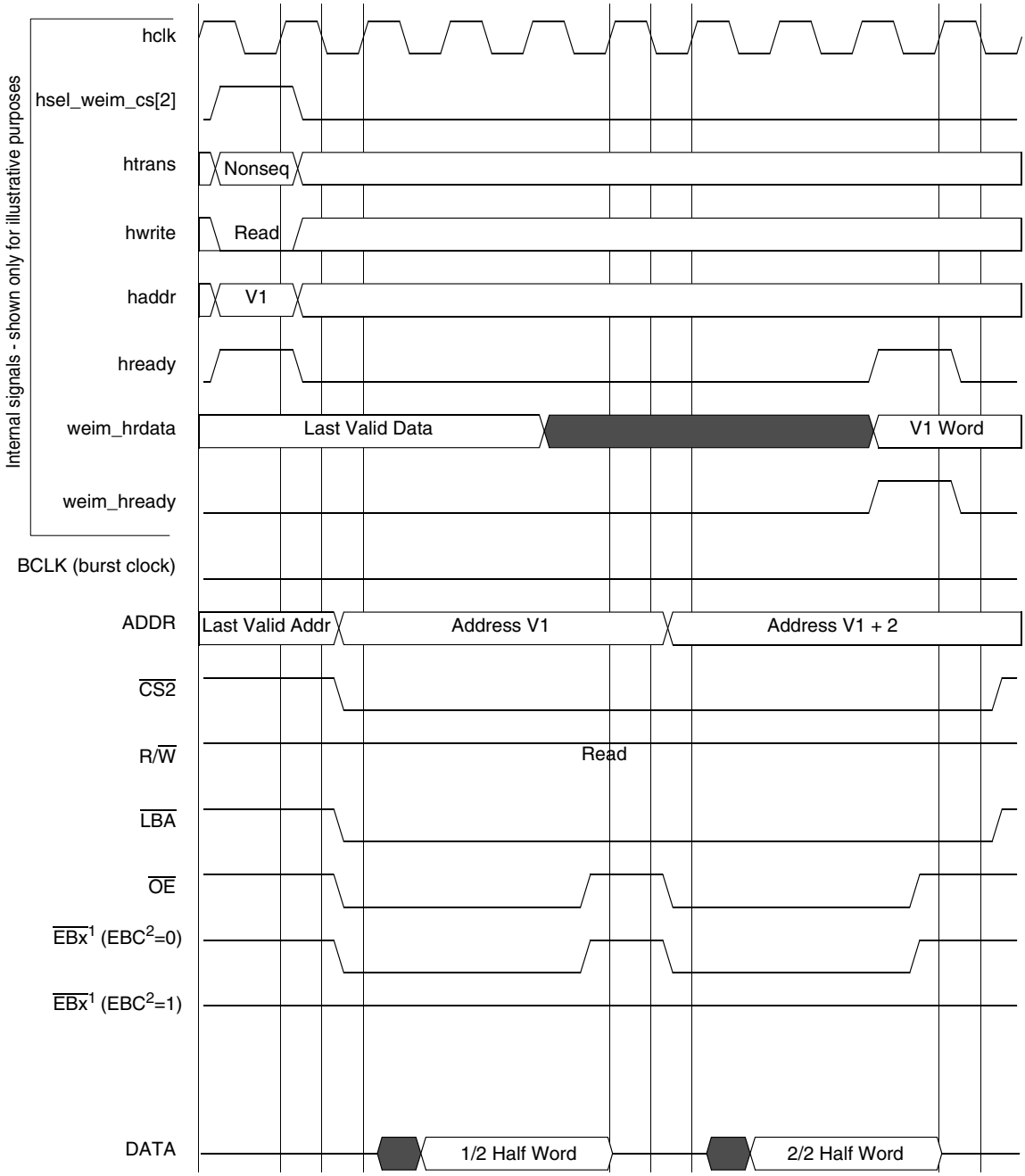


Figure 15. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 18. WSC = 3, OEN = 2, A.WORD/E.HALF

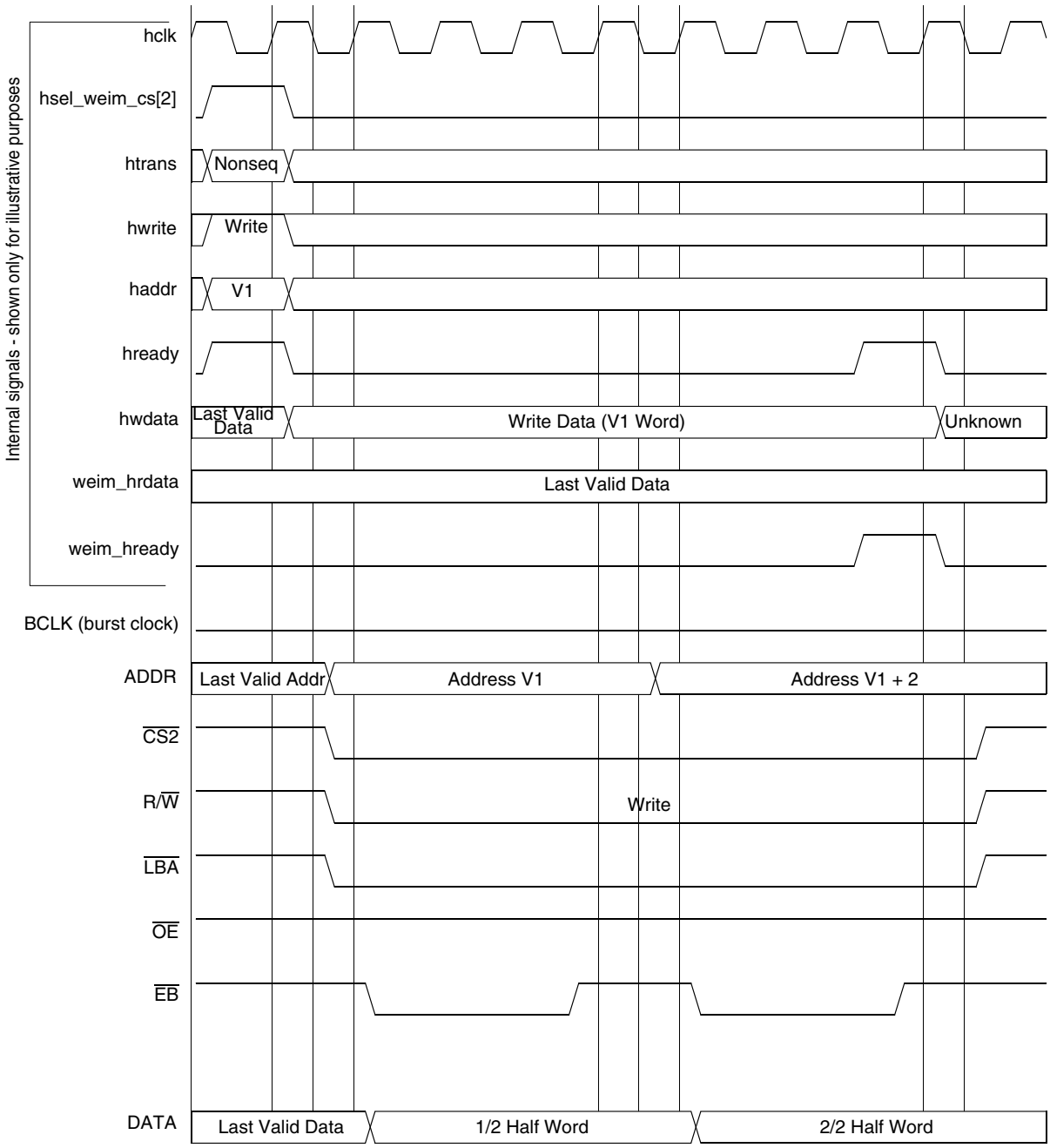


Figure 21. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF

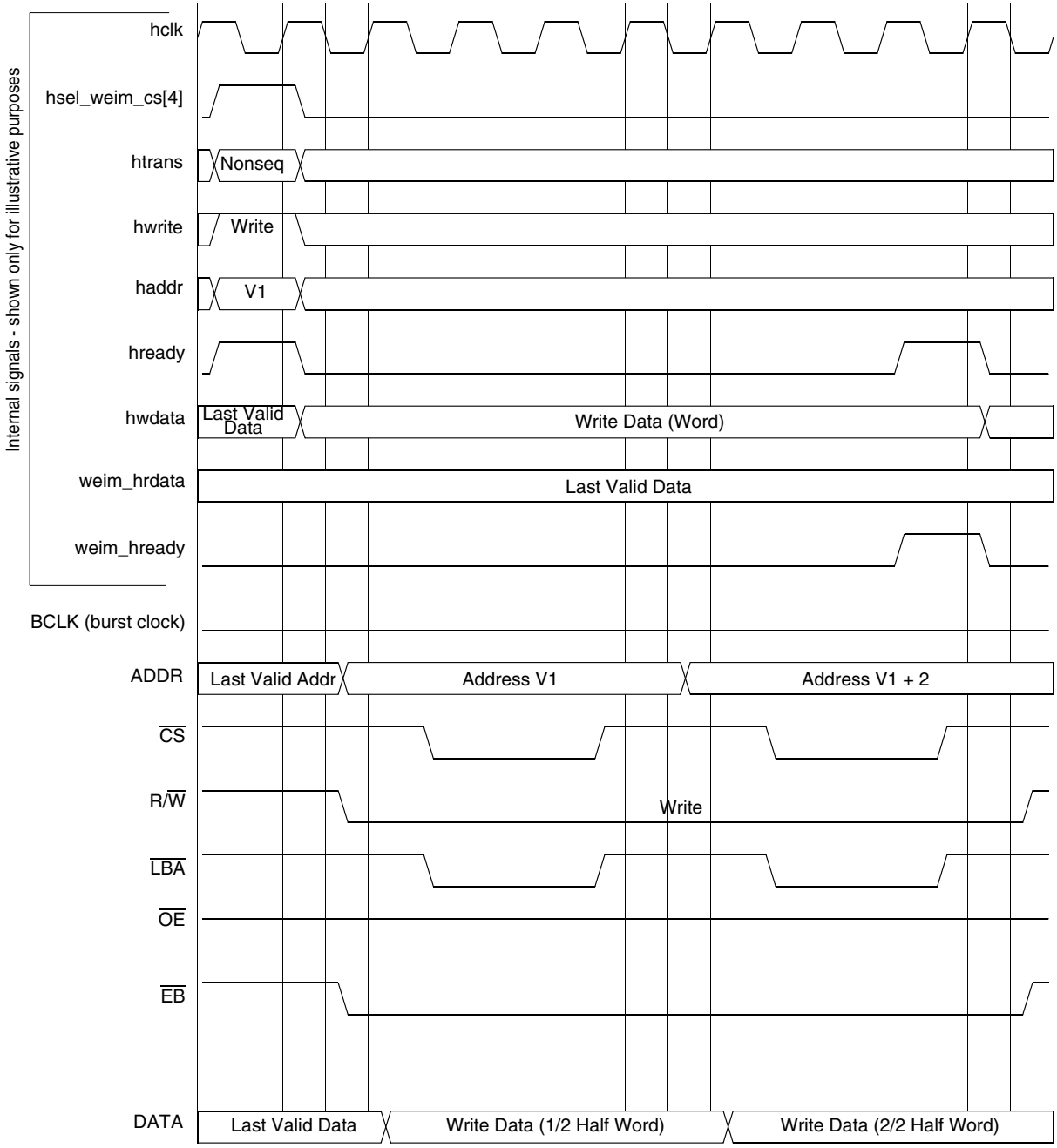
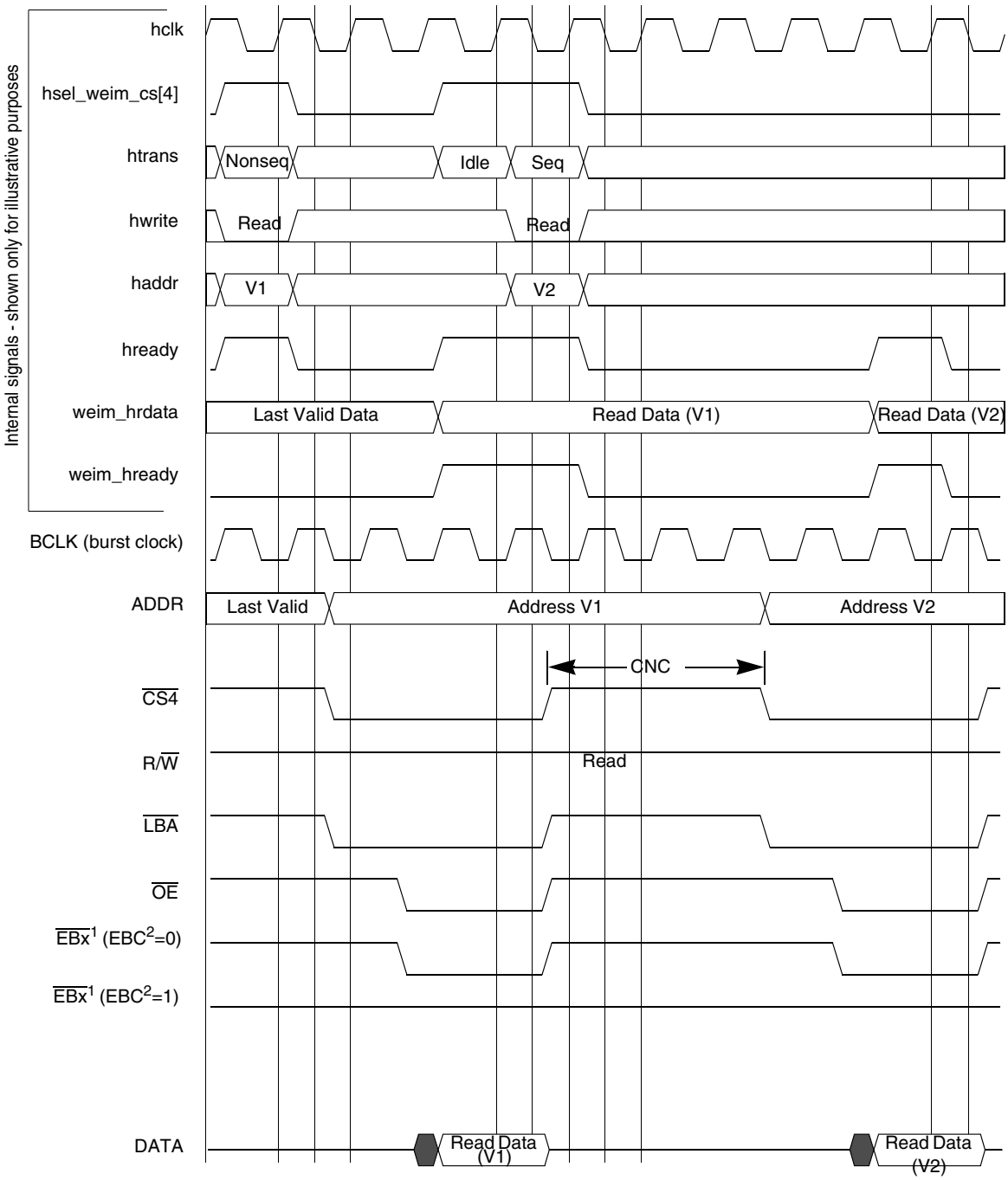
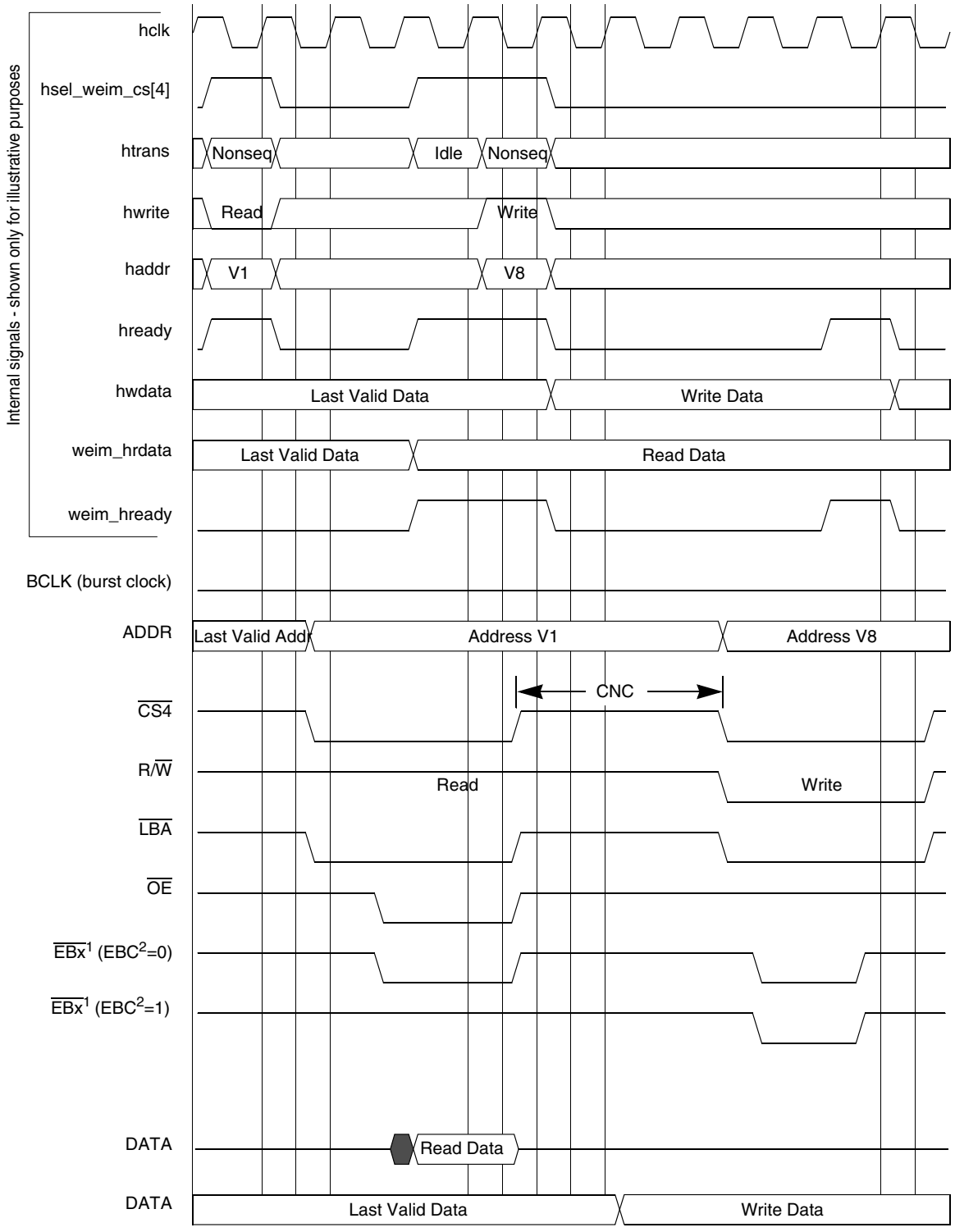


Figure 24. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF



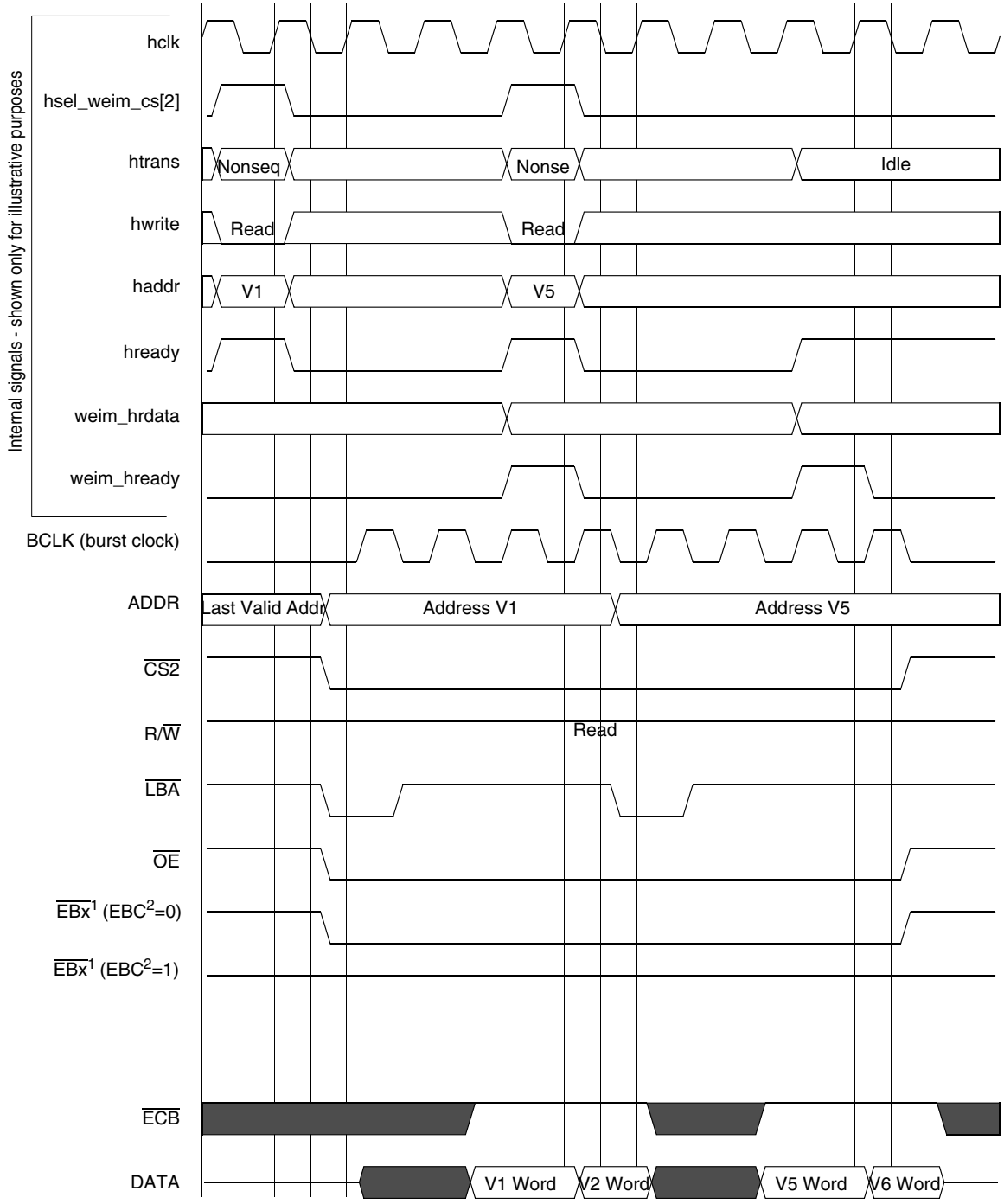
Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 26. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 27. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF



Note 1: x = 0, 1, 2 or 3
Note 2: EBC = Enable Byte Control bit (bit 11) on the Chip Select Control Register

Figure 28. WSC = 3, SYNC = 1, A.HALF/E.HALF

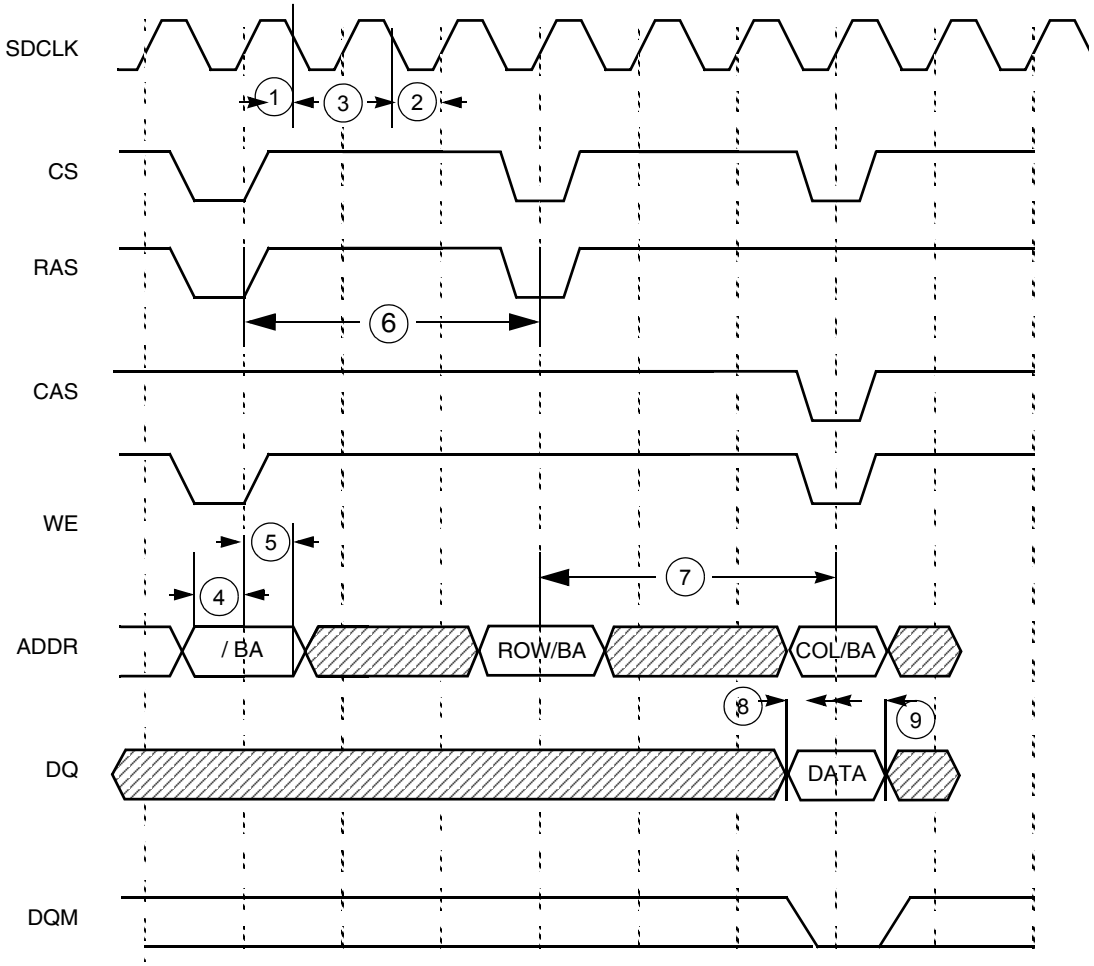


Figure 53. SDRAM Write Cycle Timing Diagram

Table 28. SDRAM Write Timing Parameter Table

Ref No.	Parameter	1.8 ± 0.1 V		3.0 ± 0.3 V		Unit
		Minimum	Maximum	Minimum	Maximum	
1	SDRAM clock high-level width	2.67	–	4	–	ns
2	SDRAM clock low-level width	6	–	4	–	ns
3	SDRAM clock cycle time	11.4	–	10	–	ns
4	Address setup time	3.42	–	3	–	ns
5	Address hold time	2.28	–	2	–	ns
6	Precharge cycle period[1]	t_{RP}[2]	–	t_{RP2}	–	ns
7	Active to read/write command delay	t_{RCD2}	–	t_{RCD2}	–	ns
8	Data setup time	4.0	–	2	–	ns
9	Data hold time	2.28	–	2	–	ns

1 Precharge cycle timing is included in the write timing diagram.

2 t_{RP} and t_{RCD} = SDRAM clock cycle time. These settings can be found in the *MC9328MXL reference manual*.

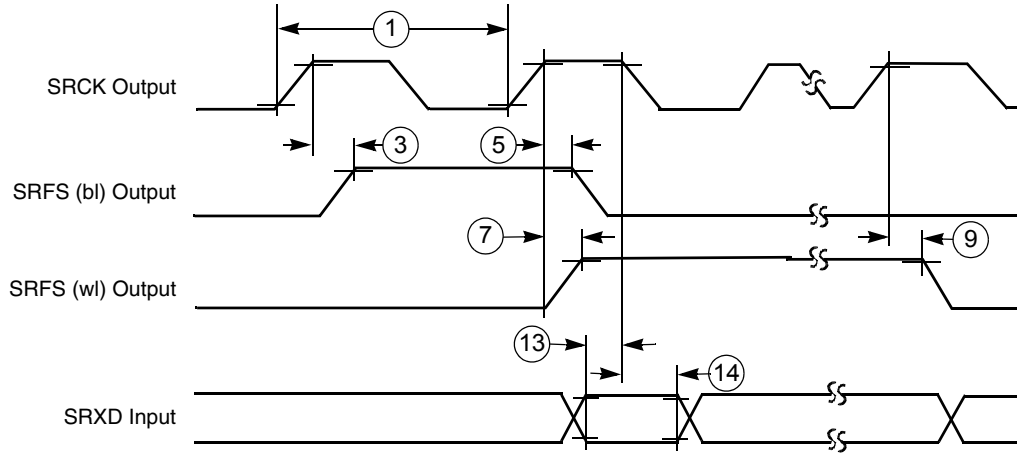
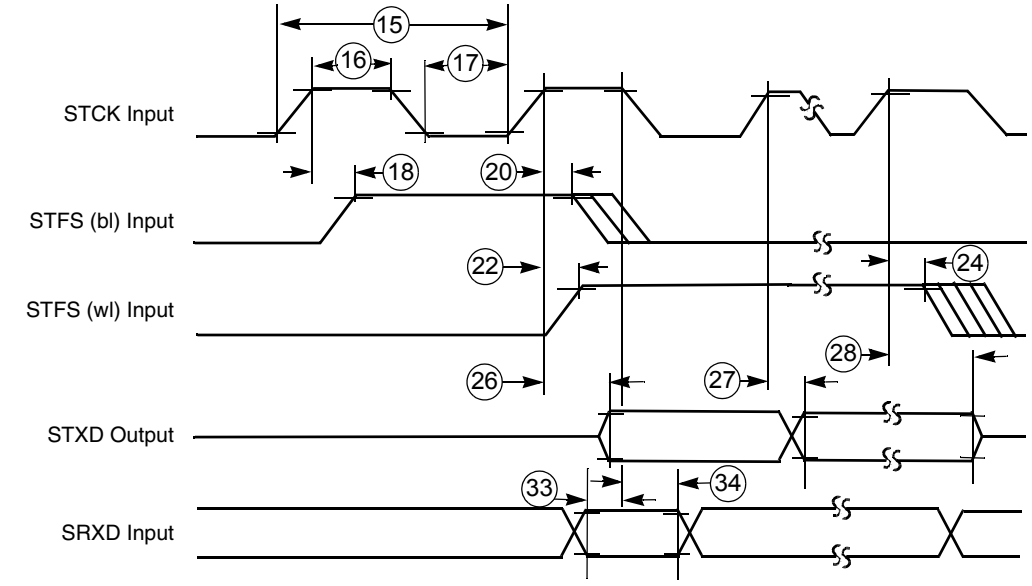


Figure 60. SSI Receiver Internal Clock Timing Diagram



Note: SRXD Input in Synchronous mode only

Figure 61. SSI Transmitter External Clock Timing Diagram

6 Product Documentation

6.1 Revision History

Table 39 provides revision history for this release. This history includes technical content revisions only and not stylistic or grammatical changes.

Table 39. i.MXL Data Sheet Revision History Rev. 8

Location	Revision
Table 2 on page 4 Signal Names and Descriptions	• Added the DMA_REQ signal to table. • Corrected signal name from $\overline{\text{USBD\_OE}}$ to $\overline{\text{USBD\_ROE}}$
Table 3 on page 9 Signal Multiplex Table i.MXL	Added Signal Multiplex table from Reference Manual with the following changes: • Changed I/O Supply Voltage,PB31–20, from NVDD3 to NVDD4 • Added 225 BGA column. • Removed 69K pull-up resistor from EB1, EB2, and added to D9
Table 10 on page 21	Changed first and second parameters descriptions: From: Reference Clock freq range, To: DPLL input clock freq range From: Double clock freq range, To: DPLL output freq range
Table 3 on page 9	Added Signal Multiplex table.

6.2 Reference Documents

The following documents are required for a complete description of the MC9328MXL and are necessary to design properly with the device. Especially for those not familiar with the ARM920T processor or previous i.MX processor products, the following documents are helpful when used in conjunction with this document.

ARM Architecture Reference Manual (ARM Ltd., order number ARM DDI 0100)

ARM9DT1 Data Sheet Manual (ARM Ltd., order number ARM DDI 0029)

ARM Technical Reference Manual (ARM Ltd., order number ARM DDI 0151C)

EMT9 Technical Reference Manual (ARM Ltd., order number DDI O157E)

MC9328MXL Product Brief (order number MC9328MXLP)

MC9328MXL Reference Manual (order number MC9328MXLRM)

The Freescale manuals are available on the Freescale Semiconductors Web site at http://www.freescale.com/imx. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.