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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f314epmc-g-sne2

(Continued)

Part number / Parameter	MB95F314E	MB95F316E	MB95F318E	MB95F314L	MB95F316L	MB95F318L
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					
LCD controller (LCDC)	• COM output: 4 (Max) • SEG output: 40 (Max) • LCD drive power supply (bias) pin: 4 (Max) • 40 SEG × 4 COM: 160 pixels can be displayed					
	• Duty LCD mode • Operate in LCD standby mode • Blinking function • Internal divider resistor for LCD drive					
16-bit reload timer	1 channel					
	• Two clock modes and two counter operating modes can be selected • Square waveform output • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Counter operating mode: reload mode or one-shot mode can be selected					
Event counter	By configuring the 16-bit reload timer and the 8/16-bit composite timer ch. 1, event counter function can be implemented. When the event counter function is used, the 16-bit reload timer and the 8/16-bit composite timer ch. 1 are unavailable.					
8/16-bit PPG	2 channels					
	• Each channel of the PPG can be used as “8-bit PPG × 2 channels” or “16-bit PPG × 1 channel” • Counter operating clock: Eight selectable clock sources					
Watch counter	• Count clock: Four selectable clock sources (125 ms, 250 ms, 500 ms or 1 s) • Counter value can be set from 0 to 63. (Capable of counting for 1 minute when selecting clock source of 1 second and setting counter value to 60)					
External interrupt	8 channels					
	• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing. (asynchronous mode)					
Watch prescaler	Eight different time intervals can be selected. (62.5 ms, 125 ms, 250 ms, 500 ms, 1 s, 2 s, 4 s, 8 s)					
Flash memory	• It supports automatic programming, Embedded Algorithm, program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of program/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-80P-M37					

• MB95370L Series

Part number / Parameter	MB95F374E	MB95F376E	MB95F378E	MB95F374L	MB95F376L	MB95F378L
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	Yes			No		
Reset input	Dedicated					
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max): 55 • CMOS I/O: 52 • N-ch open drain: 3					
Time-base timer	Interval time: 0.256 ms - 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace three bytes of data.					
I^2C	1 channel					
	• Master/Slave sending and receiving • Bus error function and arbitration function • Detecting transmitting direction function • Start condition repeated generation and detection functions • Built-in wake-up function					
UART/SIO	2 channels					
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.					
8/10-bit A/D converter	4 channels					
	8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels					
	• Each timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has built-in timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • It can output square wave.					

(Continued)

■ PIN DESCRIPTION (MB95370L Series)

Pin no.	Pin name	I/O circuit type*	Function
1	AV_{CC}	—	A/D converter power supply pin
2	P16	H	General-purpose I/O port
	PPG10		8/16-bit PPG ch. 1 output pin
3	P15	H	General-purpose I/O port
	PPG11		8/16-bit PPG ch. 1 output pin
4	P14	H	General-purpose I/O port
	UCK0		UART/SIO ch. 0 clock I/O pin
	EC0		8/16-bit composite timer ch. 0 clock input pin The pin can also be used as the event counter input pin when the event counter function is used.
	TI0		16-bit reload timer ch. 0 input pin
5	P13	H	General-purpose I/O port
	ADTG		A/D trigger input (ADTG) pin
	TO01		8/16-bit composite timer ch. 0 output pin
6	P12	C	General-purpose I/O port
	DBG		DBG input pin
7	P11	H	General-purpose I/O port
	UO0		UART/SIO ch. 0 data output pin
8	P10	G	General-purpose I/O port
	UI0		UART/SIO ch. 0 data input pin
9	P24	I	General-purpose I/O port
	SDA0		I^2C data I/O pin
10	P23	I	General-purpose I/O port
	SCL0		I^2C clock I/O pin
11	P22	H	General-purpose I/O port
	TO00		8/16-bit composite timer ch. 0 output pin
12	P21	H	General-purpose I/O port
	PPG01		8/16-bit PPG ch. 0 output pin
13	P20	H	General-purpose I/O port
	PPG00		8/16-bit PPG ch. 0 output pin
14	X0	A	Main clock oscillation pin
15	X1	A	Main clock oscillation pin
16	V_{SS}	—	Power supply pin (GND)
17	V_{CC}	—	Power supply pin
18	P90	R	General-purpose I/O port
	V3		LCDC drive power supply pin

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Pin no.	Pin name	I/O circuit type*	Function
56	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG28		LCDC SEG output pin
	UCK1		UART/SIO ch. 1 clock I/O pin
57	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG29		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
58	P05	Q	General-purpose I/O port
	INT05		External interrupt input pin
	SEG30		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
59	P04	Q	General-purpose I/O port
	INT04		External interrupt input pin
	SEG31		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
60	P03	J	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D analog input pin
61	P02	J	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D analog input pin
62	P01	J	General-purpose I/O port
	INT01		External interrupt input pin
	AN01		A/D analog input pin
63	P00	J	General-purpose I/O port
	INT00		External interrupt input pin
	AN00		A/D analog input pin
64	AV_{SS}	—	A/D converter power supply pin (GND)

*: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

Address	Register abbreviation	Register name	R/W	Initial value
0026H	PDRE	Port E data register	R/W	00000000B
0027H	DDRE	Port E direction register	R/W	00000000B
0028H, 0029H	—	(Disabled)	—	—
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH	PUL1	Port 1 pull-up register	R/W	00000000B
002EH	PUL2	Port 2 pull-up register	R/W	00000000B
002FH, 0030H	—	(Disabled)	—	—
0031H	PUL5	Port 5 pull-up register	R/W	00000000B
0032H, 0033H	—	(Disabled)	—	—
0034H	PUL9	Port 9 pull-up register	R/W	00000000B
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000B
0038H	T11CR1	8/16-bit composite timer 11 status control register 1 ch. 1	R/W	00000000B
0039H	T10CR1	8/16-bit composite timer 10 status control register 1 ch. 1	R/W	00000000B
003AH	PC01	8/16-bit PPG01 control register ch. 0	R/W	00000000B
003BH	PC00	8/16-bit PPG00 control register ch. 0	R/W	00000000B
003CH	PC11	8/16-bit PPG11 control register ch. 1	R/W	00000000B
003DH	PC10	8/16-bit PPG10 control register ch. 1	R/W	00000000B
003EH	TMCSRH	16-bit reload timer control status register upper ch. 0	R/W	00000000B
003FH	TMCSRL	16-bit reload timer control status register lower ch. 0	R/W	00000000B
0040H to 0047H	—	(Disabled)	—	—
0048H	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000B
0049H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000B
004CH, 004DH	—	(Disabled)	—	—
004EH	LVDR	LVD reset voltage selection ID register	R/W	00000000B
004FH	LVDC	LVD control register	R/W	X000000XB
0050H to 0055H	—	(Disabled)	—	—

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000B
0F97H	T11CR0	8/16-bit composite timer 11 status control register 0 ch. 1	R/W	00000000B
0F98H	T10CR0	8/16-bit composite timer 10 status control register 0 ch. 1	R/W	00000000B
0F99H	T11DR	8/16-bit composite timer 11 data register ch. 1	R/W	00000000B
0F9AH	T10DR	8/16-bit composite timer 10 data register ch. 1	R/W	00000000B
0F9BH	TMCR1	8/16-bit composite timer 10/11 timer mode control register ch. 1	R/W	00000000B
0F9CH	PPS01	8/16-bit PPG01 cycle setting buffer register ch. 0	R/W	11111111B
0F9DH	PPS00	8/16-bit PPG00 cycle setting buffer register ch. 0	R/W	11111111B
0F9EH	PDS01	8/16-bit PPG01 duty setting buffer register ch. 0	R/W	11111111B
0F9FH	PDS00	8/16-bit PPG00 duty setting buffer register ch. 0	R/W	11111111B
0FA0H	PPS11	8/16-bit PPG11 cycle setting buffer register ch. 1	R/W	11111111B
0FA1H	PPS10	8/16-bit PPG10 cycle setting buffer register ch. 1	R/W	11111111B
0FA2H	PDS11	8/16-bit PPG11 duty setting buffer register ch. 1	R/W	11111111B
0FA3H	PDS10	8/16-bit PPG10 duty setting buffer register ch. 1	R/W	11111111B
0FA4H	PPGS	8/16-bit PPG start register	R/W	00000000B
0FA5H	REVC	8/16-bit PPG output inversion register	R/W	00000000B
0FA6H	TMRH0	16-bit reload timer timer register upper	R/W	00000000B
	TMRLRH0	16-bit reload timer reload register upper	R/W	00000000B
0FA7H	TMRL0	16-bit reload timer timer register lower	R/W	00000000B
	TMRLRL0	16-bit reload timer reload register lower	R/W	00000000B
0FA8H to 0FBDH	—	(Disabled)	—	—
0FBEH	PSSR0	UART/SIO dedicated baud rate generator prescaler selecting register ch. 0	R/W	00000000B
0FBFH	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	00000000B
0FC0H	PSSR1	UART/SIO dedicated baud rate generator prescaler selecting register ch. 1	R/W	00000000B
0FC1H	BRSR1	UART/SIO dedicated baud rate generator baud rate setting register ch. 1	R/W	00000000B
0FC2H	—	(Disabled)	—	—
0FC3H	AIDRL	A/D input disable register (lower)	R/W	00000000B
0FC4H	LCDCC	LCDC control register	R/W	00010000B

(Continued)

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Address	Register abbreviation	Register name	R/W	Initial value
0FC5H	LCDCE1	LCDC enable register 1	R/W	00110000B
0FC6H	LCDCE2	LCDC enable register 2	R/W	00000000B
0FC7H	LCDCE3	LCDC enable register 3	R/W	00000000B
0FC8H	LCDCE4	LCDC enable register 4	R/W	00000000B
0FC9H	LCDCE5	LCDC enable register 5	R/W	00000000B
0FCAH	—	(Disabled)	—	—
0FCBH	LCDCB1	LCDC blinking setting register 1	R/W	00000000B
0FCCH	LCDCB2	LCDC blinking setting register 2	R/W	00000000B
0FCDH to 0FDCH	LCDRAM	LCDC display RAM	R/W	00000000B
0FDDH to 0FE1H	—	(Disabled)	—	—
0FE2H	EVCR	Event counter control register	R/W	00000000B
0FE3H	WCDR	Watch counter data register	R/W	00111111B
0FE4H	CRTH	Main CR clock trimming register (upper)	R/W	0XXXXXXXB
0FE5H	CRTL	Main CR clock trimming register (lower)	R/W	00XXXXXXB
0FE6H to 0FE8H	—	(Disabled)	—	—
0FE9H	CMCR	Clock monitoring control register	R/W	XX000000B
0FEAH	CMDR	Clock monitoring data register	R	00000000B
0FEBH	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXXB
0FECH	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXXB
0FEDH	—	(Disabled)	—	—
0FEEH	ILSR	Input level select register	R/W	00000000B
0FEFH	WICR	Interrupt pin control register	R/W	01000000B
0FF0H to 0FFFH	—	(Disabled)	—	—

• R/W access symbols
  R/W : Readable / Writable
  R : Read only

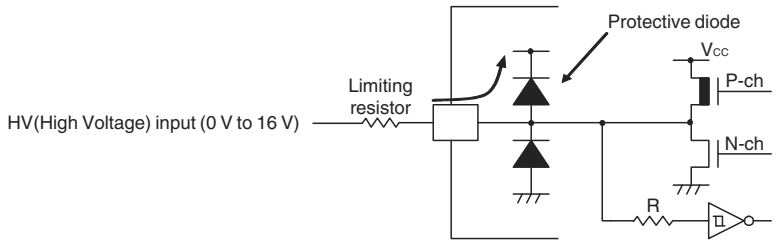
• Initial value symbols
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is indeterminate.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

(Continued)

*5: Applicable to the following pins: P00 to P07, P10, P11, P13 to P16, P20 to P22, P40 to P43, P50 to P53, P60 to P67, P90 to P95, PA0 to PA3, PB0 to PB7, PC0 to PC7, PE0 to PE7, PG0

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistance should be set so that when the HV (High Voltage) signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, and thus affects other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit
  - Input/Output equivalent circuit



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*5	Max		
Power supply current*4	I_{CCLS}	V_{CC} (External clock operation)	F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25°C	—	11.2	16.5	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25°C	—	6.7	9	µA	
	I_{CCMPLL}		F_{CH} = 4 MHz F_{MP} = 10 MHz Main PLL mode (multiplied by 2.5)	—	10.1	19.2	mA	
			F_{CH} = 6.4 MHz F_{MP} = 16 MHz Main PLL mode (multiplied by 2.5)	—	16.2	30.7	mA	
	I_{CCMCR}		F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode	—	7.9	13.2	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25°C	—	77.8	138.5	µA	
	I_{CTS}		F_{CH} = 32 MHz Time-base timer mode T_A = +25°C	—	4.3	7.4	mA	
	I_{CCH}		Substop mode T_A = +25°C	—	1	5	µA	
	I_A	AV_{CC}	Current consumption for A/D conversion at 16 MHz	—	0.8	1.9	mA	
	I_{AH}		Current consumption for stopping A/D conversion at 16 MHz	—	1	5	µA	

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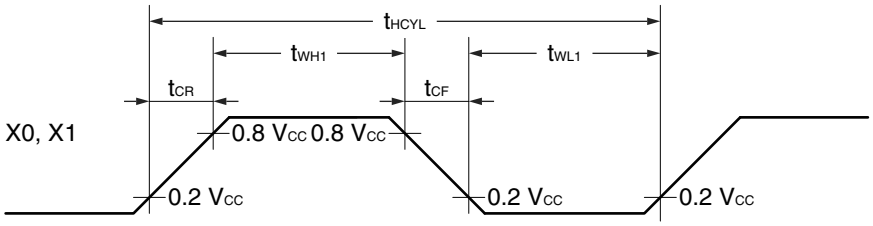
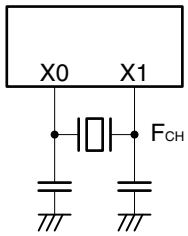
- Input waveform generated when an external clock (main clock) is used

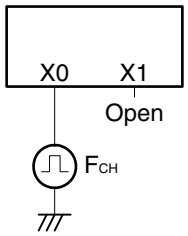


- Figure of main clock input port external connection

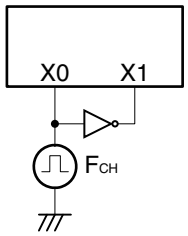
When a crystal oscillator or a ceramic oscillator is used



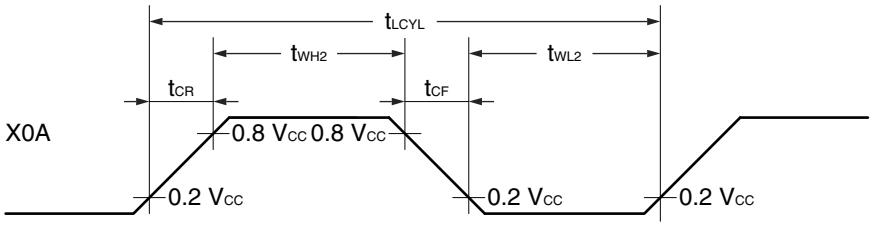
When the external clock is used (X1 is open)



When the external clock is used

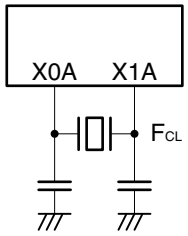


- Input waveform generated when an external clock (subclock) is used

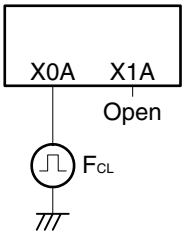


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



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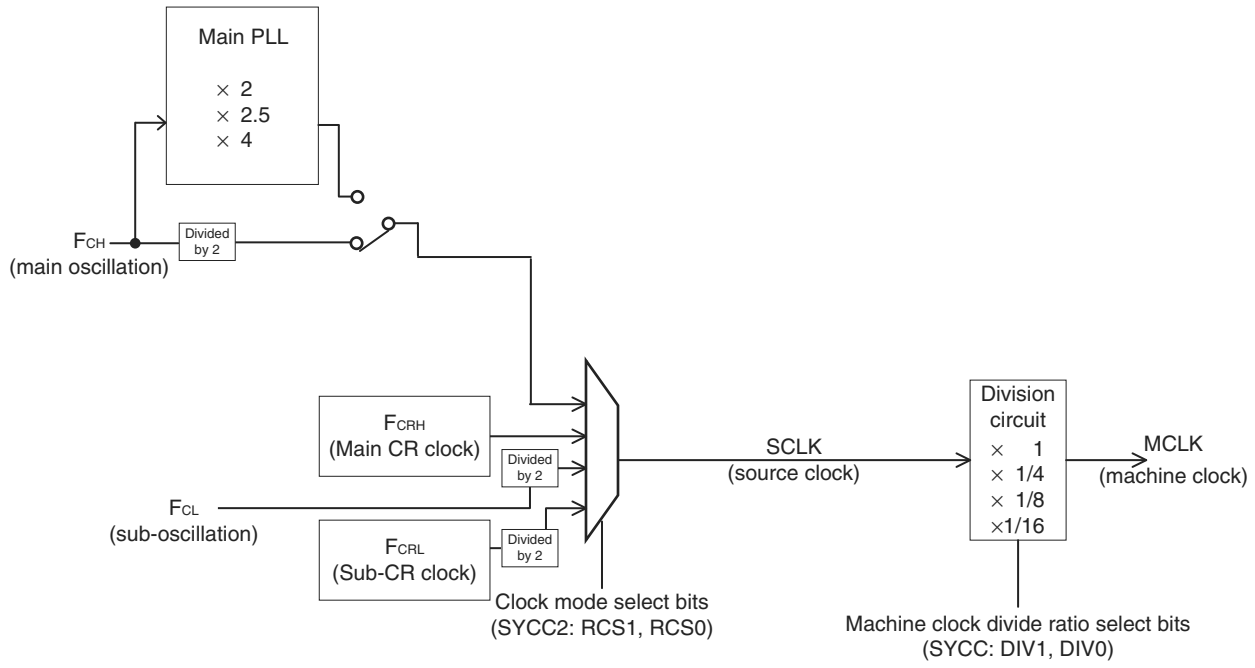
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• Schematic diagram of the clock generation block



(3) External Reset

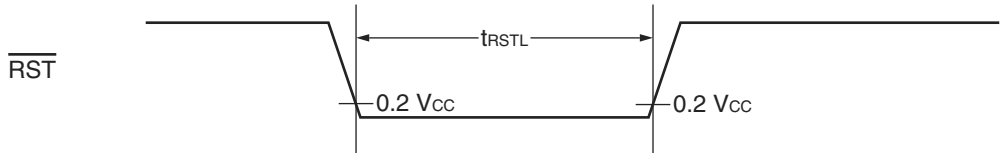
(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*1	—	ns	In normal operation
		Oscillation time of the oscillator*2 + 100	—	µs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	µs	In time-base timer mode

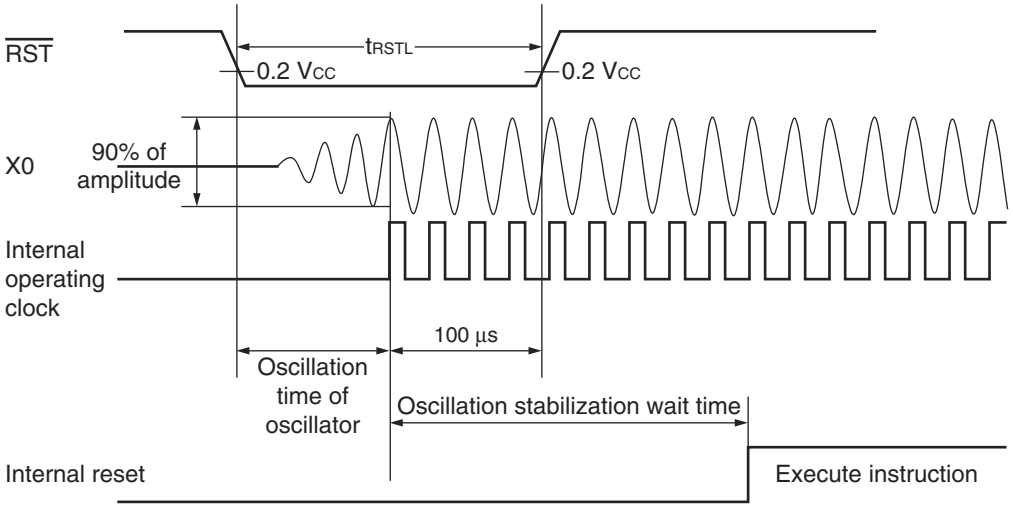
*1: See "(2) Source Clock/Machine Clock" for t_{MCLK}.

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of µs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several µs and several ms.

- In normal operation



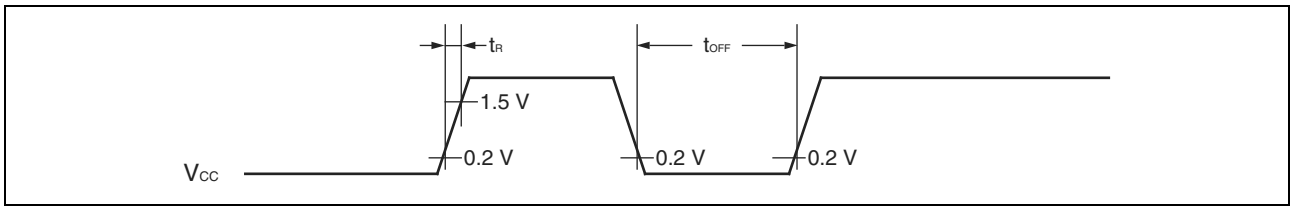
- In stop mode, subclock mode, subsleep mode, watch mode and power-on



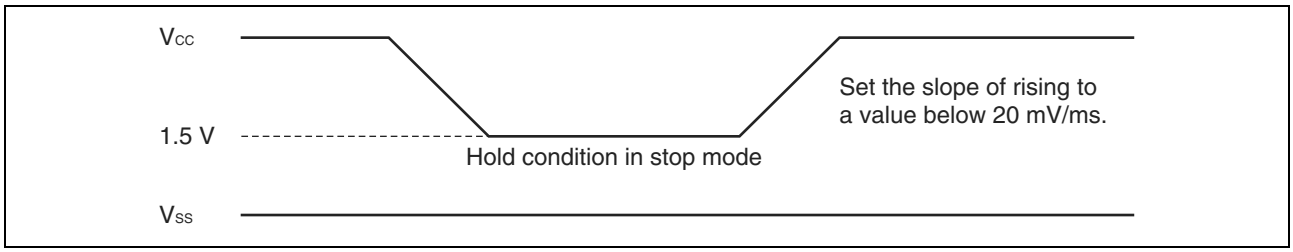
(4) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 20 mV/ms as shown below.



(8) I²C Timing

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL0	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeat) Start condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL0, SDA0		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL0		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL0		4.0	—	0.6	—	µs
(Repeat) Start condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL0, SDA0		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	$t_{HD;DAT}$	SCL0, SDA0		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	$t_{SU;DAT}$	SCL0, SDA0		0.25	—	0.1	—	µs
Stop condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL0, SDA0		4.0	—	0.6	—	µs
Bus free time between stop condition and start condition	t_{BUF}	SCL0, SDA0		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL0 and SDA0 lines, and C the load capacitor of the SCL0 and SDA0 lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT} \geq 250$ ns is fulfilled.

(Continued)

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0	R = 1.7 kΩ, C = 50 pF*1	(2 + nm / 2) t_{MCLK} – 20	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0		(nm / 2)t_{MCLK} – 20	(nm / 2)t_{MCLK} + 20	ns	Master mode
Start condition hold time	$t_{HD;STA}$	SCL0, SDA0		(–1 + nm / 2) t_{MCLK} – 20	(–1 + nm)t_{MCLK} + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	$t_{SU;STO}$	SCL0, SDA0		(1 + nm / 2) t_{MCLK} – 20	(1 + nm / 2)t_{MCLK} + 20	ns	Master mode
Start condition setup time	$t_{SU;STA}$	SCL0, SDA0		(1 + nm / 2)t_{MCLK} – 20	(1 + nm / 2)t_{MCLK} + 20	ns	Master mode
Bus free time between stop condition and start condition	t_{BUF}	SCL0, SDA0		(2 nm + 4)t_{MCLK} – 20	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		3 t_{MCLK} – 20	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		(–2 + nm / 2)t_{MCLK} – 20	(–1 + nm / 2)t_{MCLK} + 20	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.

(Continued)

(V_{CC} = 3.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Conditions	Value*2		Unit	Remarks
				Min	Max		
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL0	R = 1.7 kΩ, C = 50 pF*1	(nm / 2)t_{MCLK} – 20	(1 + nm / 2)t_{MCLK} + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock “L” width	t_{LOW}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL0		4 t_{MCLK} – 20	—	ns	At reception
Start condition detection	$t_{HD;STA}$	SCL0, SDA0		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Stop condition detection	$t_{SU;STO}$	SCL0, SDA0		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Restart condition detection condition	$t_{SU;STA}$	SCL0, SDA0		2 t_{MCLK} – 20	—	ns	Not detected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL0, SDA0		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL0, SDA0		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL0, SDA0		t_{MCLK} – 20	—	ns	At reception
SDA↓→ SCL↑ (at wakeup function)	t_{WAKEUP}	SCL0, SDA0		Oscillation stabilization wait time + 2 t_{MCLK} – 20	—	ns	

(Continued)

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of programming 00_H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of programming 00_H prior to erasure is excluded.
Byte programming time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.7	3.0	3.6	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 3.0 V, 100000 cycles

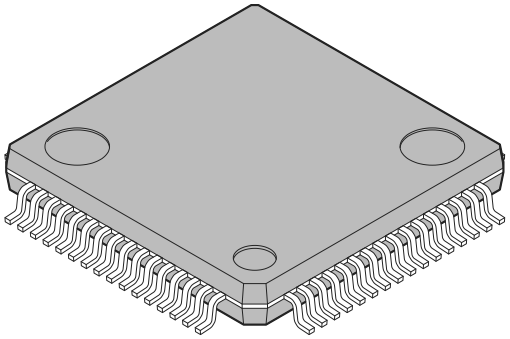
*2: T_A = +85°C, V_{CC} = 2.7 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

■ ORDERING INFORMATION

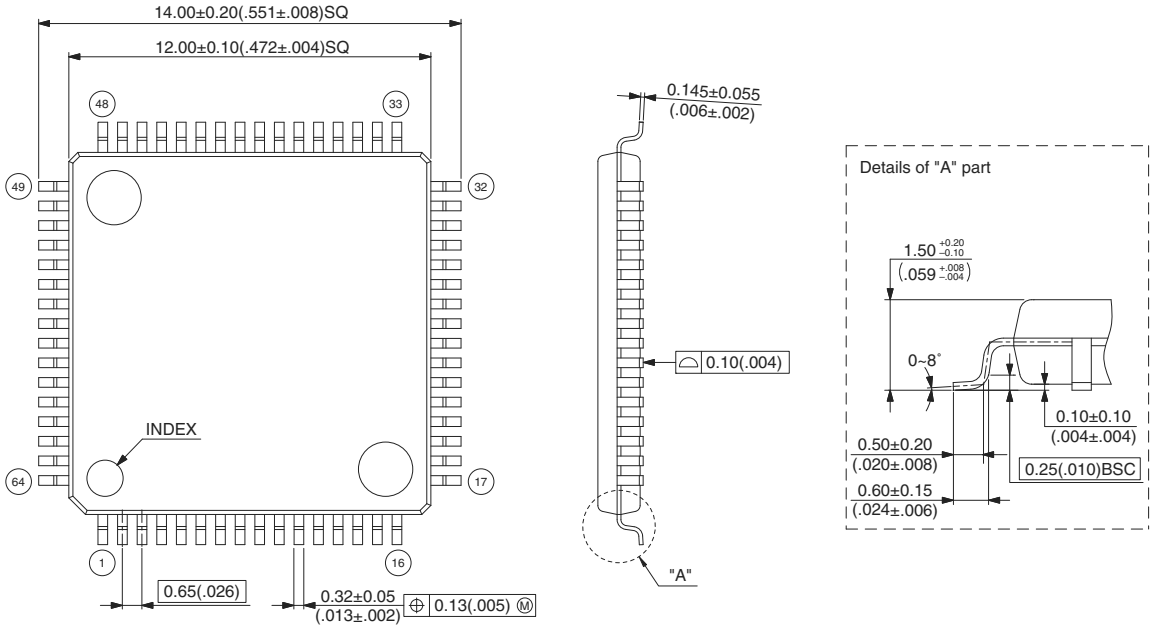
Part Number	Package
MB95F314EPMC-G-SNE2 MB95F314LPMC-G-SNE2 MB95F316EPMC-G-SNE2 MB95F316LPMC-G-SNE2 MB95F318EPMC-G-SNE2 MB95F318LPMC-G-SNE2	80-pin plastic LQFP (FPT-80P-M37)
MB95F374EPMC1-G-SNE2 MB95F374LPMC1-G-SNE2 MB95F376EPMC1-G-SNE2 MB95F376LPMC1-G-SNE2 MB95F378EPMC1-G-SNE2 MB95F378LPMC1-G-SNE2	64-pin plastic LQFP (FPT-64P-M38)
MB95F374EPMC2-G-SNE2 MB95F374LPMC2-G-SNE2 MB95F376EPMC2-G-SNE2 MB95F376LPMC2-G-SNE2 MB95F378EPMC2-G-SNE2 MB95F378LPMC2-G-SNE2	64-pin plastic LQFP (FPT-64P-M39)

(Continued)

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M39)		

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO