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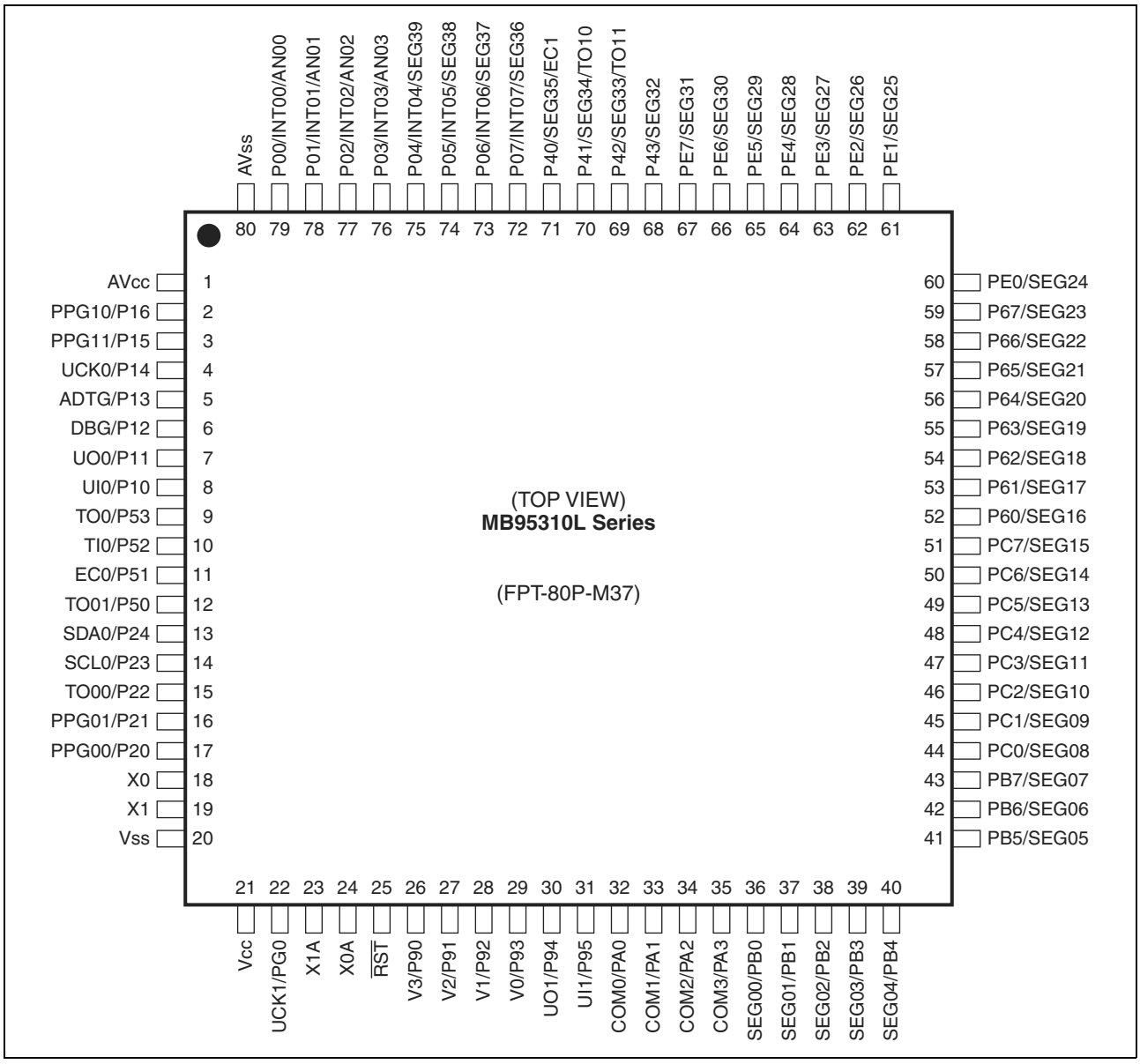
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	71
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1008 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f316epmc-g-sne2

■ PIN ASSIGNMENT



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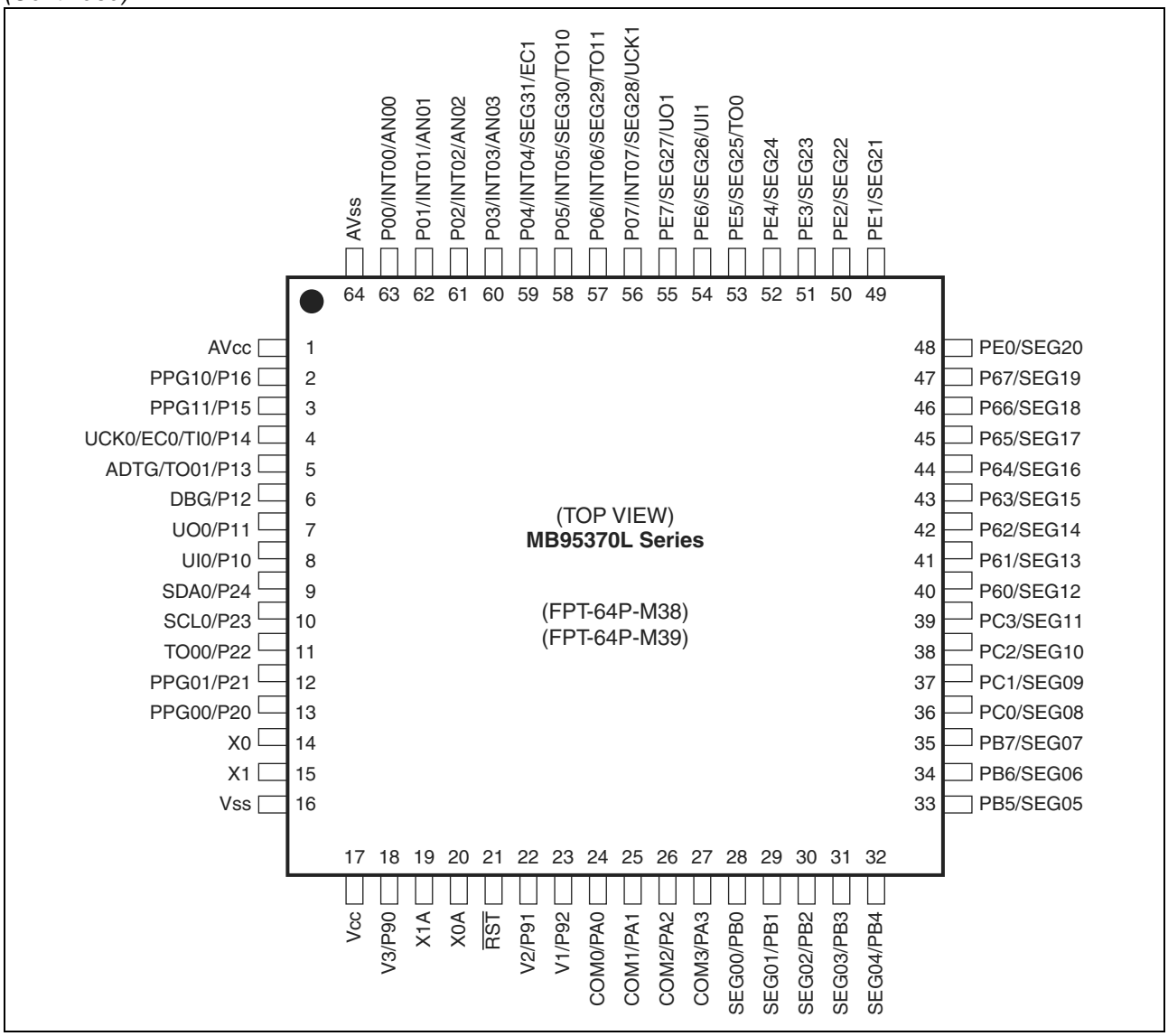

AVss
P00/INT00/AN00
P01/INT01/AN01
P02/INT02/AN02
P03/INT03/AN03
P04/INT04/SEG31/EC1
P05/INT05/SEG30/TO10
P06/INT06/SEG29/TO11
P07/INT07/SEG28/UCK1
PE7/SEG27/UO1
PE6/SEG26/UI1
PE5/SEG25/TO0
PE4/SEG24
PE3/SEG23
PE2/SEG22
PE1/SEG21
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
AVcc 1
PPG10/P16 2
PPG11/P15 3
UCK0/EC0/TI0/P14 4
ADTG/TO01/P13 5
DBG/P12 6
UO0/P11 7
UI0/P10 8
SDA0/P24 9
SCL0/P23 10
TO00/P22 11
PPG01/P21 12
PPG00/P20 13
X0 14
X1 15
Vss 16
48 PE0/SEG20
47 P67/SEG19
46 P66/SEG18
45 P65/SEG17
44 P64/SEG16
43 P63/SEG15
42 P62/SEG14
41 P61/SEG13
40 P60/SEG12
39 PC3/SEG11
38 PC2/SEG10
37 PC1/SEG09
36 PC0/SEG08
35 PB7/SEG07
34 PB6/SEG06
33 PB5/SEG05
(TOP VIEW)
MB95370L Series
(FPT-64P-M38)
(FPT-64P-M39)
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
Vcc
V3/P90
X1A
X0A
RST
V2/P91
V1/P92
COM0/PA0
COM1/PA1
COM2/PA2
COM3/PA3
SEG00/PB0
SEG01/PB1
SEG02/PB2
SEG03/PB3
SEG04/PB4

Pin no.	Pin name	I/O circuit type*	Function
41	PB5	M	General-purpose I/O port
	SEG05		LCDC SEG output pin
42	PB6	M	General-purpose I/O port
	SEG06		LCDC SEG output pin
43	PB7	M	General-purpose I/O port
	SEG07		LCDC SEG output pin
44	PC0	M	General-purpose I/O port
	SEG08		LCDC SEG output pin
45	PC1	M	General-purpose I/O port
	SEG09		LCDC SEG output pin
46	PC2	M	General-purpose I/O port
	SEG10		LCDC SEG output pin
47	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
48	PC4	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
49	PC5	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
50	PC6	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
51	PC7	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
52	P60	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
53	P61	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
54	P62	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
55	P63	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
56	P64	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
57	P65	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
58	P66	M	General-purpose I/O port
	SEG22		LCDC SEG output pin

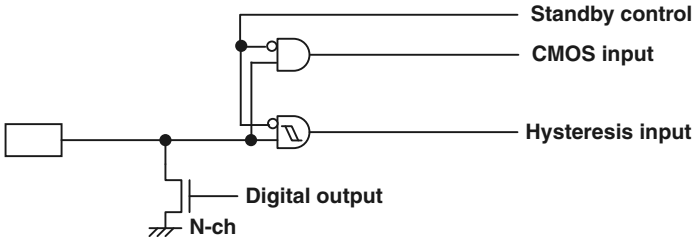
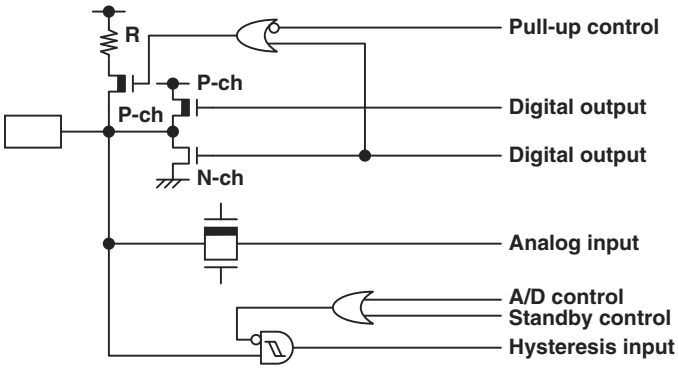
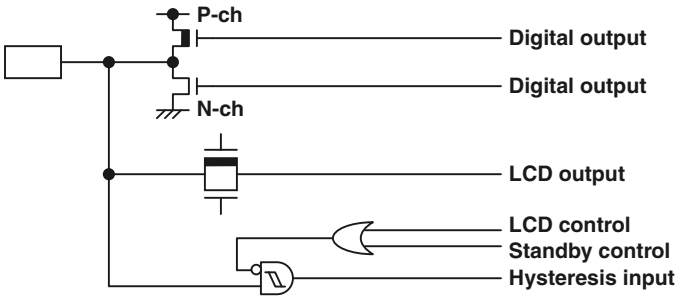
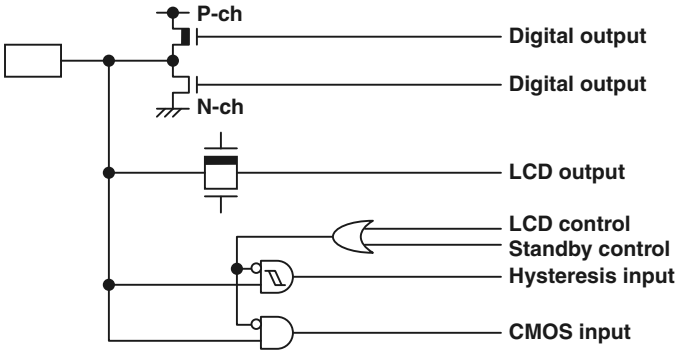
(Continued)

Pin no.	Pin name	I/O circuit type*	Function
59	P67	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
60	PE0	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
61	PE1	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
62	PE2	M	General-purpose I/O port
	SEG26		LCDC SEG output pin
63	PE3	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
64	PE4	M	General-purpose I/O port
	SEG28		LCDC SEG output pin
65	PE5	M	General-purpose I/O port
	SEG29		LCDC SEG output pin
66	PE6	N	General-purpose I/O port
	SEG30		LCDC SEG output pin
67	PE7	M	General-purpose I/O port
	SEG31		LCDC SEG output pin
68	P43	M	General-purpose I/O port
	SEG32		LCDC SEG output pin
69	P42	M	General-purpose I/O port
	SEG33		LCDC SEG output pin
	TO11		8/16-bit composite timer ch. 1 output pin
70	P41	M	General-purpose I/O port
	SEG34		LCDC SEG output pin
	TO10		8/16-bit composite timer ch. 1 output pin
71	P40	M	General-purpose I/O port
	SEG35		LCDC SEG output pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
72	P07	Q	General-purpose I/O port
	INT07		External interrupt input pin
	SEG36		LCDC SEG output pin
73	P06	Q	General-purpose I/O port
	INT06		External interrupt input pin
	SEG37		LCDC SEG output pin

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
39	PC3	M	General-purpose I/O port
	SEG11		LCDC SEG output pin
40	P60	M	General-purpose I/O port
	SEG12		LCDC SEG output pin
41	P61	M	General-purpose I/O port
	SEG13		LCDC SEG output pin
42	P62	M	General-purpose I/O port
	SEG14		LCDC SEG output pin
43	P63	M	General-purpose I/O port
	SEG15		LCDC SEG output pin
44	P64	M	General-purpose I/O port
	SEG16		LCDC SEG output pin
45	P65	M	General-purpose I/O port
	SEG17		LCDC SEG output pin
46	P66	M	General-purpose I/O port
	SEG18		LCDC SEG output pin
47	P67	M	General-purpose I/O port
	SEG19		LCDC SEG output pin
48	PE0	M	General-purpose I/O port
	SEG20		LCDC SEG output pin
49	PE1	M	General-purpose I/O port
	SEG21		LCDC SEG output pin
50	PE2	M	General-purpose I/O port
	SEG22		LCDC SEG output pin
51	PE3	M	General-purpose I/O port
	SEG23		LCDC SEG output pin
52	PE4	M	General-purpose I/O port
	SEG24		LCDC SEG output pin
53	PE5	M	General-purpose I/O port
	SEG25		LCDC SEG output pin
	TO0		16-bit reload timer ch. 0 output pin
54	PE6	N	General-purpose I/O port
	SEG26		LCDC SEG output pin
	UI1		UART/SIO ch. 1 data input pin
55	PE7	M	General-purpose I/O port
	SEG27		LCDC SEG output pin
	UO1		UART/SIO ch. 1 data output pin

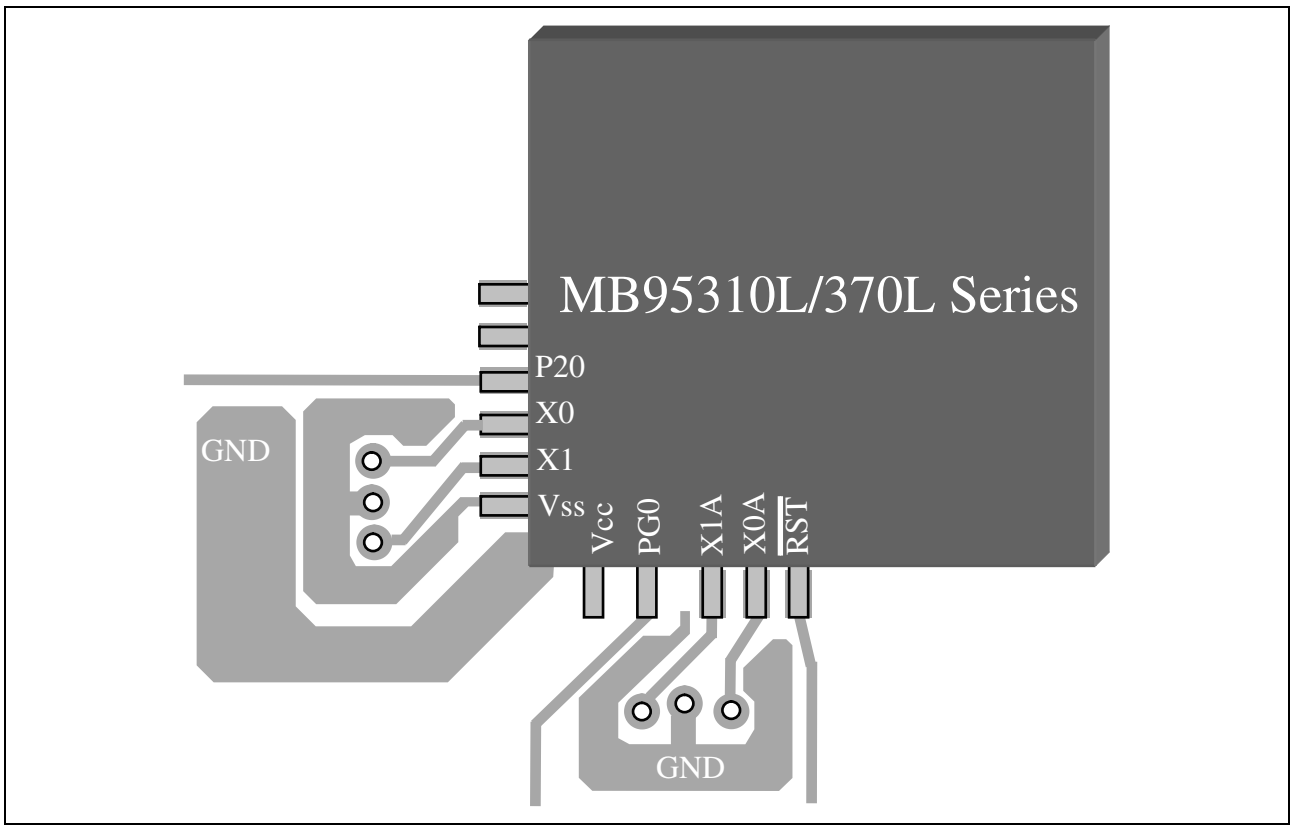
(Continued)

Type	Circuit	Remarks
I		• N-ch open drain output • CMOS input • Hysteresis input
J		• CMOS output • Hysteresis input • Analog input • Pull-up control available
M		• CMOS output • LCD output • Hysteresis input
N		• CMOS output • LCD output • Hysteresis input • CMOS input

(Continued)

■ RECOMMENDED LAYOUT

• GND wire should be placed around X0, X1, X0A and X1A
The recommended layout method illustrated in following diagram aims to avoid noise coupled between the oscillator pins and GPIO, which may cause the main oscillator or the suboscillator to malfunction.



■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 4					
External interrupt ch. 1	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 5					
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
UART/SIO ch. 0	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
Low-voltage detection reset circuit					
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
—	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
—	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
UART/SIO ch. 1					
8/16-bit PPG ch. 1 (upper)	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
16-bit reload timer ch. 0	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
I^{2}C	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
Watch counter					
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}, AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Power supply voltage for LCD	V0 to V3	V_{SS} – 0.3	V_{SS} + 4.0	V	Products with LCD internal division resistance*3
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	P23,P24*4
		V_{SS} – 0.3	V_{SS} + 4.0	V	Other than P23,P24*4
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*4
Maximum clamp current	I_{CLAMP}	–2.0	+2.0	mA	Applicable to specific pins*5
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*5
“L” level maximum output current	I_{OL}	—	15	mA	Applicable to specific pins*5
“L” level average current	I_{OLAV}	—	4	mA	Applicable to specific pins*5 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	-15	mA	Applicable to specific pins*5
“H” level average current	I_{OHAV}	—	-4	mA	Applicable to specific pins*5 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	-100	mA	
“H” level total average output current	ΣI_{OHAV}	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	Pd	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.

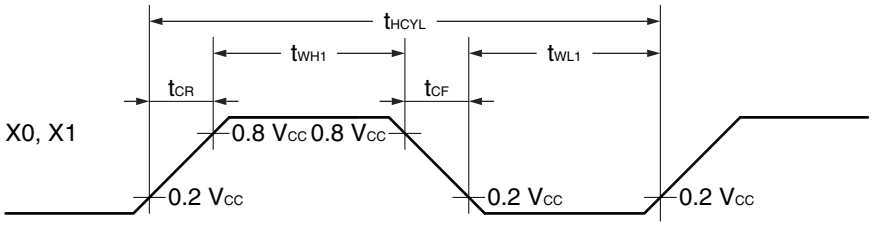
*2: Apply equal potential to V_{CC} and AV_{CC}.

*3: V0 to V3 should not exceed V_{CC} + 0.3 V.

*4: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

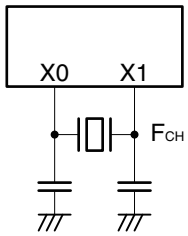
(Continued)

- Input waveform generated when an external clock (main clock) is used

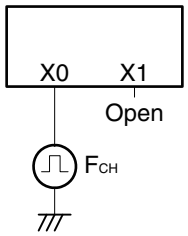


- Figure of main clock input port external connection

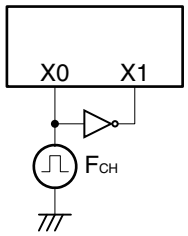
When a crystal oscillator or a ceramic oscillator is used



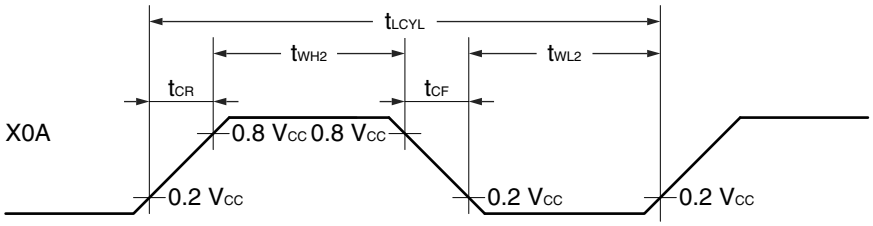
When the external clock is used (X1 is open)



When the external clock is used

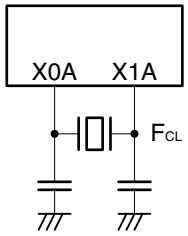


- Input waveform generated when an external clock (subclock) is used

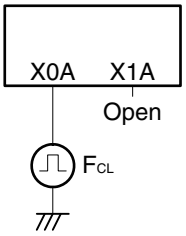


- Figure of subclock input port external connection

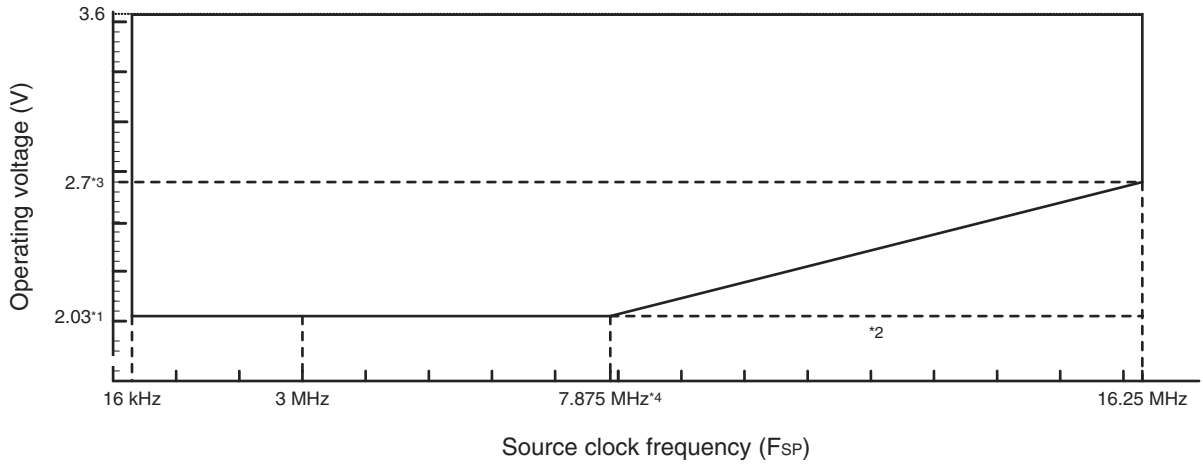
When a crystal oscillator or a ceramic oscillator is used



When the external clock is used



• Operating voltage - Operating frequency (When T_A = +5°C to +35°C)
With the on-chip debug function



*1: This is the default LVD reset clear threshold: 1.93 V ± 0.10 V. It can also be set to 2.40 V ± 0.15 V or 2.95 V ± 0.15 V.

*2: If the LVD reset clear threshold is set to 2.95 V ± 0.15 V, the slope from 10 MHz to 16.25 MHz should be a horizontal line.

*3: The operating voltage becomes 3.1 V if the LVD reset clear threshold is set to 2.95 V ± 0.15 V.

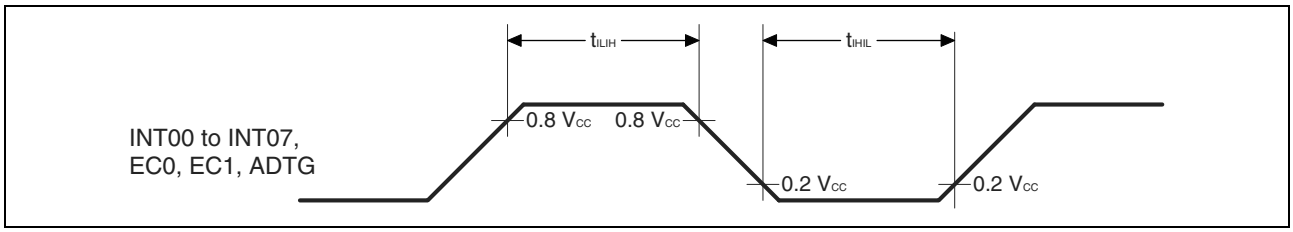
*4: The source clock frequency becomes 14.375 MHz if the LVD reset clear threshold is set to 2.40 V ± 0.15 V.

(5) Peripheral Input Timing

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, EC1, ADTG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



5. A/D Converter

(1) A/D Converter Electrical Characteristics

(V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

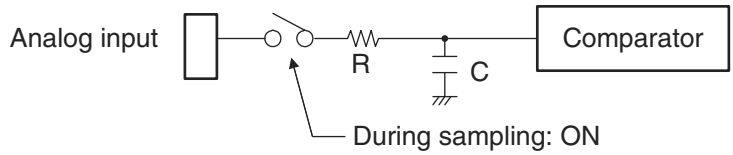
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linear error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		AV_{SS} – 0.5 LSB	AV_{SS} + 1.5 LSB	AV_{SS} + 3.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Full-scale transition voltage	V_{FST}	AV_{CC} – 3.5 LSB	AV_{CC} – 1.5 LSB	AV_{CC} + 0.5 LSB	V	2.7 V ≤ V_{CC} ≤ 3.6 V
		AV_{CC} – 2.5 LSB	AV_{CC} – 0.5 LSB	AV_{CC} + 1.5 LSB	V	1.8 V ≤ V_{CC} < 2.7 V
Compare time	—	0.6	—	140	µs	2.7 V ≤ V_{CC} ≤ 3.6 V
		20	—	140	µs	1.8 V ≤ V_{CC} < 2.7 V
Sampling time	—	0.4	—	∞	µs	2.7 V ≤ V_{CC} ≤ 3.6 V, with external impedance < 1.8 kΩ
		30	—	∞	µs	1.8 V ≤ V_{CC} < 2.7 V, with external impedance < 14.8 kΩ
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	AV_{SS}	—	AV_{CC}	V	

(2) Notes on Using the A/D Converter

• External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

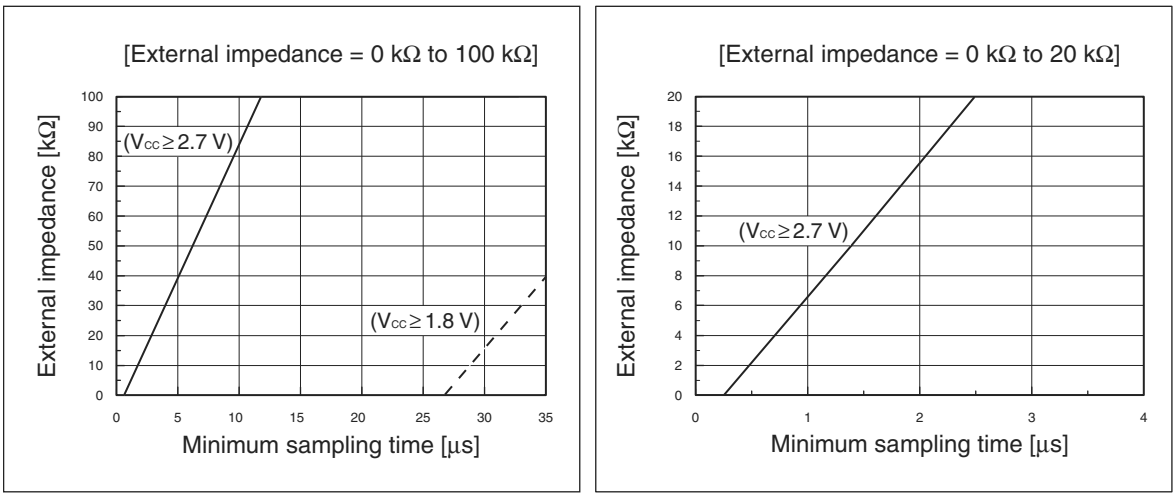
- Analog input equivalent circuit



V_{CC}	R	C
2.7 V ≤ V_{CC} ≤ 3.6V	1.7 kΩ (Max)	14.5 pF (Max)
1.8 V ≤ V_{CC} < 2.7 V	8.4 kΩ (Max)	25.2 pF (Max)

Note: The values are reference values.

- Relationship between external impedance and minimum sampling time

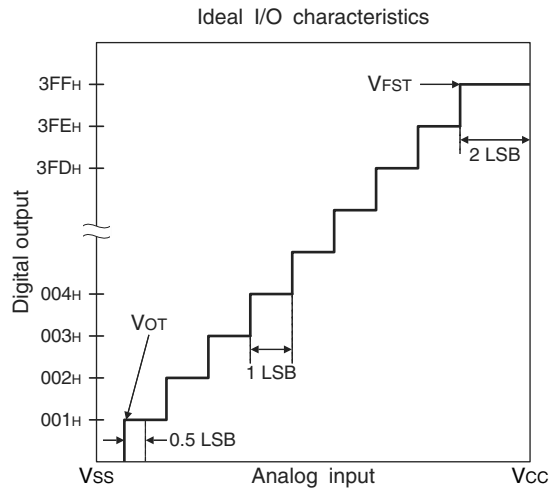


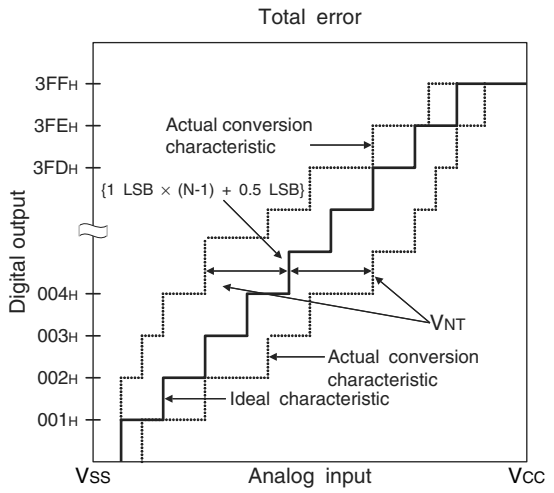
• A/D conversion error

As |V_{CC}–V_{SS}| decreases, the A/D conversion error increases proportionately.

(3) Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ (\text{V})$$

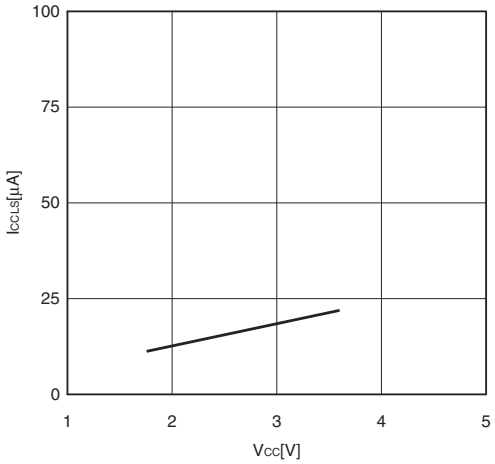
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

N : A/D converter digital output value

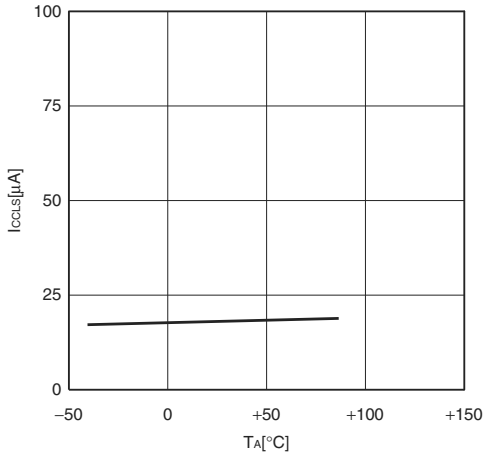
V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

(Continued)

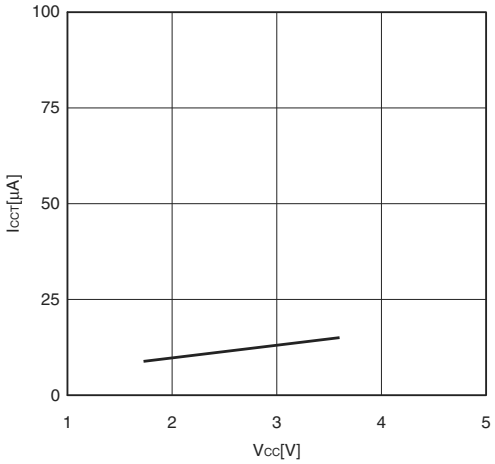
I_{CCLS} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



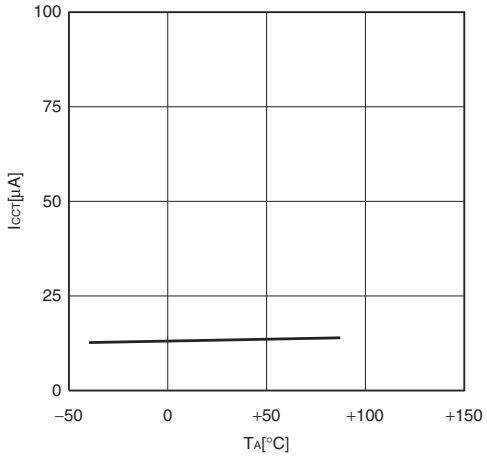
I_{CCLS} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



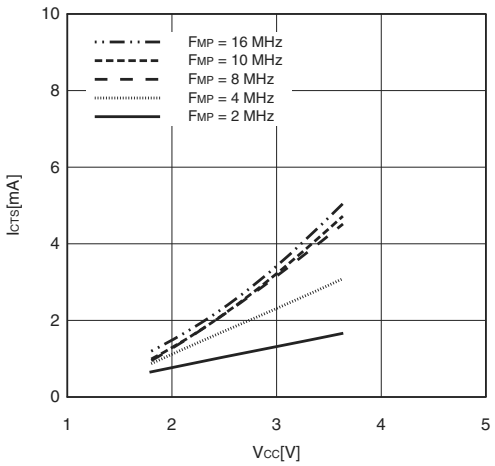
I_{CCT} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



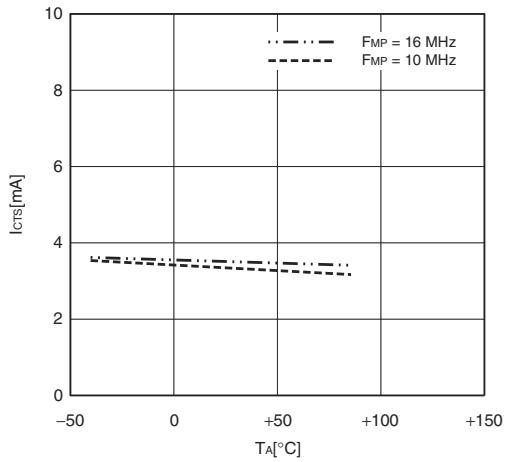
I_{CCT} – T_A
V_{CC} = 3.0 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CTS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

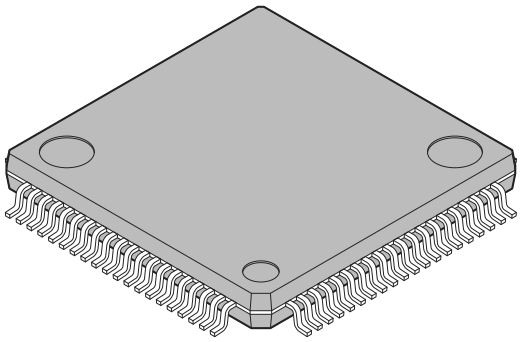


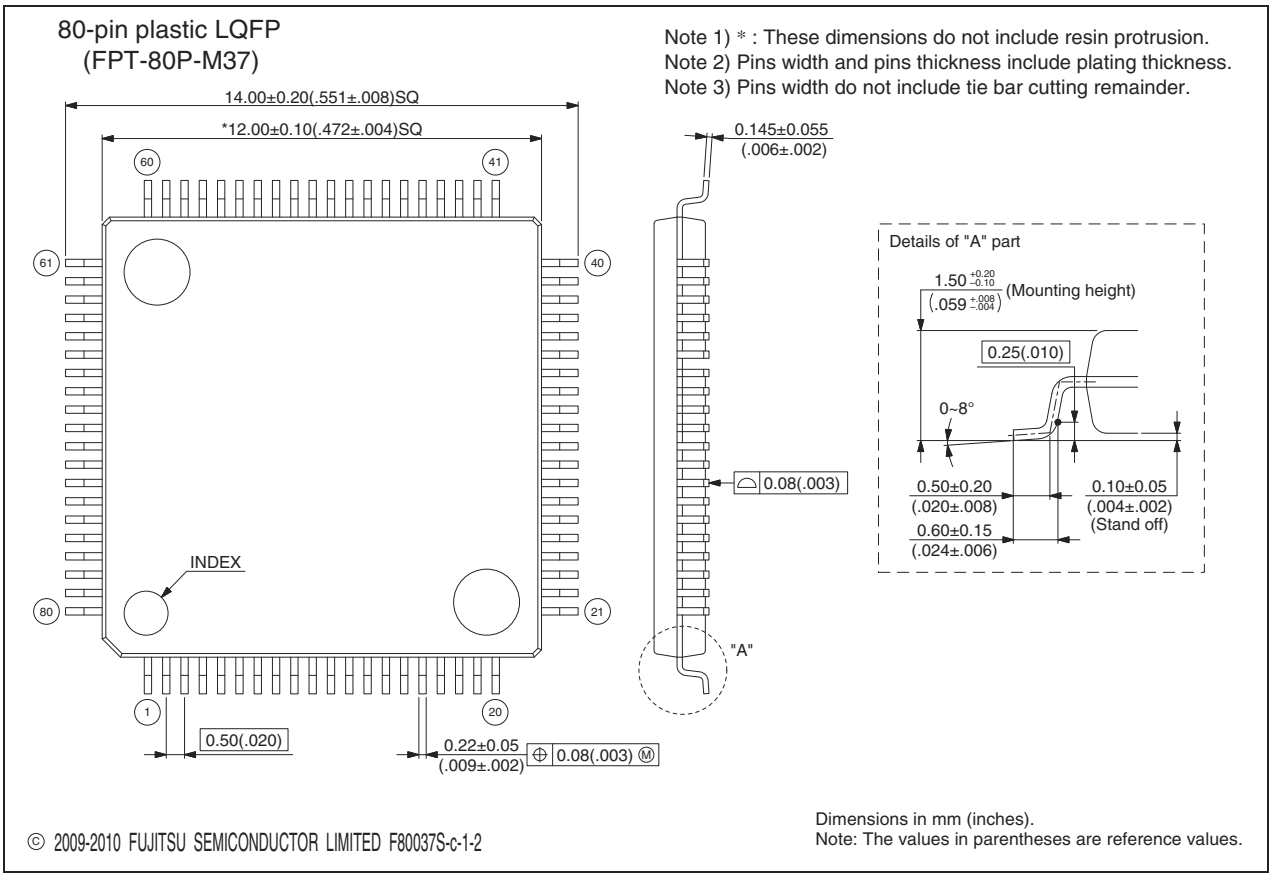
I_{CTS} – T_A
V_{CC} = 3.0 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



(Continued)

■ PACKAGE DIMENSION

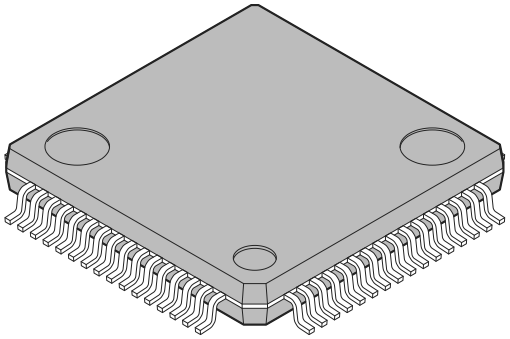
80-pin plastic LQFP		
 (FPT-80P-M37)	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

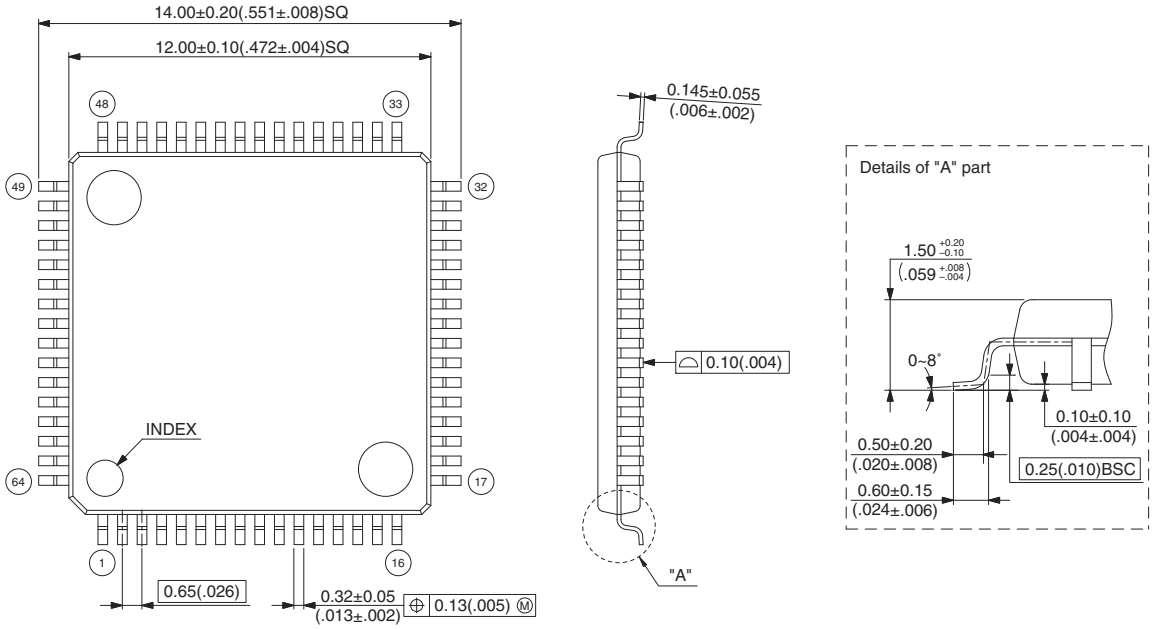
(Continued)

(Continued)

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M39)		

64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Details
1	—	Changed the family name. F²MC-8FX → New 8FX
1	■ FEATURES	Changed the main CR clock oscillation frequency. 1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz → 1/8/10/12.5 MHz ±2%, maximum machine clock frequency: 12.5 MHz
23	■ PIN CONNECTION	Added "• Notes on handling the external clock pins while using the CR clock".
46	■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics	Changed the condition for the power supply current (I_{CCMCR}). F_{CRH} = 10 MHz F_{MP} = 10 MHz Main CR clock mode → F_{CRH} = 12.5 MHz F_{MP} = 12.5 MHz Main CR clock mode Changed the condition for the power supply current (I_{CCSCR}). F_{CL} = 32 kHz F_{MPL} = 16 kHz Sub-CR clock mode (divided by 2) T_A = +25°C → Sub-CR clock mode (divided by 2) T_A = +25°C
47		Changed the condition for the power supply current (I_{CRH}). Current consumption for the main CR oscillator at 10 MHz → Current consumption for the main CR oscillator
48	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Clock Timing	Changed the values of the clock frequency (F_{CRH}).
58	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (7) Low-voltage Detection	Deleted the following parameters: Power hysteresis width 0, Power hysteresis width 1, Power hysteresis width 2, Interrupt hysteresis width 0, Interrupt hysteresis width 1, Interrupt hysteresis width 2, Interrupt hysteresis width 3, Interrupt hysteresis width 4
59		Deleted V_{PHYS}/V_{IHYS} from the diagram.
64	■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (8) I²C Timing	Changed the settings related to the machine clock shown in *2.
70 to 75	■ SAMPLE CHARACTERISTICS	Added "■ SAMPLE CHARACTERISTICS".

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fsp/

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