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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1619-e-ml

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7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: Interrupt Logic



7.6 Register Definitions: Interrupt Control

R/W-0/0	0 R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE ⁽¹⁾	PEIE ⁽²⁾	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF ⁽³⁾
bit 7							bit 0
Legend:							
R = Reada	ble bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'	
u = Bit is u	nchanged	x = Bit is unkr	nown	-n/n = Value	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is :	set	'0' = Bit is clea	ared				
bit 7	GIE: Global II	nterrupt Enable	e bit ⁽¹⁾				
	1 = Enables a 0 = Disables a	all active interru all interrupts	ipts				
bit 6	PEIE: Periphe 1 = Enables a 0 = Disables a	eral Interrupt E all active periph all peripheral ir	nable bit ⁽²⁾ ieral interrupts	S			
bit 5	TMR0IE: Tim 1 = Enables t 0 = Disables	er0 Overflow Ir he Timer0 inter the Timer0 inte	nterrupt Enabl rrupt rrupt	le bit			
bit 4	INTE: INT Ex 1 = Enables t 0 = Disables	ternal Interrupt he INT externa the INT externa	Enable bit I interrupt al interrupt				
bit 3	IOCIE: Interru 1 = Enables t 0 = Disables t	upt-on-Change he interrupt-on the interrupt-or	Enable bit -change -change				
bit 2	TMR0IF: Time 1 = TMR0 reg 0 = TMR0 reg	er0 Overflow Ir gister has overf gister did not ov	iterrupt Flag b lowed /erflow	bit			
bit 1	INTF: INT Ex 1 = The INT e 0 = The INT e	ternal Interrupt external interrup external interrup	Flag bit ot occurred ot did not occi	ur			
bit 0	IOCIF: Interru 1 = When at I 0 = None of t	upt-on-Change east one of the he interrupt-on-	Interrupt Flag interrupt-on- change pins	y bit ⁽³⁾ change pins ch have changed	anged state state		
Note 1:	Interrupt flag bits enable bit or the C appropriate interr	are set when a Global Interrupt upt flag bits are	an interrupt co Enable bit, G e clear prior to	ondition occurs IE of the INTC enabling an ir	, regardless of t ON register. Use iterrupt.	he state of its o er software sho	corresponding uld ensure the
2:	Bit PEIE of the IN	TCON register	must be set t	to enable any p	eripheral interru	ıpt.	
3:	The IOCIF Flag b have been cleare	it is read-only a d by software.	and cleared w	hen all the inte	rrupt-on-change	e flags in the IC	CxF registers

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

TABLE 9-2: WDT CLEARING CONDITIONS

Conditions	WDT	
WDTE<1:0> = 00		
WDTE<1:0> = 01 and SEN = 0		
WDTE<1:0> = 10 and enter Sleep	Cleared	
CLRWDT Command	Cleared	
Oscillator Fail Detected		
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK		
Change INTOSC divider (IRCF bits)	Unaffected	

FIGURE 9-2: WINDOW PERIOD AND DELAY



10.5 Write Verify

It is considered good programming practice to verify that program memory writes agree with the intended value. Since program memory is stored as a full page then the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

FIGURE 10-8: FLASH PROGRAM MEMORY VERIFY FLOWCHART



	U-1	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q ⁽²⁾	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
	_(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD
bit 7					· · ·			bit 0
Legei	nd:							
R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'								
S = B	it can	only be set	x = Bit is unkno	own	-n/n = Value at F	POR and BOR/V	alue at all other l	Resets
'1' = E	Bit is s	set	'0' = Bit is clea	red	HC = Bit is clear	red by hardware		
bit 7		Unimplement	ed: Read as '1'					
bit 6		CFGS: Config	uration Select bit					
		$\perp = \text{Access C}$ 0 = Access F	ontiguration, Use	er ID and Device	Registers			
bit 5		LWLO: Load \	Write Latches On	lv bit ⁽³⁾				
bit 0		1 = Only the	addressed progra	am memory write	e latch is loaded/u	updated on the n	ext WR comman	d
		0 = The addr	essed program m	emory write latc	h is loaded/update	ed and a write of	all program mem	ory write latches
		will be ini	tiated on the nex	t WR command				
bit 4		FREE: Progra	m Flash Erase E	nable bit	NP command (ba	rdwara alaarad i	upon completion	
		0 = Performs	a write operation	on the next WF	R command		upon completion,	
bit 3		WRERR: Prog	, gram/Erase Error	Flag bit				
		1 = Condition	indicates an imp	proper program	or erase sequend	e attempt or ter	mination (bit is s	et automatically
		on any se	et attempt (write '	1') of the WR bit	i) d. normolly <i>i</i>			
hit 2		WPEN: Progr	m/Eraso Enable	hit	u normaliy			
		1 = Allows pr	ogram/erase cvc	les				
		0 = Inhibits p	rogramming/eras	ing of program F	Flash			
bit 1		WR: Write Co	ntrol bit					
		1 = Initiates a	a program Flash p	program/erase o	peration.			
		The oper	ation is self-timed bit can only be se	and the bit is c t (not cleared) ii	leared by hardwa n software	re once operatio	n is complete.	
		0 = Program	erase operation f	to the Flash is co	omplete and inact	ive		
bit 0		RD: Read Cor	ntrol bit					
		1 = Initiates a	a program Flash r	ead. Read takes	s one cycle. RD is	cleared in hard	ware. The RD bit	can only be set
		(not clear	red) in software.	n Flash read				
Note	1.		read as '1'	in nasin Itau				
Hole	2:	The WRERR bit is a	utomatically set l	by hardware whe	en a program mer	nory write or era	se operation is s	tarted (WR = 1).
	3:	The LWLO bit is ign	ored during a pro	gram memory e	rase operation (F	REE = 1).	P	-/-

REGISTER 10-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

12.3.7 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the peripheral pin select logic. See **Section13.0** "**Peripheral Pin Select (PPS) Module**" for more information. Analog input functions, such as ADC inputs, are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELB register. Digital output functions continue to may continue to control the pin when it is in Analog mode.

REGISTER 12-19: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7 ⁽¹⁾	LATC6 ⁽¹⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0	LATC<7:0>: RC<7:0> Output Latch Value bits ⁽¹⁾
	1 = PORTC pin configured as an input (tri-stated)
	0 = PORTC pin configured as an output

Note 1: LATC<7:6> on PIC16(L)F1619 only.

2: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

REGISTER 12-20: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	—	—	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **ANSC<7:6>**: Analog Select between Analog or Digital Function on Pins RC<7:6>, respectively⁽¹⁾ 1 = Analog input. Pin is assigned as analog input⁽²⁾. Digital input buffer disabled.

- 0 = Digital I/O. Pin is assigned to port or digital special function.
- bit 5-4 Unimplemented: Read as '0'

bit 3-0 **ANSC<3:0>**: Analog Select between Analog or Digital Function on Pins RC<3:0>, respectively 1 = Analog input. Pin is assigned as analog input⁽²⁾. Digital input buffer disabled. 0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: ANSC<7:6> on PIC16(L)F1619 only.

2: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

14.0 INTERRUPT-ON-CHANGE

The PORTA, PORTB⁽¹⁾ and PORTC pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- · Rising and falling edge detection
- Individual pin interrupt flags

Figure 14-1 is a block diagram of the IOC module.

Note 1: PORTB available on PIC16(L)F1619 only.

14.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

14.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

14.3 Interrupt Flags

The IOCAFx, IOCBFx and IOCCFx bits located in the IOCAF, IOCBF and IOCCF registers, respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx, IOCBFx and IOCCFx bits.

14.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx, IOCBFx and IOCCFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 14-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

MOVLW 0xff XORWF IOCAF, W ANDWF IOCAF, F

14.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

23.5.6 EDGE-TRIGGERED ONE-SHOT MODE

The Edge-Triggered One-Shot modes start the timer on an edge from the external signal input, after the ON bit is set, and clear the ON bit when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 01001)
- Falling edge (MODE<4:0> = 01010)
- Rising or Falling edge (MODE<4:0> = 01011)

If the timer is halted by clearing the ON bit then another TMRx_ers edge is required after the ON bit is set to resume counting. Figure 23-9 illustrates operation in the rising edge One-Shot mode.

When Edge-Triggered One-Shot mode is used in conjunction with the CCP then the edge-trigger will activate the PWM drive and the PWM drive will deactivate when the timer matches the CCPRx pulse width value and stay deactivated when the timer halts at the PRx period count match.

FIGURE 23-9: EDGE-TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)

MODE	0b01001
TMRx_clk	
PRx	5
Instruction ⁽¹⁾ -	(BSF) (BCF)
ON	
TMRx_ers	
TMRx	$0 \qquad 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 0 \qquad 1 \\ 2 \qquad 2$
TMRx_out	
MRx_postscaled	
PWM Duty Cycle	3
PWM Output	

23.6 Timer2 Operation During Sleep

When PSYNC = 1, Timer2 cannot be operated while the processor is in Sleep mode. The contents of the TMR2 and T2PR registers will remain unchanged while processor is in Sleep mode.

When PSYNC = 0, Timer2 will operate in Sleep as long as the clock source selected is also still running. Selecting the LFINTOSC, MFINTOSC, or HFINTOSC oscillator as the timer clock source will keep the selected oscillator running during Sleep.

24.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPxCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 24-30).

24.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

24.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPxCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 24-31).

24.6.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 24-30: ACKNOWLEDGE SEQUENCE WAVEFORM







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25.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VoL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 25-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

25.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 25-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXxREG register.

25.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXxSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXxSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCxSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note: The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

25.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXxREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXxREG until the Stop bit of the previous character has been transmitted. The pending character in the TXxREG is then transferred to the TSR in one Tcy immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXxREG.

25.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUDxCON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 25.5.1.2 "Clock Polarity**".

25.1.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXxREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXxREG. The TXIF flag bit is not cleared immediately upon writing TXxREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXxREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXxREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXxREG.

25.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDxCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. The overflow condition will set the RCIF flag. The counter continues to count until the fifth rising edge is detected on the RX pin. The RCIDL bit will remain false ('0') until the fifth rising edge at which time the RCIDL bit will be set. If the RCREG is read after the overflow occurs but before the fifth rising edge then the fifth rising edge will set the RCIF again.

Terminating the auto-baud process early to clear an overflow condition will prevent proper detection of the sync character fifth rising edge. If any falling edges of the sync character have not yet occurred when the ABDEN bit is cleared then those will be falsely detected as Start bits. The following steps are recommended to clear the overflow condition:

- 1. Read RCREG to clear RCIF.
- 2. If RCIDL is zero then wait for RCIF and repeat step 1.
- 3. Clear the ABDOVF bit.

25.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDxCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 25-7), and asynchronously if the device is in Sleep mode (Figure 25-8). The interrupt condition is cleared by reading the RCxREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

25.4.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCxREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

25.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

25.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCxSTA and TXxSTA Control registers must be configured for Synchronous Slave Reception (see Section 25.5.2.4 "Synchronous Slave Reception Set-up:").
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCxREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

25.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- The RCxSTA and TXxSTA Control registers must be configured for synchronous slave transmission (see Section 25.5.2.2 "Synchronous Slave Transmission Set-up:").
- The TXIF interrupt flag must be cleared by writing the output data to the TXxREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXxREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXxREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
			CCPF	R<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimpler	nented bit, read	d as '0'		
u = Bit is unchanged x = Bit is u		x = Bit is unkr	nown	-n/n = Value a	at POR and BC	R/Value at all	other Reset	
'1' = Bit is set		'0' = Bit is cle	ared					
bit 7-0	<u>MODE = Ca</u>	<u>pture Mode</u>						
	CCPRxL<7:	0>: LSB of capt	ured TMR1 va	alue				
	MODE = Co	<u>mpare Mode</u>						
	CCPRxL<7:	0>: LSB compa	red to TMR1 v	/alue				
	MODE = PW	M Mode && FN	<u>1T = o</u>					
	CCPRxL<7:	0>: CCPW<7:0	> — Pulse wic	th Least Signifi	cant eight bits			
	MODE = PWM Mode && FMT = 1							

CCPRxL<7:6>: CCPW<1:0> — Pulse width Least Significant two bits

REGISTER 26-3: CCPRxL: CCPx LOW BYTE REGISTER

CCPRxL<5:0>: Not used

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27.2 Register Definitions: PWM Control

R/W-0/0	U-0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
PWMxEN	—	PWMxOUT	PWMxPOL	—	—	—	—
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimpler	mented bit, read	d as '0'	
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BO				R/Value at all o	other Resets		
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	PWMxEN: PV	VM Module En	able bit				
	1 = PWM mo	dule is enable	b				
	0 = PWM mo	dule is disable	d				
bit 6	Unimplemen	ted: Read as '	0'				
bit 5	bit 5 PWMxOUT: PWM Module Output Value bi			t			
bit 4	PWMxPOL: PWMx Output Polarity Select bit						
	1 = PWM out	tput is active-lo	w				
	0 = PWM out	tput is active-hi	gh				

REGISTER 27-1: PWMxCON: PWM CONTROL REGISTER

bit 3-0 Unimplemented: Read as '0'

REGISTER 27-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWMxDCH<7:0>							
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0

PWMxDCH<7:0>: PWM Duty Cycle Most Significant bits

These bits are the MSbs of the PWM duty cycle. The two LSbs are found in the PWMxDCL register.

REGISTER 27-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxD	CL<7:6>	_	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	PWMxDCL<7:6>: PWM Duty Cycle Least Significant bits
	These bits are the LSbs of the PWM duty cycle. The MSbs are found in the PWMxDCH register.
bit 5-0	Unimplemented: Read as '0'



REGISTER 32-23: PIDxACCU: PID ACCUMULATOR UPPER REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	_		_			ACC<34:32>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-3 Unimplemented: Read as '0'

bit 2-0 ACC<34:32>: Bits <34:32> of ACC. ACC is the accumulator register in which all of the multiplier results for the PID are accumulated before being written to the output.

REGISTER 32-24: PIDxACCHH: PID ACCUMULATOR HIGH HIGH REGISTER

| R/W-0/0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| | | | ACC< | 31:24> | | | |
| bit 7 | | | | | | | bit 0 |
| | | | | | | | |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-0 **ACC<31:24>:** Bits <31:24> of ACC. ACC is the accumulator register in which all of the multiplier results for the PID are accumulated before being written to the output.

REGISTER 32-25: PIDxACCHL: PID ACCUMULATOR HIGH LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACC<23:16>							
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-0 ACC<23:16>: Bits <23:16> of ACC. ACC is the accumulator register in which all of the multiplier results for the PID are accumulated before being written to the output.

35.2 Standard Operating Conditions

The standard operating conditions for any device are defined as: $V \text{DDMIN} \leq V \text{DD} \leq V \text{DDMAX}$ Operating Voltage: Operating Temperature: TA MIN \leq TA \leq TA MAX VDD — Operating Supply Voltage⁽¹⁾ PIC16LF1615/9 PIC16F1615/9 TA — Operating Ambient Temperature Range Industrial Temperature TA MIN.....--40°C **Extended Temperature** Ta MIN.....--40°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

Note: Unless otherwise noted, VIN = 5V, Fosc = 500 kHz, CIN = 0.1 μ F, TA = 25°C.



FIGURE 36-107: ZCD Pin Voltage, Typical Measured Values.



FIGURE 36-108: ZCD Response Time over Voltage Typical Measured Values.



FIGURE 36-109: ZCD Pin Current over ZCD Pin Voltage, Typical Measured Values from -40°C to 125°C.



FIGURE 36-110: ZCD Pin Response Timer over Current, Typical Measured Values from -40°C to 125°C.