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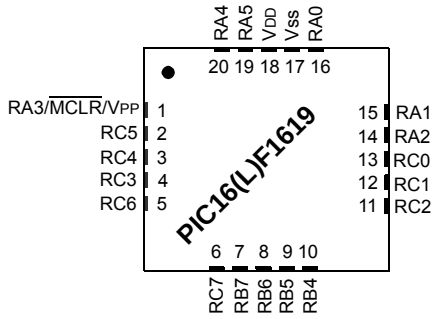
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 14KB (8K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 12x10b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | 20-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f1619-e-p |

**20-pin QFN, UQFN**



## 5.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

| **Note:** | Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear. |
|---|---|

### 5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 00.
- FOSC<2:0> bits in the Configuration Words configured for HS mode.

Two-Speed Start-up mode is entered after:

- Power-On Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

| **Note:** | When FSCM is enabled, Two-Speed Start-up will automatically be enabled. |
|---|---|

### 5.4.2 TWO-SPEED START-UP SEQUENCE

1. Wake-up from Power-on Reset or Sleep.
2. Instructions begin execution by the internal oscillator at the frequency set in the IRCF<3:0> bits of the OSCCON register.
3. OST enabled to count 1024 clock cycles.
4. OST timed out, wait for falling edge of the internal oscillator.
5. OSTS is set.
6. System clock held low until the next falling edge of new clock (HS mode).
7. System clock is switched to external clock source.

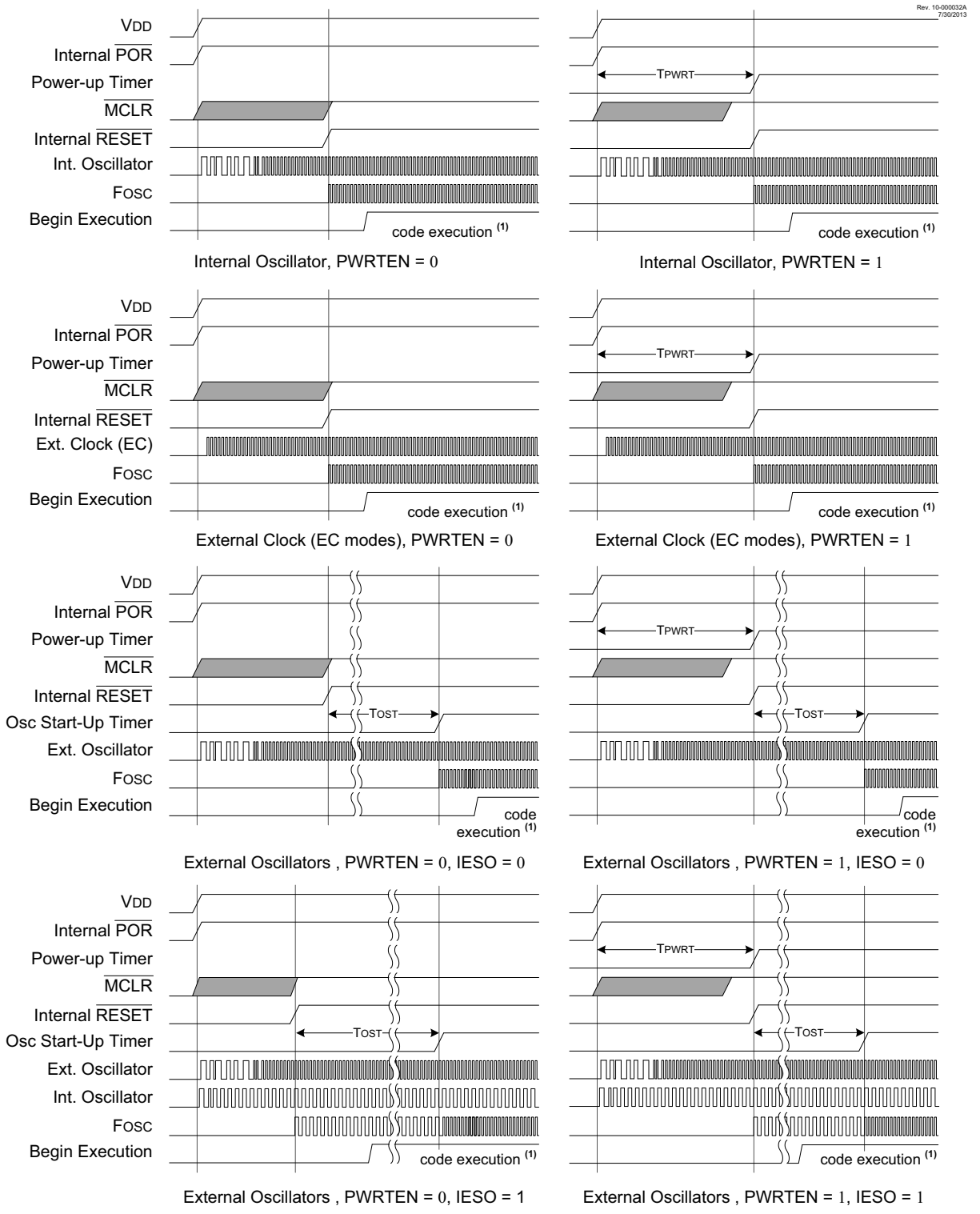
### 5.4.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCSTAT register will confirm if the CPU is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or the internal oscillator. See Table 5-2.

**TABLE 5-2: OSCILLATOR SWITCHING DELAYS**

| Switch From | Switch To | Oscillator Delay |
|---|---|---|
| Any clock source | LFINTOSC | 1 cycle of each clock source |
| | HFINTOSC | 2 μs (approx.) |
| | ECH, ECM, ECL, EXTRC | 2 cycles |
| | HS | 1024 Clock Cycles (OST) |
| | Secondary Oscillator | 1024 Secondary Oscillator Cycles |

**FIGURE 6-3: RESET START-UP SEQUENCE**




**Note 1:** Code execution begins 10 FOSC cycles after the FOSC clock is released.

**REGISTER 12-5: WPUA: WEAK PULL-UP PORTA REGISTER**

| U-0 | U-0 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| — | — | WPUA5 | WPUA4 | WPUA3 | WPUA2 | WPUA1 | WPUA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUA<5:0>**: Weak Pull-up Register bits(3)
1 = Pull-up enabled
0 = Pull-up disabled

**Note 1:** Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
**2:** The weak pull-up device is automatically disabled if the pin is configured as an output.
**3:** For the WPUA3 bit, when MCLRE = 1, weak pull-up is internally enabled, but not reported here.

**REGISTER 12-6: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER**

| U-0 | U-0 | R/W-0/0 | R/W-0/0 | U-0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| — | — | ODA5 | ODA4 | — | ODA2 | ODA1 | ODA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **ODA<5:4>:** PORTA Open-Drain Enable bits
For RA<5:4> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ODA<2:0>:** PORTA Open-Drain Enable bits
For RA<2:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

## 24.6 I²C Master Mode

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPxCON1 register and by setting the SSPEN bit. In Master mode, the SDA and SCK pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDA and SCL lines.

The following events will cause the SSP Interrupt Flag bit, SSPxIF, to be set (SSP interrupt, if enabled):

- Start condition detected
- Stop condition detected
- Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated

**Note 1:** The MSSP module, when configured in I²C Master mode, does not allow queuing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur

**2:** When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

### 24.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/$\overline{W}$) bit. In this case, the R/$\overline{W}$ bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/$\overline{W}$ bit. In this case, the R/$\overline{W}$ bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCL. See **Section 24.7 "Baud Rate Generator"** for more detail.

**REGISTER 24-5: SSP1MSK: SSP MASK REGISTER**

| R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 | R/W-1/1 |
|---|---|---|---|---|---|---|---|
| MSK<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

bit 7-1 **MSK<7:1>:** Mask bits
1 = The received address bit n is compared to SSP1ADD<n> to detect $I^2C$ address match
0 = The received address bit n is not used to detect $I^2C$ address match

bit 0 **MSK<0>:** Mask bit for $I^2C$ Slave mode, 10-bit Address
$I^2C$ Slave mode, 10-bit address (SSPM<3:0> = 0111 or 1111):
1 = The received address bit 0 is compared to SSP1ADD<0> to detect $I^2C$ address match
0 = The received address bit 0 is not used to detect $I^2C$ address match
$I^2C$ Slave mode, 7-bit address, the bit is ignored

**REGISTER 24-6: SSP1ADD: MSSP ADDRESS AND BAUD RATE REGISTER ($I^2C$ MODE)**

| R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 | R/W-0/0 |
|---|---|---|---|---|---|---|---|
| ADD<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| '1' = Bit is set | '0' = Bit is cleared | |

**Master mode:**

bit 7-0 **ADD<7:0>:** Baud Rate Clock Divider bits
SCL pin clock period = ((ADD<7:0> + 1) *4)/FOSC

**10-Bit Slave mode – Most Significant Address Byte:**

bit 7-3 **Not used:** Unused for Most Significant Address Byte. Bit state of this register is a "don't care". Bit pattern sent by master is fixed by $I^2C$ specification and must be equal to '11110'. However, those bits are compared by hardware and are not affected by the value in this register.

bit 2-1 **ADD<2:1>:** Two Most Significant bits of 10-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

**10-Bit Slave mode – Least Significant Address Byte:**

bit 7-0 **ADD<7:0>:** Eight Least Significant bits of 10-bit address

**7-Bit Slave mode:**

bit 7-1 **ADD<7:1>:** 7-bit address

bit 0 **Not used:** Unused in this mode. Bit state is a "don't care".

### 27.1.9 SETUP FOR PWM OPERATION USING PWMx PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRIS bit(s).
2. Clear the PWMxCON register.
3. Load the PR2 register with the PWM period value.
4. Clear the PWMxDCH register and bits <7:6> of the PWMxDCL register.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register. See note below.
   - Configure the CKPS bits of the T2CON register with the Timer2 prescale value.
   - Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin and wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See note below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRIS bit(s) and setting the PWMxOE bit of the PWMxCON register.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

**Note 1:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

**2:** For operation with other peripherals only, disable PWMx pin outputs.

### 28.1.4 STEERING MODES

In Steering modes, the data input can be steered to any or all of the four CWG output pins. In Synchronous Steering mode, changes to steering selection registers take effect on the next rising input.

In Non-Synchronous mode, steering takes effect on the next instruction cycle. Additional details are provided in **Section 28.9 “CWG Steering Mode”**.

## 28.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the CS bit of the CWGxCLKCON register.

## 28.3 Selectable Input Sources

The CWG generates the output waveforms from the input sources in Table 28-1.

**TABLE 28-1: SELECTABLE INPUT SOURCES**

| Source Peripheral | Signal Name |
|---|---|
| CWG pin | PPS selection |
| Comparator C1 | C1_OUT_sync |
| Comparator C2 | C2_OUT_sync |
| CCP1 | CCP1_out |
| CCP2 | CCP2_out |
| CLC1 | LC1_out |
| CLC2 | LC2_out |
| CLC3 | LC3_out |
| CLC4 | LC4_out |
| PWM3 | PWM3_out |
| PWM4 | PWM4_out |

The input sources are selected using the CWGxISM register.

## 28.4 Output Control

### 28.4.1 OUTPUT ENABLES

Each CWG output pin has individual output enable control. Output enables are selected with the Gx1OEx <3:0> bits. When an output enable control is cleared, the module asserts no control over the pin. When an output enable is set, the override value or active PWM waveform is applied to the pin per the port priority selection. The output pin enables are dependent on the module enable bit, EN of the CWGxCON0 register. When EN is cleared, CWG output enables and CWG drive levels have no effect.

### 28.4.2 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the POLx bits of the CWGxCON1. Auto-shutdown and steering options are unaffected by polarity.

### 30.6.4 HIGH AND LOW MEASURE MODE

This mode measures the high and low pulse time of the SMTSIGx relative to the SMT clock. It begins incrementing the SMTxTMR on a rising edge on the SMTSIGx input, then updates the SMTxCPW register with the value and resets the SMTxTMR on a falling edge, starting to increment again. Upon observing another rising edge, it updates the SMTxCPR register with its current value and once again resets the SMTxTMR value and begins incrementing again. See Figure 30-8 and Figure 30-9.

**FIGURE 30-13: GATED WINDOWED MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAMS**

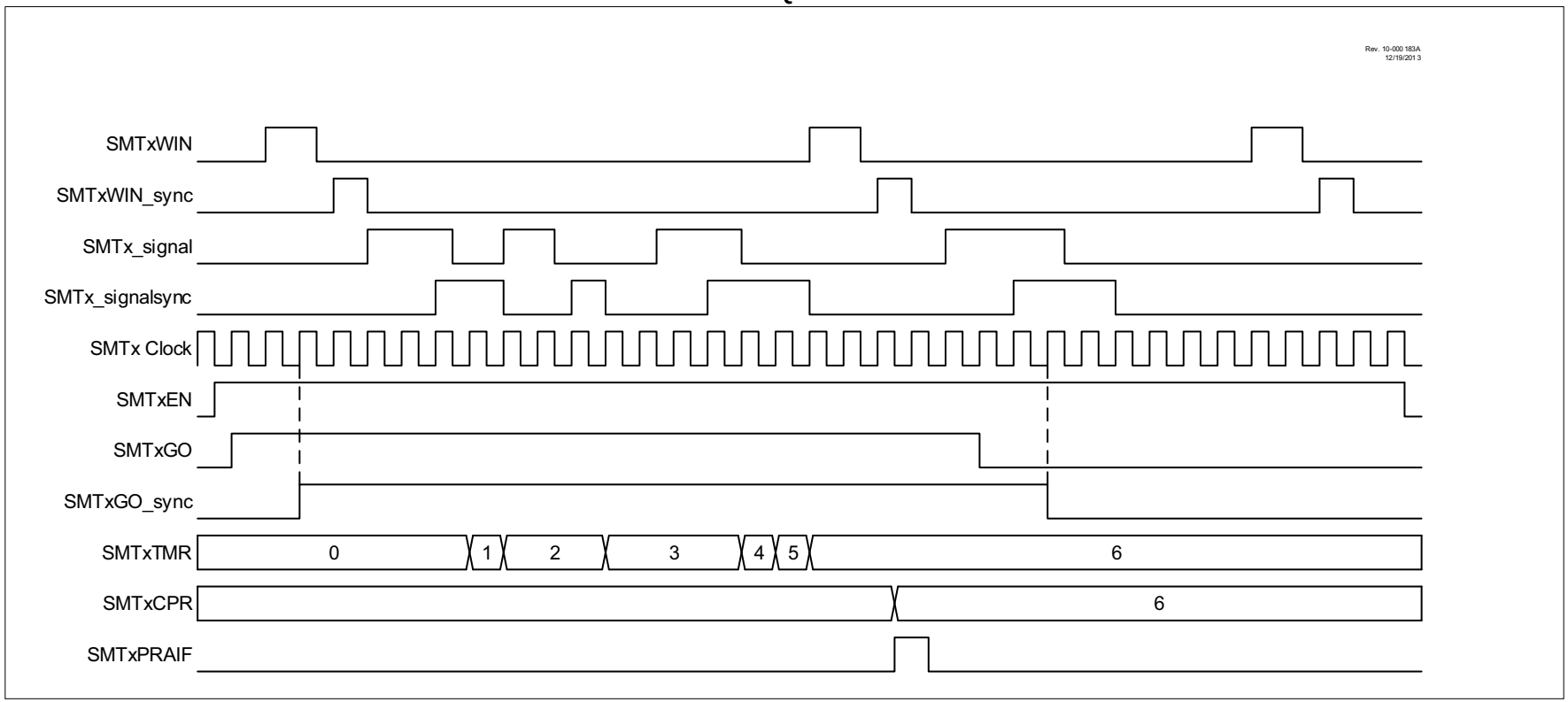
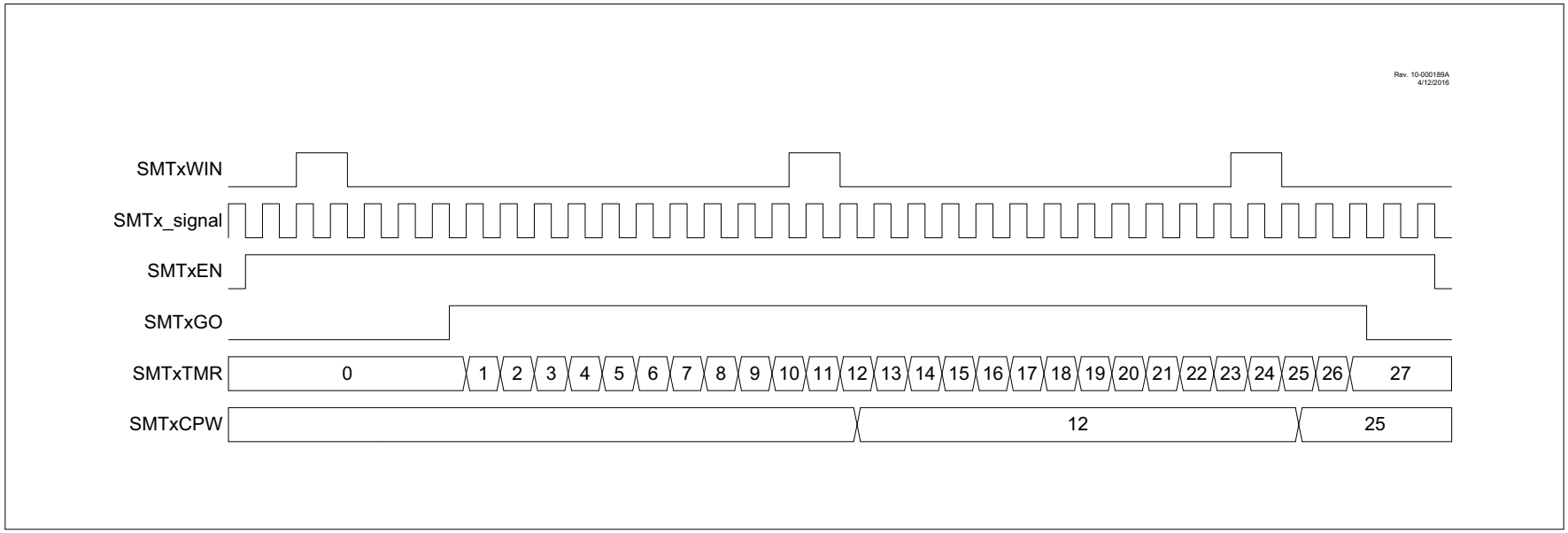


**FIGURE 30-18: COUNTER MODE TIMING DIAGRAM**



### 30.6.11 WINDOWED COUNTER MODE

This mode counts pulses on the SMTx_signal input, within a window dictated by the SMTxWIN input. It begins counting upon seeing a rising edge of the SMTxWIN input, updates the SMTxCPW register on a falling edge of the SMTxWIN input, and updates the SMTxCPR register on each rising edge of the SMTxWIN input beyond the first. See Figure 30-21 and Figure 30-22.

**REGISTER 30-18: SMTxPRL: SMT PERIOD REGISTER – LOW BYTE**

| R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 |
|---|---|---|---|---|---|---|---|
| SMTxPR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **SMTxPR<7:0>**: Significant bits of the SMT Timer Value for Period Match – Low Byte

**REGISTER 30-19: SMTxPRH: SMT PERIOD REGISTER – HIGH BYTE**

| R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 |
|---|---|---|---|---|---|---|---|
| SMTxPR<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

bit 7-0 **SMTxPR<15:8>**: Significant bits of the SMT Timer Value for Period Match – High Byte

**REGISTER 30-20: SMTxPRU: SMT PERIOD REGISTER – UPPER BYTE**

| R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 | R/W-x/1 |
|---|---|---|---|---|---|---|---|
| SMTxPR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | |

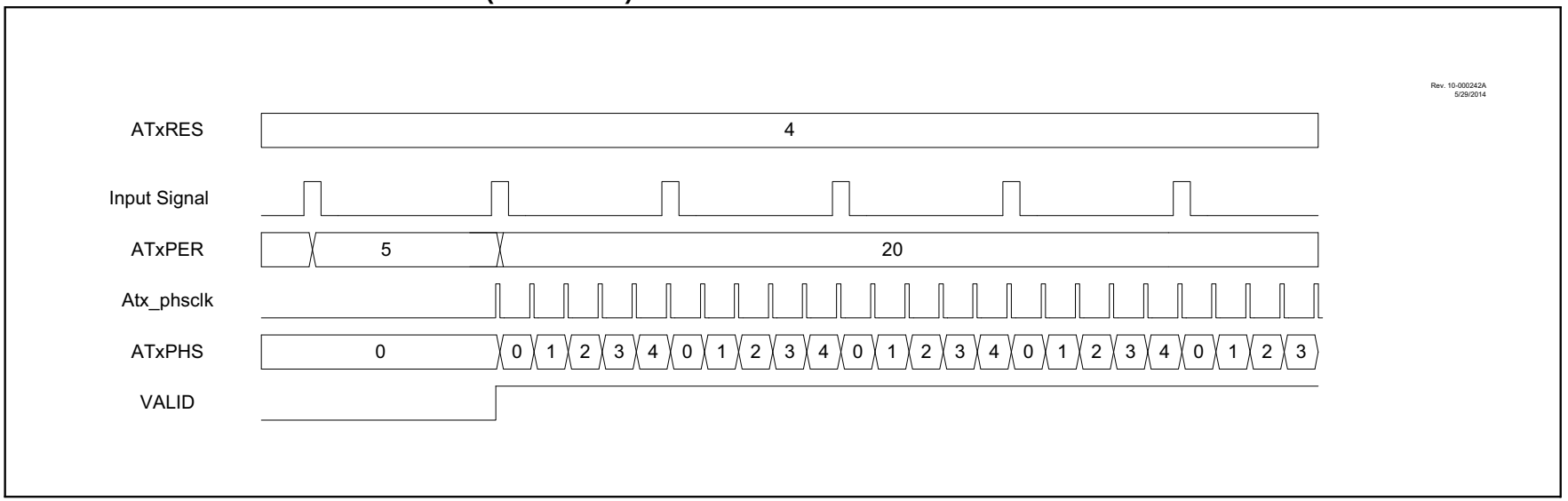
bit 7-0 **SMTxPR<23:16>**: Significant bits of the SMT Timer Value for Period Match – Upper Byte

**TABLE 30-3: SUMMARY OF REGISTERS ASSOCIATED WITH SMTx**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Register on Page |
|---|---|---|---|---|---|---|---|---|---|
| PIE4 | SCANIE | CRCIE | SMT2PWAIE | SMT2PRAIE | SMT2IE | SMT1PWAIE | SMT1PRAIE | SMT1IE | 109 |
| PIR4 | SCANIF | CRCIF | SMT2PWAIF | SMT2PRAIF | SMT2IF | SMT1PWAIF | SMT1PRAIF | SMT1IF | 114 |
| SMT1CON0 | EN | — | STP | WPOL | SPOL | CPOL | SMT1PS<1:0> | | 445 |
| SMT1CON1 | SMT1GO | REPEAT | — | — | MODE<3:0> | | | | 446 |
| SMT1CPRH | SMT1CPR<15:8> | | | | | | | | 454 |
| SMT1CPRL | SMT1CPR<7:0> | | | | | | | | 454 |
| SMT1CPRU | SMT1CPR<23:16> | | | | | | | | 454 |
| SMT1CPWH | SMT1CPW<15:8> | | | | | | | | 455 |
| SMT1CPWL | SMT1CPW<7:0> | | | | | | | | 455 |
| SMT1CPWU | SMT1CPW<23:16> | | | | | | | | 455 |
| SMT1PRH | SMT1PR<15:8> | | | | | | | | 456 |
| SMT1PRL | SMT1PR<7:0> | | | | | | | | 456 |
| SMT1PRU | SMT1PR<23:16> | | | | | | | | 456 |
| SMT1SIG | — | — | — | SSEL<4:0> | | | | | 451 |
| SMT1STAT | CPRUP | CPWUP | RST | — | — | TS | WS | AS | 447 |
| SMT1TMRH | SMT1TMR<15:8> | | | | | | | | 453 |
| SMT1TMRL | SMT1TMR<7:0> | | | | | | | | 453 |
| SMT1TMRU | SMT1TMR<23:16> | | | | | | | | 453 |
| SMT1WIN | — | — | — | WSEL<4:0> | | | | | 449 |
| SMT2CLK | — | — | — | — | — | CSEL<2:0> | | | 448 |
| SMT2CON0 | EN | — | STP | WPOL | SPOL | CPOL | SMT2PS<1:0> | | 445 |
| SMT2CON1 | SMT2GO | REPEAT | — | — | MODE<3:0> | | | | 446 |
| SMT2CPRH | SMT2CPR<15:8> | | | | | | | | 454 |
| SMT2CPRL | SMT2CPR<7:0> | | | | | | | | 454 |
| SMT2CPRU | SMT2CPR<23:16> | | | | | | | | 454 |
| SMT2CPWH | SMT2CPW<15:8> | | | | | | | | 455 |
| SMT2CPWL | SMT2CPW<7:0> | | | | | | | | 455 |
| SMT2CPWU | SMT2CPW<23:16> | | | | | | | | 455 |
| SMT2PRH | SMT2PR<15:8> | | | | | | | | 456 |
| SMT2PRL | SMT2PR<7:0> | | | | | | | | 456 |
| SMT2PRU | SMT2PR<23:16> | | | | | | | | 456 |
| SMT2SIG | — | — | — | — | — | SSEL<2:0> | | | 451 |
| SMT2STAT | CPRUP | CPWUP | RST | — | — | TS | WS | AS | 447 |
| SMT2TMRH | SMT2TMR<15:8> | | | | | | | | 453 |
| SMT2TMRL | SMT2TMR<7:0> | | | | | | | | 453 |
| SMT2TMRU | SMT2TMR<23:16> | | | | | | | | 453 |
| SMT2WIN | — | — | — | WSEL<4:0> | | | | | 448 |

**Legend:** x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for SMTx module.

**FIGURE 31-6: EXAMPLE OPERATION (ATxRES = 4)**



**REGISTER 31-9: ATxPERH: ANGULAR TIMER MEASURED PERIOD HIGH REGISTER**

| R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x |
|---|---|---|---|---|---|---|---|
| POV | PER<14:8> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | q = Value depends on condition |

bit 7 **POV:** Period Counter Overflow bit
1 = Counter rolled over one or more times during measurement
0 = Value shown by ATxPER is valid

bit 6-0 **PER<14:8>:** Most Significant bits of ATxPER. ATxPER is the measured period value from the period counter.

**REGISTER 31-10: ATxPERL: ANGULAR TIMER MEASURED PERIOD LOW REGISTER**

| R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x | R-x/x |
|---|---|---|---|---|---|---|---|
| PER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ |
| u = Bit is unchanged | x = Bit is unknown | -n/n = Value at POR and BOR/Value at all other Resets |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | q = Value depends on condition |

bit 7-0 **PER<7:0>:** Least Significant bits of ATxPER. ATxPER is the measured period value from the period counter.

**Note:** Unless otherwise noted, VIN = 5V, FOSC = 500 kHz, CIN = 0.1 µF, TA = 25°C.

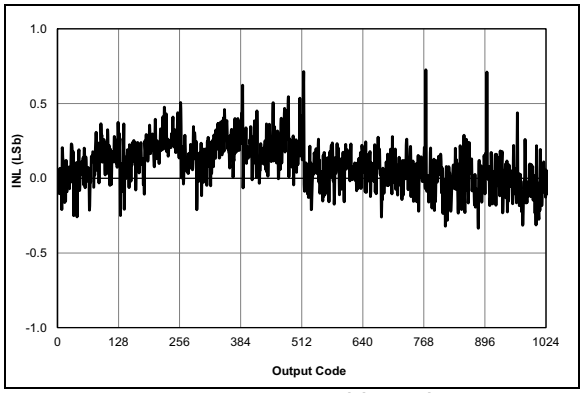



***FIGURE 36-73:*** *ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1 µS, 25°C.*

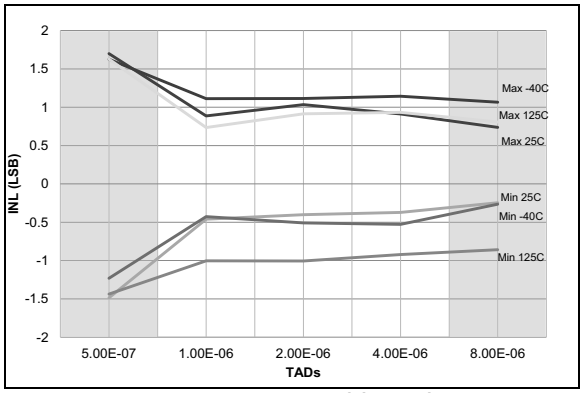



***FIGURE 36-76:*** *ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, VREF = 3.0V.*

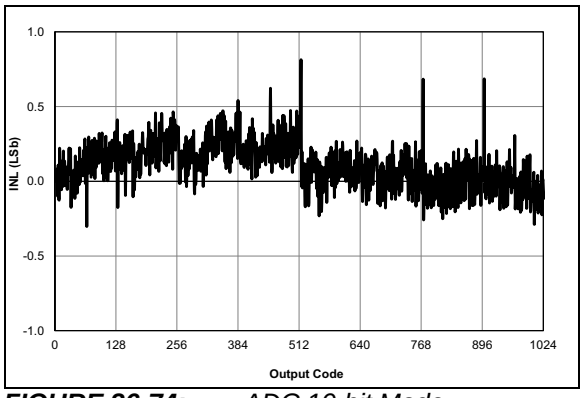



***FIGURE 36-74:*** *ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 4 µS, 25°C.*

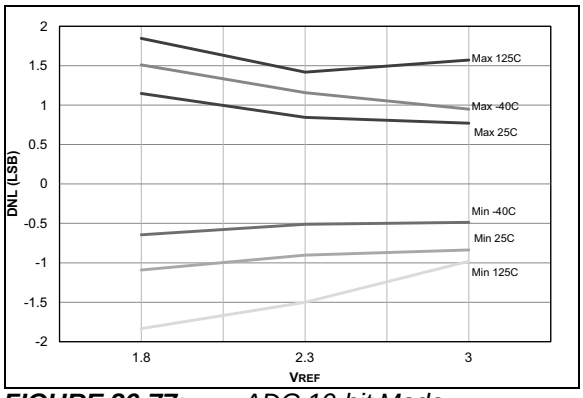



***FIGURE 36-77:*** *ADC 10-bit Mode, Single-Ended DNL, VDD = 3.0V, TAD = 1 µS.*

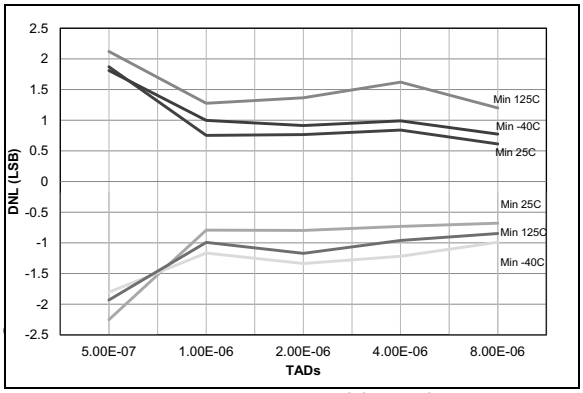



***FIGURE 36-75:*** *ADC 10-bit Mode, Single-Ended DNL, VDD = 3.0V, VREF = 3.0V.*

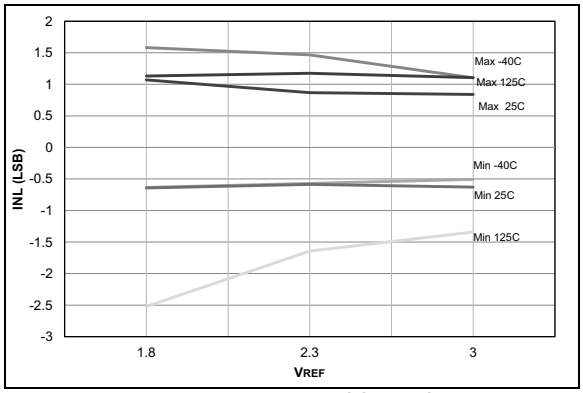



***FIGURE 36-78:*** *ADC 10-bit Mode, Single-Ended INL, VDD = 3.0V, TAD = 1 µS.*

**Note:** Unless otherwise noted, VIN = 5V, FOSC = 500 kHz, CIN = 0.1 µF, TA = 25°C.

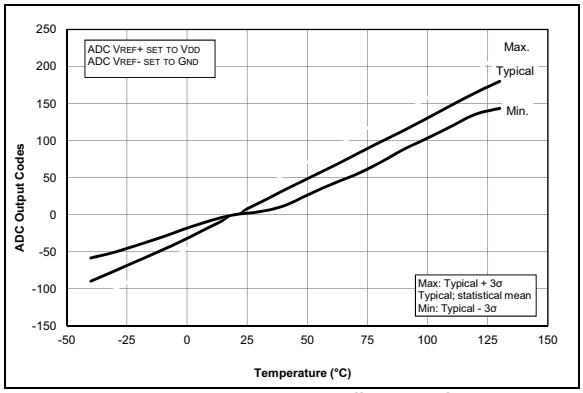



***FIGURE 36-85:*** *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 1.8V, PIC16LF1615/9 Only.*

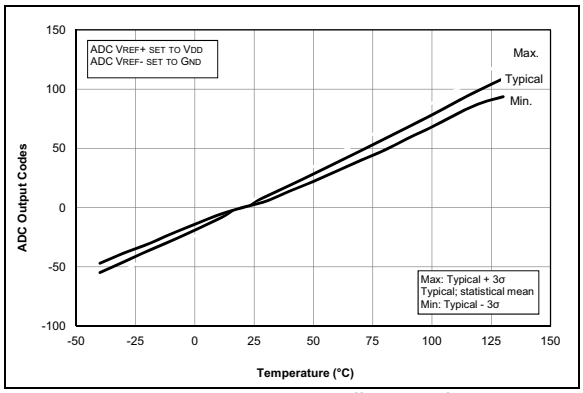



***FIGURE 36-86:*** *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16LF1615/9 Only.*

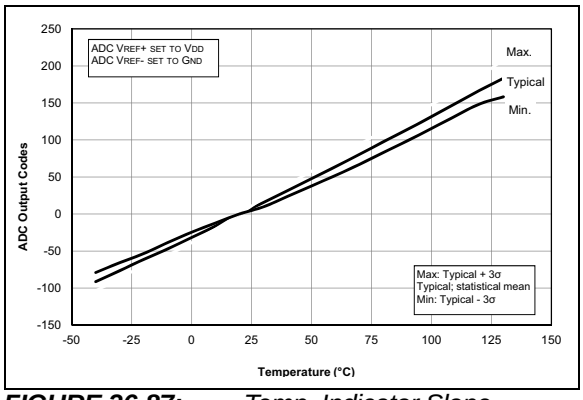



***FIGURE 36-87:*** *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16LF1615/9 Only.*

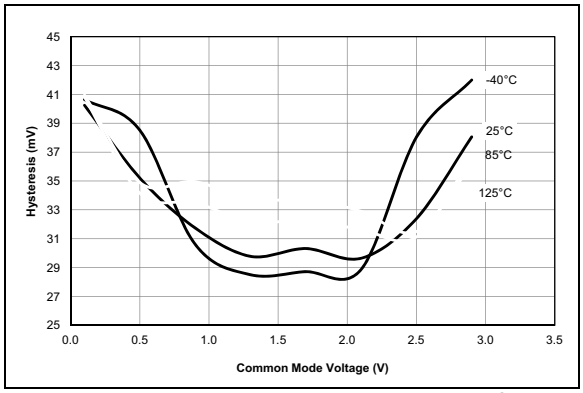



***FIGURE 36-88:*** *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values.*

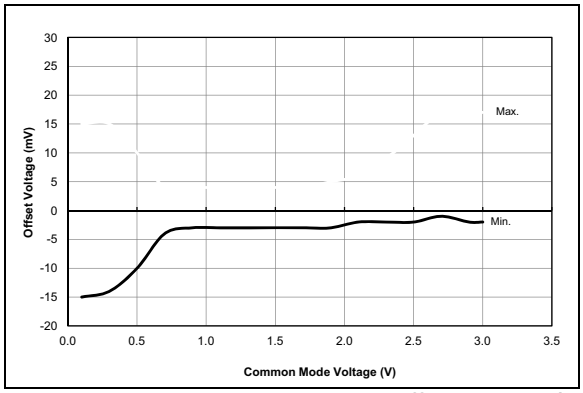



***FIGURE 36-89:*** *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values at 25°C.*

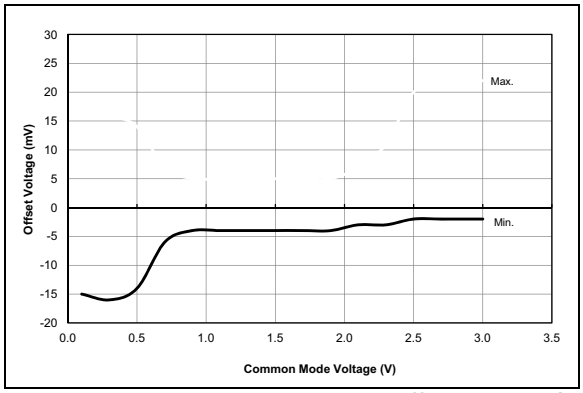



***FIGURE 36-90:*** *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values From -40°C to 125°C.*

## 38.2 Package Details

The following sections give the technical details of the packages.

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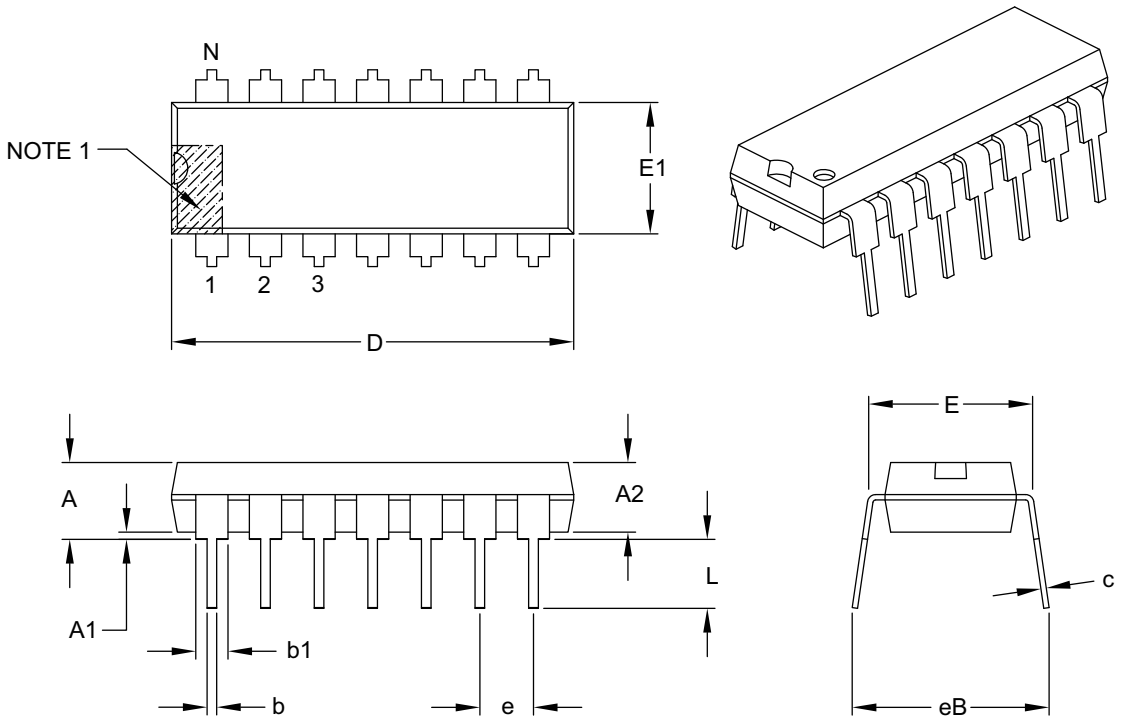
### 14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 14 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .735 | .750 | .775 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B