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Core Size	8-Bit
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Connectivity	-
Peripherals	-
Number of I/O	40
Program Memory Size	6KB (4K x 12)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	262 x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/parallax/sx52bd

Table of Contents

2.2 Pin Descriptions

Name	Pin Type	Input Levels	Description
RA0	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA1	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA2	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA3	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability
RA4	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability (52-pin pkg. only)
RA5	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability (52-pin pkg. only)
RA6	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability (52-pin pkg. only)
RA7	I/O	TTL/CMOS	Bidirectional I/O Pin; symmetrical source / sink capability (52-pin pkg. only)
RB0	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator output; MIWU/Interrupt input
RB1	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator negative input; MIWU/Interrupt input
RB2	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; comparator positive input; MIWU/Interrupt input
RB3	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU/Interrupt input
RB4	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU/Interrupt input, Timer T1 Capture Input 1
RB5	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU/Interrupt input, Timer T1 Capture Input 2
RB6	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU/Interrupt input, Timer T1 PWM/Compare Output
RB7	I/O	TTL/CMOS/ST	Bidirectional I/O Pin; MIWU/Interrupt input, Timer T1 External Event Input
RC0	I/O	TTL/CMOS/ST	Bidirectional I/O pin, Timer T2 Capture Input 1
RC1	I/O	TTL/CMOS/ST	Bidirectional I/O pin, Timer T2 Capture Input 2
RC2	I/O	TTL/CMOS/ST	Bidirectional I/O pin, Timer T2 PWM/Compare Output
RC3	I/O	TTL/CMOS/ST	Bidirectional I/O pin, Timer T2 External Event Counter Input
RC4	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC5	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC6	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RC7	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD0	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD1	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD2	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD3	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD4	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD5	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD6	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RD7	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE0	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE1	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE2	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE3	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE4	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE5	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE6	I/O	TTL/CMOS/ST	Bidirectional I/O pin
RE7	I/O	TTL/CMOS/ST	Bidirectional I/O pin
$\overline{\text{RTCC}}$	I	ST	Input to Real-Time Clock/Counter
$\overline{\text{MCLR}}$	I	ST	Master Clear reset input – active low
OSC1/In/Vpp	I	ST	Crystal oscillator input – external clock source input
OSC2/Out	O	CMOS	Crystal oscillator output – in R/C mode, internally pulled to V_{dd} through weak pull-up
V_{dd}	P	–	Positive supply pins (a total of four positive supply pins, one on each side of the device)
Vss	P	–	Ground pins (a total of four ground pins, one on each side of the device)
Note: I = input, O = output, I/O = Input/Output, P = Power, TTL = TTL input, CMOS = CMOS input, ST = Schmitt Trigger input, MIWU = Multi-Input Wakeup input			

2.3 Part Numbering

Table 1. Ordering Information

Device	Pins	I/O	Max. Operating Frequency (MHz)	EE/Flash (Words)	RAM (Bytes)	Voltage Range (V)	Operating Temp. (°C)
SX48BD/TQ	48	36	50	4K	262	3.0 - 5.5	-40°C to +85°C
SX48BD/TQ	48	36	75	4K	262	4.5 - 5.5	0°C to +70°C
SX52BD/PQ	52	40	50	4K	262	3.0 - 5.5	-40°C to +85°C
SX52BD/PQ	52	40	75	4K	262	4.5 - 5.5	0°C to +70°C

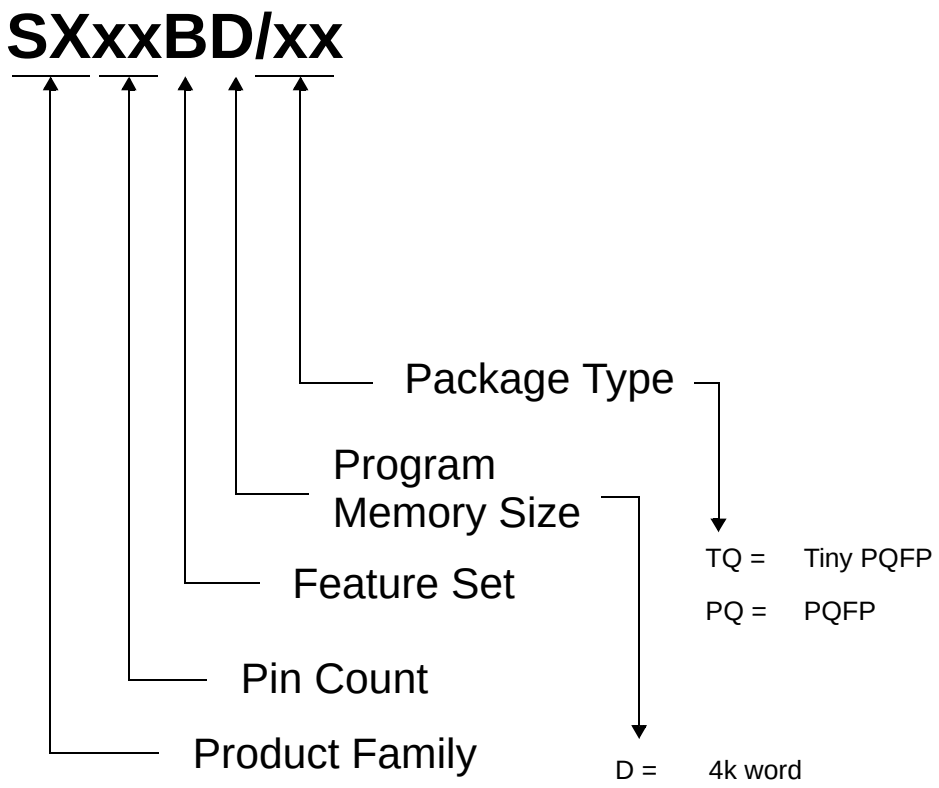


Figure 2-1. Part Number Reference Guide

3.0 PORT DESCRIPTIONS

The device contains five 8-bit I/O ports (Port A through Port E). Port A provides symmetrical drive capability. In the 48-pin version of the device, Port A has only four pins rather than eight. The unavailable pins are pulled high. Each port has four associated 8-bit registers (Direction, Data, TTL/CMOS Select, and Pull-Up Enable) to configure each port pin as Hi-Z input or output, to select TTL or CMOS voltage levels, and to enable/disable the weak pull-up resistor. The least significant bit of the registers corresponds to the least significant port pin. To access these configuration registers, an appropriate value must be written into the MODE register.

Upon power-up, all bits in these registers are initialized to "1".

The associated registers allow for each port bit to be individually configured under software control as shown below:

Table 3-1. Port Configuration

Data Direction Registers: RA, RB, RC, RD, RE		TTL/CMOS Select Registers: LVL_A, LVL_B, LVL_C, LVL_D, LVL_E		Pullup Enable Registers: PLP_A, PLP_B, PLP_C, PLP_D, PLP_E	
0	1	0	1	0	1
Output	Hi-Z Input	CMOS	TTL	Enable	Disable

Ports B, C, D, and E have additional associated registers (Schmitt-Trigger Enable Registers ST_B and ST_C) to enable or disable the Schmitt Trigger function on each individual port pin as indicated in table below.

Table 3-2. Schmitt Trigger Select

Schmitt Trigger Enable Registers: ST_B, ST_C, ST_D, ST_E	
0	1
Enable	Disable

Port B also supports the on-chip differential comparator. Ports RB1 and RB2 are the comparator negative and positive inputs, respectively, while Port RB0 is the comparator output pin. Port B also supports the Multi-Input Wakeup feature on all eight pins.

Port B and Port C also support the multi-function timers T1 and T2. RB4 and RB5 are the T1 capture inputs, RB6 is the T1 PWM output, and RB7 is the T1 external event counter input. Similarly, RC0 and RC1 are the T2 capture inputs, RC2 is the T2 PWM output, and RC3 is the T2 external event counter input.

Figure 3-1 shows the internal hardware structure and configuration registers for each pin of Port A. Figure 3-2 shows the same for each pin of Port B, C, D, or E.

3.1 Reading and Writing the Ports

The five ports are memory-mapped into the data memory address space. To the CPU, the five ports are available as the RA, RB, RC, RD, and RE file registers at data memory addresses 05h through 09h, respectively. Writing to a port data register sets the voltage levels of the corresponding port pins that have been configured to operate as outputs. Reading from a data register reads either the voltage levels of the corresponding port pins or the data contained in the port data register depending on the status PORTRD bit contained in the T2CNTB register.

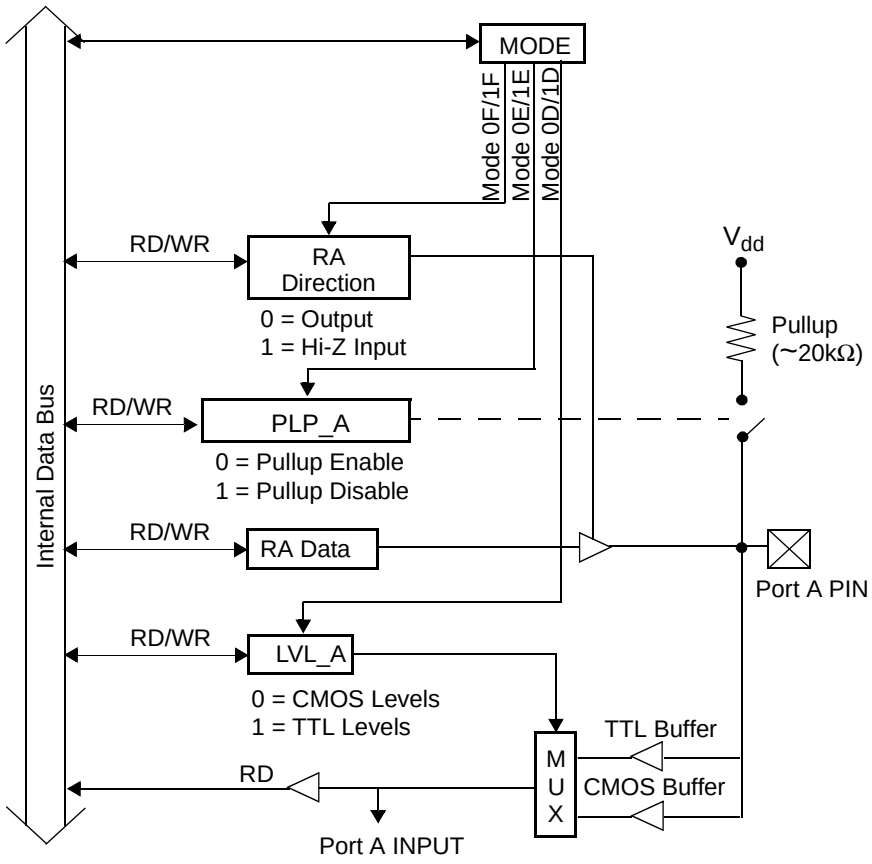


Figure 3-1. Port A Configuration

3.2 Read-Modify-Write Considerations

When two successive instructions are used on the same I/O port (except “mov Rx,W”) with a very high clock rate, the “write” part of one instruction might not occur soon enough before the “read” part of the very next instruction, resulting in getting “old” data for the second instruction. To ensure predictable results, avoid using two successive read-modify-write instructions that access the same port data register if the clock rate is high or, insert 3 NOP instructions between the successive read-modify-write instructions (if SYNC bit in the FUSE register is enabled, 5 NOP instructions are required), for operating frequencies of 50 MHz or lower. If bit 7 of the T2CNTB (PORTRD) is set, the port reads data from the data register instead of port pins. In this case, the NOP instructions are not required.

3.3 Port Configuration

Each port pin offers the following configuration options:

- data direction
- input voltage levels (TTL or CMOS)
- pullup type (enable or disable)
- Schmitt trigger input (except for Port A)

Port B offers the additional option to use the port pins for the Multi-Input Wakeup/Interrupt function, the analog comparator function, or Timer T1 I/O. Port C offers the additional option to use the port pins for Timer T2 I/O.

Port configuration is performed by writing to a set of control registers associated with the port. A special-purpose instruction is used to write these control registers:

- mov !RA,W (move W to/from Port A control register)
- mov !RB,W (move W to/from Port B control register)
- mov !RC,W (move W to/from Port C control register)
- mov !RD,W (move W to/from Port D control register)
- mov !RE,W (move W to/from Port E control register)

Each one of these instructions reads or writes a port control register for Port A, B, C, D, or E. There are multiple control registers for each port. To specify which one you want to access, you use another register called the MODE register.

3.3.1 MODE Register

The MODE register controls access to the port configuration registers and Timer T1/T2 control registers. Because the MODE register is not memory-mapped, it is accessed by the following special-purpose instructions:

- mov M, #lit (move literal to lower 4-bits of MODE register)
- mov M,W (move W to lower 5-bits of MODE register)
- mov W,M (move MODE register to W)

The value contained in the MODE register determines which port control register is accessed by the “mov !rx,W” instruction as indicated in Table 3-3. (The table also shows the timer control registers accessed according to the MODE register setting.) MODE register values not defined in the table are reserved for future expansion and should not be used. Upon power-up, the MODE register is initialized to 1Fh, which enables write access to the port direction control registers.

When bit 4 of the MODE register is 0 (the top half of Table 3-3), a “mov !rx,W” instruction moves the contents of the applicable control register into W. When bit 4 of the MODE register is 1 (the bottom half of Table 3-3), a “mov !rx,W” instruction moves the contents of W into the applicable control register. However, there are some exceptions to this. For the CMP_B and WKPND_B registers, the CPU does an exchange of data between W and the control register, regardless of the state of bit 4 in the MODE register. For the WKED_B and WKEN_B registers, the CPU moves the data from W to the control register, regardless of the state of bit 4 in the MODE register.

After a value is written to the MODE register, that setting remains in effect until it is changed by writing to the MODE register again. For example, you can write the value 1Eh to the MODE register just once, and then write to each of the five pullup configuration registers using the five “mov !rx,W” instructions.

Table 3-3. Mode Register Settings

MODE Reg.	mov !RA,W	mov !RB,W	mov !RC,W	mov !RD,W	mov !RE,W
00h		Read T1CPL	Read T2CPL		
01h		Read T1CPH	Read T2CPH		
02h		Read T1R2CML	Read T2R2CML		
03h		Read T1R2CMH	Read T2R2CMH		
04h		Read T1R1CML	Read T2R1CML		
05h		Read T1R1CMH	Read T2R1CMH		
06h		Read T1CNTB	Read T2CNTB		
07h		Read T1CNTA	Read T2CNTA		
08h		Exchange CMP_B with W			
09h		Exchange WKPND_B with W			
0Ah		Write WKED_B			
0Bh		Write WKEN_B			
0Ch		Read ST_B	Read ST_C	Read ST_D	Read ST_E
0Dh	Read LVL_A	Read LVL_B	Read LVL_C	Read LVL_D	Read LVL_E
0Eh	Read PLP_A	Read PLP_B	Read PLP_C	Read PLP_D	Read PLP_E
0Fh	Read RA Direction	Read RB Direction	Read RC Direction	Read RD Direction	Read RE Direction
10h		Clear Timer T1	Clear Timer T2		
11h					
12h		Write T1R2CML	Write T2R2CML		
13h		Write T1R2CMH	Write T2R2CMH		
14h		Write T1R1CML	Write T2R1CML		
15h		Write T1R1CMH	Write T2R1CMH		
16h		Write T1CNTB	Write T2CNTB		
17h		Write T1CNTA	Write T2CNTA		
18h		Exchange CMP_B with W			
19h		Exchange WKPND_B with W			
1Ah		Write WKED_B			
1Bh		Write WKEN_B			
1Ch		Write ST_B	Write ST_C	Write ST_D	Write ST_E
1Dh	Write LVL_A	Write LVL_B	Write LVL_C	Write LVL_D	Write LVL_E
1Eh	Write PLP_A	Write PLP_B	Write PLP_C	Write PLP_D	Write PLP_E
1Fh	Write RA Direction	Write RB Direction	Write RC Direction	Write RD Direction	Write RE Direction

The following code example shows how to program the pullup control registers.

```
mov  W,#$1E   ;MODE=1Eh to write port pullup
mov  M, W     ;registers

mov  W,#$03   ;W = 0000 0011
mov  !RA,W    ;disable pullups for A0 and A1

mov  W,#$FF   ;W = 1111 1111
mov  !RB,W    ;disable all pullups for B0-B7

mov  W,#$00   ;W = 0000 0000
mov  !RC,W    ;enable all pullups for C0-C7
```

First the MODE register is loaded with 1Eh to select write access to the pullup control registers (PLP_A, PLP_B, and so on). Then the MOV !rx,W instructions are used to specify which port pins are to be connected to the internal pullup resistors. Setting a bit to 1 disconnects the corresponding pullup resistor, and clearing a bit to 0 connects the corresponding pullup resistor.

7.0 INTERRUPT SUPPORT

The device supports both internal and external maskable interrupts. The internal interrupt is generated as a result of the RTCC rolling over from FFh to 00h. This interrupt source has an associated enable bit located in the OPTION register and pending flag bit in the Timer T1 Control B register. In addition, timers T1 and T2 each have three interrupt sources associated with counter overflow, compare match, and input capture.

Port B provides the source for eight external software selectable, edge sensitive interrupts, when the device is not in the power down mode. These interrupt sources share logic with the Multi-Input Wakeup circuitry. The WKEN_B register allows interrupt from Port B to be individually enabled or disabled. Clearing a bit in the WKEN_B register enables the interrupt on the corresponding Port B pin. The WKED_B selects the transition edge to be either positive or negative. The WKEN_B and WKED_B registers are set to FFh upon reset. Setting a bit in the WKED_B register selects the falling edge while clearing the bit selects the rising edge on the corresponding Port B pin.

The WKPND_B register serves as the external interrupt pending register.

The WKPND_B register comes up with a random value upon reset. The user program must clear the WKPND_B register prior to enabling the interrupt.

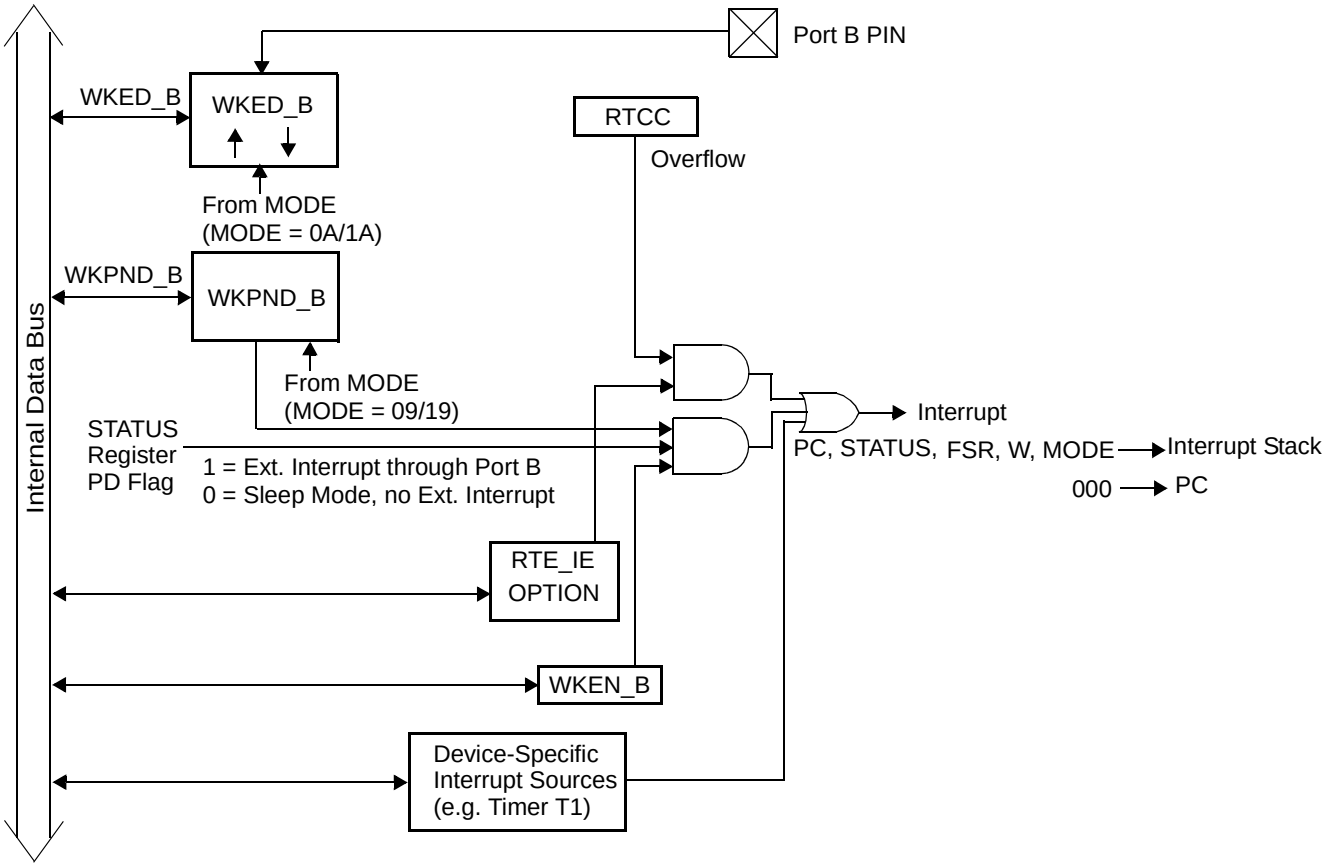


Figure 7-1. Interrupt Structure

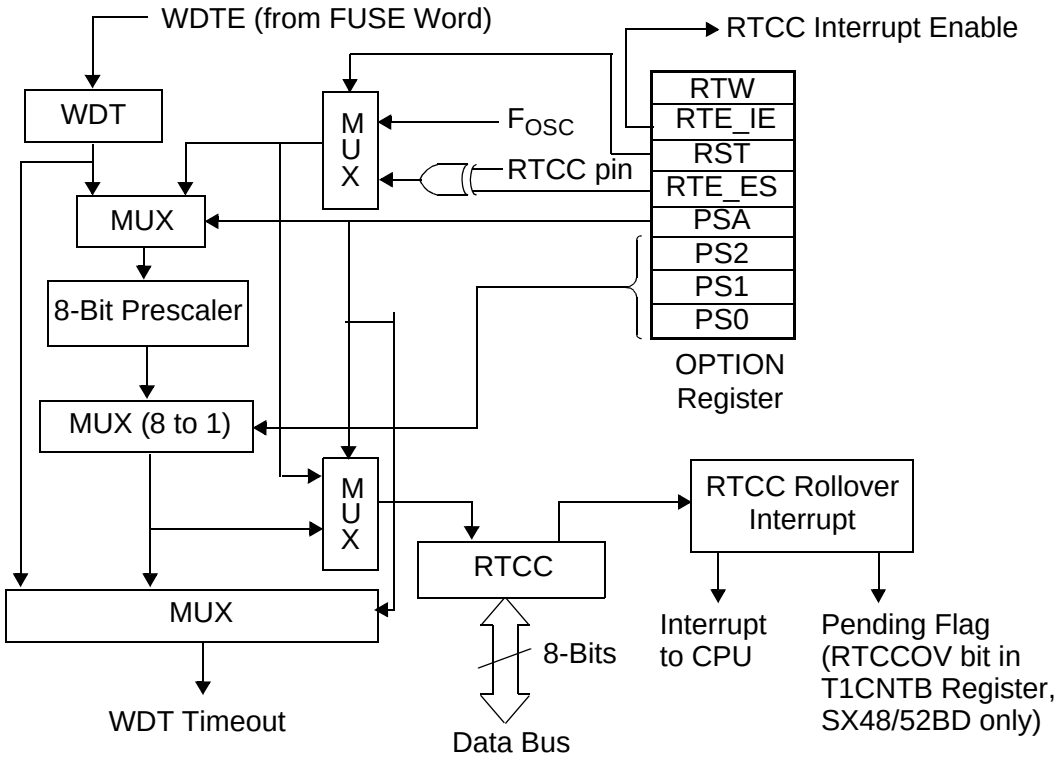


Figure 9-1. RTCC and WDT Block Diagram

10.0 MULTI-FUNCTION TIMERS

The device contains two independent 16-bit multi-function timers, designated T1 and T2. These versatile, programmable timers reduce the software burden on the CPU in real-time control applications such as PWM generation, motor control, triac control, variable-brightness display control, sine wave generation, and data acquisition.

Each timer consists of a 16-bit counter register supported by a dedicated 16-bit capture register and two 16-bit comparison registers. The second compare register can also serve as capture register. Each timer uses up to four I/O pins: one clocking input, two capture inputs, and one timer output. The timer I/O pins are alternate functions of Port B pins for timer T1 and Port C pins for Timer T2.

Figure 10-1 is a block diagram showing the registers and I/O pins of one timer. The 16-bit free-running timer/counter register is initialized to 0000h upon reset and counts upward continuously. It is clocked either by an external signal provided on an I/O pin or by the on-chip system clock divided by a 3-bit divide-by factor.

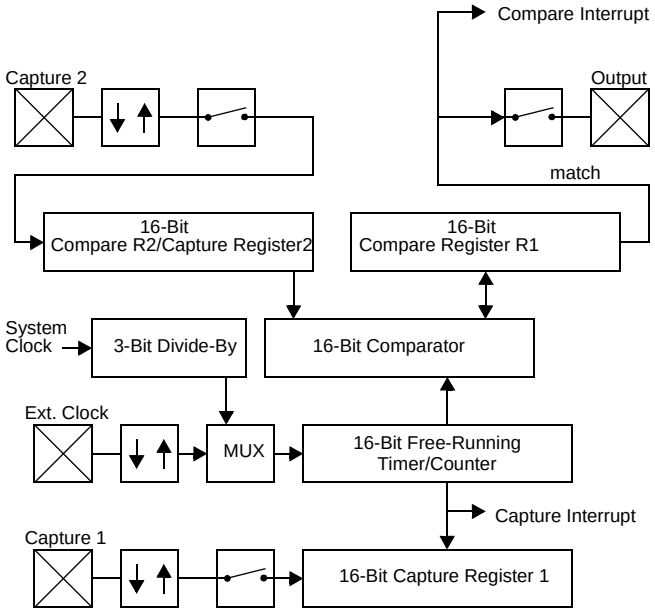


Figure 10-1. Multi-Function Timer Block Diagram

The CPU can access the Compare and Capture registers by using the “mov !RB,W” instruction for T1 or the “mov !RC,W” instruction for T2. The other timer registers are not directly accessible.

You can configure the timer to generate an interrupt upon overflow from FFFFh to 0000h, upon a match between the counter value and a programmed comparison value, or upon the occurrence of a valid capture signal on either of two capture inputs.

The timers can be cleared to 0000h by writing to the registers accessed via MODE address $10. Clearing the timer forces it to begin compare with R1.

The MODE register controls access to the timer registers. Because the MODE register is not memory mapped, it is accessed by the following special purpose insteructions:

- mov M, #lit (move literal to lower 4-bits of MODE register)
- mov M,W (move W to lower 5-bits of MODE register)
- mov W,M (move MODE register to W)

The value contained in the MODE register determines which timer register is accessed by the “mov !rx,W” instruction as indicated in Table 10-1.

10.1 Timer Registers

Each timer consists of several registers.

Timer T1 registers:

T1CPL - Lower byte of Timer T1 capture register

T1CPH - Higher byte of Timer T1 capture register

T1R1CML - Lower byte of Timer T1 compare register 1

T1R1CMH - Higher byte of Timer T1 compare register 1

T1R2CML - Lower byte of Timer T1 compare register 2

T1R2CMH - Higher byte of Timer T1 compare register 2

T1CNTA - Timer T1 control register A

T1CNTB - Timer T1 control register B

Timer T2 registers:

T2CPL - Lower byte of Timer T2 capture register

T2CPH - Higher byte of Timer T2 capture register

T2R1CML - Lower byte of Timer T2 compare register 1

T2R1CMH - Higher byte of Timer T2 compare register 1

T2R2CML - Lower byte of Timer T2 compare register 2

T2R2CMH - Higher byte of Timer T2 compare register 2

T2CNTA - Timer T1 control register A

T2CNTB - Timer T1 control register B

Table 10-1. Mode Register Settings for T1/T2 Registers

MODE Reg.	mov !RB,W	mov !RC,W
00h	Read T1CPL	Read T2CPL
01h	Read T1CPH	Read T2CPH
02h	Read T1R2CML	Read T2R2CML
03h	Read T1R2CMH	Read T2R2CMH
04h	Read T1R1CML	Read T2R1CML
05h	Read T1R1CMH	Read T2R1CMH
06h	Read T1CNTB	Read T2CNTB
07h	Read T1CNTA	Read T2CNTA
12h	Write T1R2CML	Write T2R2CML
13h	Write T1R2CMH	Write T2R2CMH
14h	Write T1R1CML	Write T2R1CML
15h	Write T1R1CMH	Write T2R1CMH
16h	Write T1CNTB	Write T2CNTB
17h	Write T1CNTA	Write T2CNTA

10.2 Timer Operating Modes

Each timer can be configured to operate in one of the following modes:

- Pulse Width Modulation (PWM) mode
- Software Timer mode
- External Event mode
- Capture/Compare mode

10.2.1 PWM Mode

In the Pulse Width Modulation (PWM) mode, the timer generates an output signal having a programmable frequency and duty cycle. To use this mode, you load two 16-bit comparison registers, R1 and R2, with the number of timer clock cycles that you want the output signal to be high and low. The contents of R1 define the PWM low time while the contents of R2 define the PWM high time.

After the “Clear Timer” command is initiated through the MODE register, the timer starts from zero and counts up until it reaches the value in R1. At that point, it generates an interrupt (if enabled), toggles the output signal to a logic high level, and starts counting from zero again. The second time, it counts up until it reaches the value in R2. At that point, it again generates an interrupt (if enabled), toggles the output signal to a logic low level, and starts counting from zero again. This process is repeated continuously, alternating between R1 and R2 to obtain the value at which to toggle the output signal and return the counter to zero. The values of R1 and R2 establish the duty cycle and frequency of the output signal. If R1 and R2 contain the same value, the resulting output signal is a square wave. If R1 is changed to a value less than the timer count while the timer is counting to match R1, the timer will continue to count through FFFFh, and back up to the R1 value, while the output is low. Same is true for R2, except the output signal will be high.

Upon reset, the timer/counter is initialized to 0000.

In the PWM mode, the timer is clocked by the on-chip system clock divided by an 8-bit prescaler value. The divide-by factor can be set to any power-of-2 from 1 to 256. Thus, the period of the timer clock can be set from 1 to 256 times the system clock period.

Upon entering the PWM mode, the internally generated PWM signal is connected to the designated PWM output pin. The PWM mode bypasses the port data register (does not affect the contents of the data register). For the PWM output signal to appear on the pin (RB6 for T1, RC2 for T2), the corresponding port pin direction register must be configured for output.

10.2.2 Software Timer Mode

The Software Timer mode is the same as the PWM mode, except that the timer does not toggle the output signal. Instead, the application program takes action in response to the internally generated PWM signal upon each match between the counter and the contents of the active comparison value in either R1 or R2. The software can determine the cause of each interrupt by checking the timer interrupt pending flags. There are different flag bits associated with each type of event (R1 match, R2 match, and overflow).

10.2.3 External Event Mode

The External Event mode is the same as the PWM mode, except that the counter register is clocked by an external signal provided on an input pin (RB7 for T1 and RC3 for T2) rather than by the system clock. This mode can be used to count the occurrences of external events. The input pin can be configured to sense either rising or falling edges.

10.2.4 Capture/Compare Mode

In the Capture/Compare mode, the counter counts upward continuously without interruption. A valid transition received on either of two input pins causes the current value of the counter to be captured in an associated capture register. This capture feature can be used to keep track of the elapsed time between successive external events. In addition, the timer continuously compares the counter value against the value programmed into the R1 register. Each time a match occurs, it toggles the timer output pin, generates an interrupt (if enabled) and sets an associated interrupt pending flag. The timer continues to count upward after a match occurs (unlike the PWM mode, which resets the counter to zero when a match occurs).

In the Capture/Compare mode, the timer is clocked by the on-chip system clock divided by a value defined by a 3-bit divide-by factor. The divide-by factor can be set to any power-of-2 from 1 to 128.

The two input capture pins are designated Capture 1 and Capture 2. They can be configured to sense either rising or falling edges. The Capture 1 pin captures the counter value in a dedicated 16-bit capture register, a read-only register. The Capture 2 pin captures the counter value in the R2 register. The occurrence of a capture event also generates an interrupt (if enabled) and sets an associated interrupt pending flag.

Overflow of the counter from FFFFh to 0000h also generates an interrupt (if enabled) and sets an associated interrupt pending flag. Because the counter is free-running, an overflow can occur at any time. In cases where the time between successive capture events might exceed 65,536 counts of the timer, the software should keep track of the number of overflows between successive events in order to determine the true amount of time between such events.

10.3 Timer Pin Assignments

The following table lists the I/O port pins associated with the Timer T1 and Timer T2 I/O functions.

Table 10-2. Timer T1/T2 Pin Assignments

I/O Pin	Timer T1/T2 Function
RB4	Timer T1 Capture Input 1
RB5	Timer T1 Capture Input 2
RB6	Timer T1 PWM/Compare Output
RB7	Timer T1 External Event Clock Source
RC0	Timer T2 Capture Input 1
RC1	Timer T2 Capture Input 2
RC2	Timer T2 PWM/Compare Output
RC3	Timer T2 External Event Clock Source

10.4 Timer Control Registers

There are two 8-bit control registers associated with each timer, called the Control A and Control B registers. The Control A register contains the interrupt enable bits and interrupt flag bits associated with the timer. (Interrupts are caused by comparison, capture, and overflow events.) The Control B register contains bits for setting the timer operating mode, the clock prescaler divide-by factor, and the input signal edge sensitivity. Each Control B register also contains one device configuration bit not related to operation of the multi-function timers.

The register formats are shown in the following diagrams.

Timer T1 Control B Register (T1CNTB)

RTCCOV	T1CPEDG	T1EXEDG	T1PS2-T1PS0			T1MC1-T1MC0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

RTCCOV — RTCC Overflow Flag. This flag is automatically set to 1 when the Real-Time Clock/Counter (RTCC) overflows from FFh to 00h. This flag stays set until it is cleared by the software. Note that this flag is not related to multi-function timers T1 and T2.

T1CPEDG — Timer T1 Capture Edge. This bit sets the edge sensitivity of the Timer T1 input capture pins, Capture 1 and Capture 2 (RB4 and RB5). Set this bit to 1 to sense positive-going (low-to-high) edges. Clear this bit to 0 to sense negative-going (high-to-low) edges.

T1EXEDG — Timer T1 External Event Clock Edge. This bit sets the edge sensitivity of the Timer T1 input used to count external events (RB7). Set this bit to 1 to sense positive-going (low-to-high) edges. Clear this bit to 0 to sense negative-going (high-to-low) edges.

T1PS2-T1PS0 — Timer T1 Prescaler Divider field. This 3-bit field specifies the divide-by factor for generating the timer clock from the on-chip system clock:

000 = divide by 1
001 = divide by 2
010 = divide by 4
011 = divide by 8
100 = divide by 16
101= divide by 32
110 = divide by 64
111 = divide by 128

For example, setting this field to 010 sets the divide-by factor to 4, which means that the T1 counter register is incremented once every four system clock cycles.

T1MC1-T1MC0 — Timer T1 Mode Control field. This 2-bit field specifies the Timer T1 operating mode as follows:

00 = Software Timer mode
01 = PWM mode
10 = Capture/Compare mode
11 = External Event mode

Timer T2 Control A Register (T2CNTA)

T2CPF2	T2CPF1	T2CPIE	T2CMF2	T2CMF1	T2CMIE	T2OVF	T2OVIE
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

T2CPF2 Timer T2 Capture Flag 2. In Capture/Compare mode, this flag is automatically set to 1 when a capture event occurs on the Capture 2 pin of Timer T2 (pin RC1). It stays set until cleared by the software.

T2CPF1 Timer T2 Capture Flag 1. In Capture/Compare mode, this flag is automatically set to 1 when a capture event occurs on the Capture 1 pin of Timer T2 (pin RC1). It stays set until cleared by the software.

T2CPIE Timer T2 Capture Interrupt Enable. Set this bit to 1 to enable capture interrupts for Timer T2 in Capture/Compare mode. In that case, an interrupt will occur each time a valid edge is received on the Capture 1 or Capture 2 pin of Timer T2. Clear this bit to 0 to disable capture interrupts.

T2CMF2 Timer T2 Comparison Flag 2. This flag is automatically set to 1 when the contents of the timer counter match the contents of R2, when R2 is the active comparison register. The flag stays set until it is cleared by the software.

T2CMF1 Timer T2 Comparison Flag 1. This flag is automatically set to 1 when the contents of the timer counter match the contents of R1, when R1 is the active comparison register. The flag stays set until it is cleared by the software.

T2CMIE Timer T2 Comparison Interrupt Enable. Set this bit to 1 to enable comparison interrupts for Timer T2. In that case, an interrupt will occur each time the contents of the timer counter match the contents of the active comparison register (R1 or R2) of Timer T2. Clear this bit to 0 to disable comparison interrupts.

T2OVF Timer T2 Overflow Flag. This flag is automatically set to 1 when the timer counter overflows from FFFFh to 0000h. The flag stays set until it is cleared by the software.

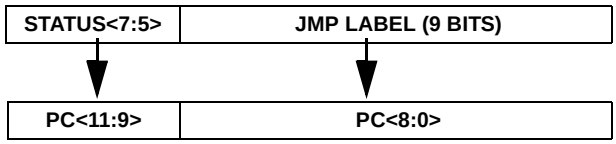
T2OVIE Timer T2 Overflow Interrupt Enable. Set this bit to 1 to enable overflow interrupts for Timer T2. In that case, an interrupt will occur each time Timer T2 overflows. Clear this bit to 0 to disable overflow interrupts.

15.9 Branch and Loop Call Instructions

The device contains an 8-level hardware stack where the return address is stored with a subroutine call. Multiple stack levels allow subroutine nesting. The instruction set supports absolute address branching.

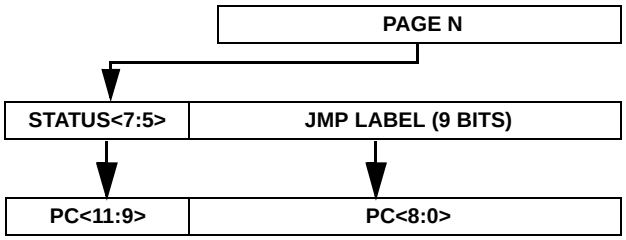
15.9.1 Jump Operation

When a JMP instruction is executed, the lower nine bits of the program counter are loaded with the address of the specified label. The upper three bits of the program counter are loaded with the page select bits, PA2:PA0, contained in the STATUS register. Therefore, care must be exercised to ensure the page select bits are pointing to the correct page *before* the jump occurs.



15.9.2 Page Jump Operation

When a JMP instruction is executed and the intended destination is on a different page, the page select bits must be initialized with appropriate values to point to the desired page before the jump occurs. This can be done easily with SETB and CLRB instructions or by writing a value to the STATUS register. The device also has the PAGE instruction, which automatically selects the page in a single-cycle execution.



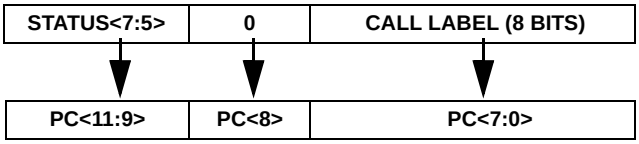
Note:“N” must be 0, 1, 2, or 3.

15.9.3 Call Operation

The following happens when a CALL instruction is executed:

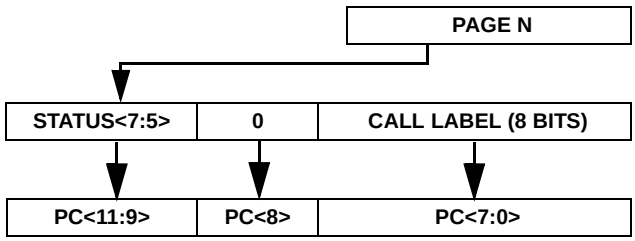
- The current value of the program counter is incremented and pushed onto the top of the stack.
- The lower eight bits of the label address are copied into the lower eight bits of the program counter.
- The ninth bit of the Program Counter is cleared to zero.
- The page select bits (in STATUS register) are copied into the upper three bits of the 12-bit program counter.

This means that the call destination must *start* in the lower half of any page. For example, 00h-0FFh, 200h-2FFh, 400h-4FFh, etc.



15.9.4 Page Call Operation

When a subroutine that resides on a different page is called, the page select bits must contain the proper values to point to the desired page before the call instruction is executed. This can be done easily using SETB and CLRB instructions or writing a value to the STATUS register. The device also has the PAGE instruction, which automatically selects the page in a single-cycle execution.



15.10 Return Instructions

The device has several instructions for returning from subroutines and interrupt service routines. The return from subroutine instructions are RET (return without affecting W), RETP (same as RET but affects PA2:PA0), RETI (return from interrupt), RETIW (return and add W to RTCC), and RETW #literal (return and place literal in W). The literal serves as an immediate data value from memory. This instruction can be used for table lookup operations. To do table lookup, the table must contain a string of RETW #literal instructions. The first instruction just in front of the table calculates the offset into the table. The table can be used as a result of a CALL.

Table 16-1. The SX Instruction Set (Continued)

Mnemonic, Operands	Description	Cycles	Opcode	Flags Affected
Bitwise Operations				
CLRB fr.bit	Clear Bit in fr (fr.bit = 0)	1	0100 bbbf ffff	none
SB fr.bit	Test Bit in fr and Skip if Set (test fr.bit and skip next instruction if bit is 1)	1 or 2 (skip)	0111 bbbf ffff	none
SETB fr.bit	Set Bit in fr (fr.bit = 1)	1	0101 bbbf ffff	none
SNB fr.bit	Test Bit in fr and Skip if Clear (test fr.bit and skip next instruction if bit is 0)	1 or 2 (skip)	0110 bbbf ffff	none
Data Movement Instructions				
MOV fr,W	Move W to fr (fr = W)	1	0000 001f ffff	none
MOV W,fr	Move fr to W (W = fr)	1	0010 000f ffff	Z
MOV W,fr-W	Move (fr-W) to W (W = fr - W); complement of carry flag is subtracted if $\overline{CF}$ bit in FUSEX register is cleared to 0	1	0000 100f ffff	C, DC, Z
MOV W,#lit	Move Literal to W (W = lit)	1	1100 kkkk kkkk	none
MOV W,/fr	Move Complement of fr to W (W = fr ^ FFh)	1	0010 010f ffff	Z
MOV W,--fr	Move (fr-1) to W (W = fr - 1)	1	0000 110f ffff	Z
MOV W,++fr	Move (fr+1) to W (W = fr + 1)	1	0010 100f ffff	Z
MOV W,<<fr	Rotate fr Left through Carry and Move to W (W = << fr)	1	0011 010f ffff	C
MOV W,>>fr	Rotate fr Right through Carry and Move to W (W = >> fr)	1	0011 000f ffff	C
MOV W,<>fr	Swap High/Low Nibbles of fr and move to W (W = <> fr)	1	0011 100f ffff	none
MOV W,M	Move MODE Register to W (W = MODE), high nibble of W cleared	1	0000 0100 0010	none
MOVSZ W,--fr	Move (fr-1) to W and Skip if Zero (W = fr -1 and skip next instruction if result is zero)	1 2 (skip)	0010 110f ffff	none
MOVSZ W,++fr	Move (fr+1) to W and Skip if Zero (W = fr + 1 and skip next instruction if result is zero)	1 2 (skip)	0011 110f ffff	none
MOV M,W	Move W to MODE Register (MODE = W)	1	0000 0100 0011	none
MOV M,#lit	Move Literal to MODE Register (MODE = lit, only lower 4 bits)	1	0000 0101 kkkk	none
MOV !rx,W	Move Data Between W and Control Register: rx = W (move W to rx) - MODE Reg bit 4 = 1 W = rx (move rx to W) - MODE Reg bit 4 = 0 rx <=> W (exchange W and rx) - MODE = x8 or x9	1	0000 0000 ffff	none
MOV !OPTION, W	Move W to OPTION Register (OPTION = W)	1	0000 0000 0010	none
TEST fr	Test fr for Zero (fr = fr to set or clear Z flag)	1	0010 001f ffff	Z
Program Control Instructions				

Table 16-1. The SX Instruction Set (Continued)

Mnemonic, Operands	Description	Cycles	Opcode	Flags Affected
CALL addr8	Call Subroutine: top-of-stack = program counter + 1 PC(7:0) = addr8 program counter (8) = 0 program counter (11:9) = PA2:PA0	3	1001 kkkk kkkk	none
JMP addr9	Jump to Address: PC(7:0) = addr9(7:0) program counter (8) = addr9(8) program counter (11:9) = PA2:PA0	3	101k kkkk kkkk	none
NOP	No Operation	1	0000 0000 0000	none
RET	Return from Subroutine (program counter = top-of-stack) Note: Not recommended, use RETP	3	0000 0000 1100	none
RETP	Return from Subroutine Across Page Boundary (PA2:PA0 = top-of-stack (11:9) and program counter = top-of-stack)	3	0000 0000 1101	PA2, PA1, PA0
RETI	Return from Interrupt (restore W, STATUS, FSR, MODE and program counter from shadow registers)	3	0000 0000 1110	all STATUS except TO, PD bits
RETIW	Return from Interrupt and add W to RTCC (restore W, STATUS, FSR, MODE and program counter from shadow registers; and add W to the RTCC register)	3	0000 0000 1111	all STATUS except TO, PD bits
RETW lit	Return from Subroutine with Literal in W (W = lit and program counter = top-of-stack)	3	1000 kkkk kkkk	none
System Control Instructions				
BANK addr12	Load Bank Number into FSR(6:4) FSR(6:4) = addr12(10:8)	1	0000 0001 1nnn	none
IREAD	Read Word from Instruction Memory MODE:W = data at address (MODE:W)	4	0000 0100 0001	none
PAGE addr12	Load Page Number into STATUS(7:5) STATUS(7:5) = addr12(11:9)	1	0000 0001 0nnn	PA2, PA1, PA0
SLEEP	Power Down Mode WDT = 00h, TO = 1, stop oscillator (PD = 0, clear prescaler if assigned)	1	0000 0000 0011	TO, PD

17.3 AC Characteristics

SX48BD/SX52BD running at 50MHz: Operating Temperature -40°C <= Ta <= +85°C (Industrial)

SX48BD/SX52BD running at 75MHz: Operating Temperature 0°C <= Ta <= +70°C (Commercial)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
F_{osc}	External CLKIN Frequency	DC	-	32.0	KHz	LP1
				1.0	MHz	LP2
				4.0	MHz	RC
				1.0	MHz	XT1
				8.0	MHz	XT2
				50.0	MHz	HS1/HS2/HS3
				75.0	MHz	HS3
	Oscillator Frequency	DC	-	32.0	KHz	LP1
	(Crystal/Resonator)	0.032		1.0	MHz	LP2
		DC		4.0	MHz	RC
		0.032		1.0	MHz	XT1
		1.0		8.0	MHz	XT2
		1.0		50.0	MHz	HS1/HS2/HS3
		1.0		75.0	MHz	HS3
T_{osc}	External CLKIN Period	31.25	-	-	µs	LP1
		1.0			µs	LP2
		250.0			ns	RC
		1.0			µs	XT1
		125.0			ns	XT2
		20.0			ns	HS1/HS2/HS3
		13.3			ns	HS3
	Oscillator Period	31.25	-	-	µs	LP1
	(Crystal/Resonator)	1.0		31.25	µs	LP2
		250.0		-	ns	RC
		1.0		31.25	µs	XT1
		125.0		1000	ns	XT2
		20.0		1000	ns	HS1/HS2/HS3
		13.3		-		HS3
T_{osL}, T_{osH}	Clock in (OSC1) Low or High Time	400	-	-	ns	LP1/LP2
		50.0			ns	XT1/XT2
		8.0			ns	HS1/HS2/HS3
		5.3			ns	HS3

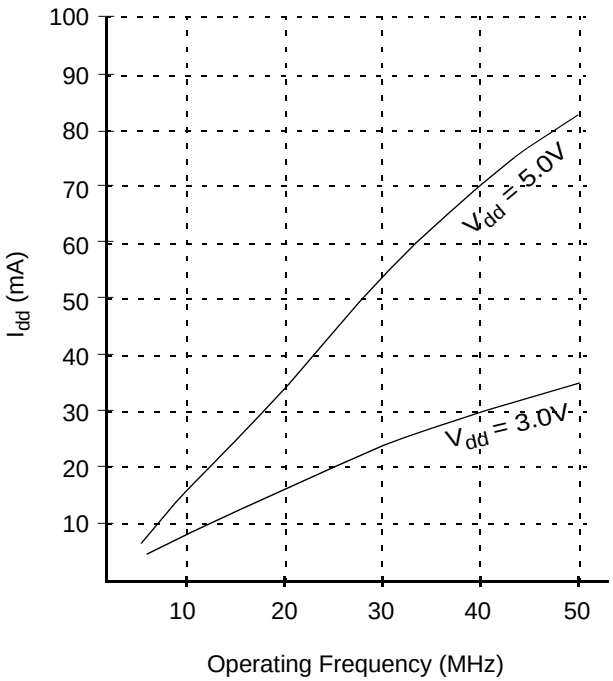
Note:Data in the Typical (“TYP”) column is at 5V, 25°C unless otherwise stated.

17.4 Comparator DC and AC Specifications

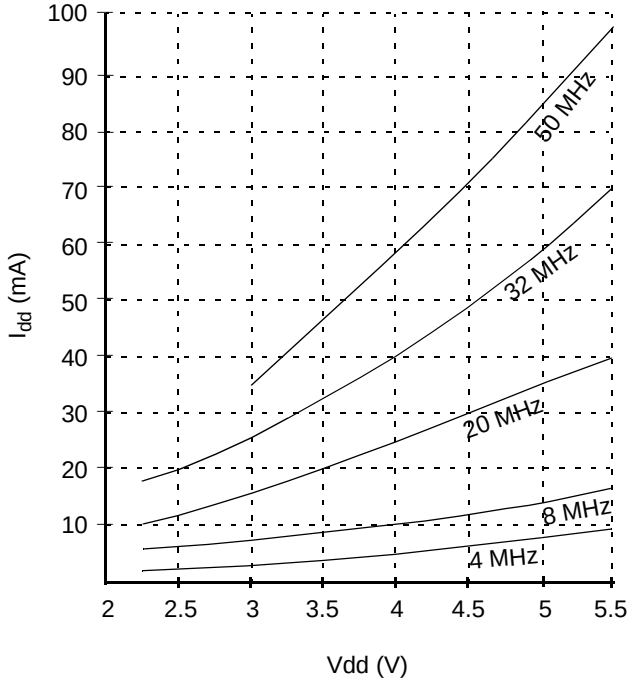
Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	0V < Vin < Vdd		+/- 10	+/- 25	mV
Input Common Mode Voltage Range		0		Vdd	V
Voltage Gain			300k		V/V
Response Time	$V_{overdrive}$ = 25 mV			250	ns

17.5 Typical Performance Characteristics (25°C)

Active Supply Current Idd Vs Operating Frequency (Crystal Clock)

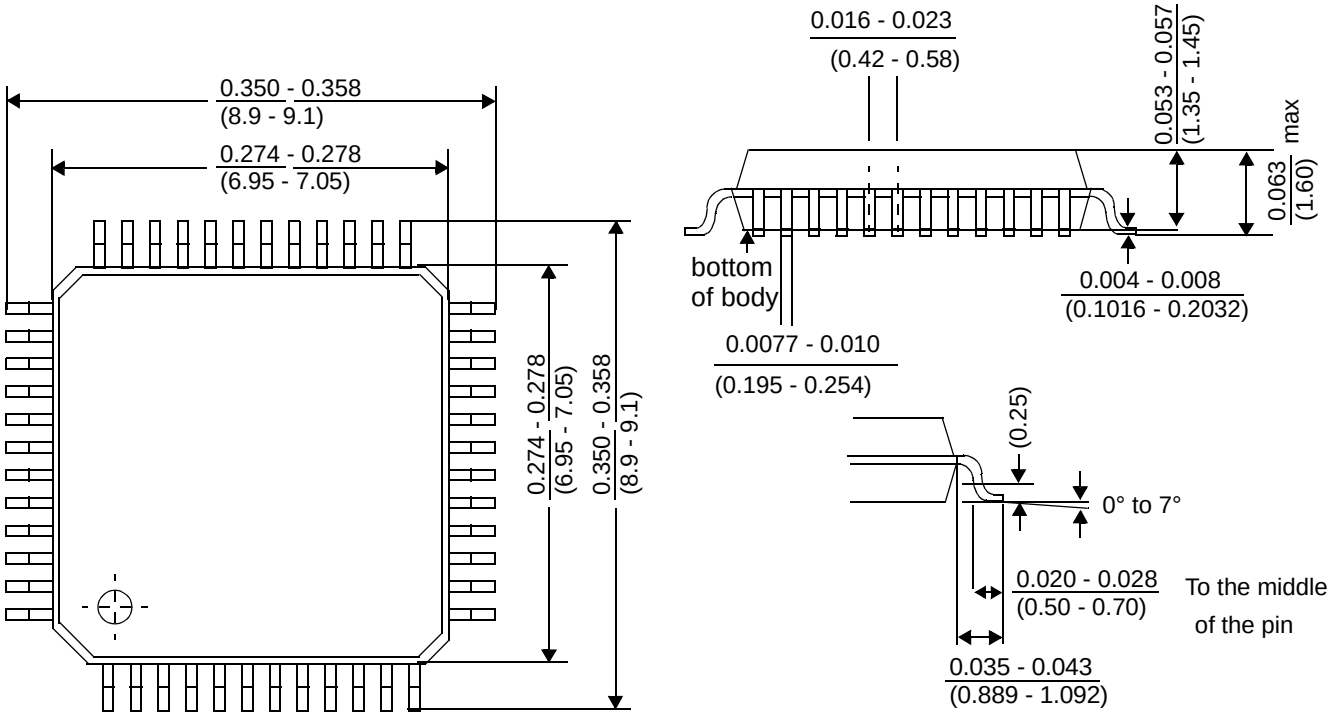


Active Idd Vs Vdd (Crystal Clock)



18.0 PACKAGE DIMENSIONS [DIMENSIONS ARE IN INCHES/(MILLIMETERS)]

SX48BD/TQ: 7x7x1.4 mm body, 0.5 mm pitch, 9 mm tip to tip, JEDEC #MO-136



SX52BD/PQ: 10x10x2.0 mm body, 0.65 mm pitch, 13.2 mm tip to tip, JEDEC #MO-108 (AC-2)