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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc18s37jet100e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_5	R5	J4	48	65	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**SD_POW —** SD/MMC card power monitor output.
P1_6	T4	K4	49	67	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCTimer/PWM input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**EMC_WE —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							O	**EMC_BLS0 —** LOW active Byte Lane select signal 0.
							-	**R —** Function reserved.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	G4	50	69	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCTimer/PWM output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_16	M7	H9	64	90	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							O	**T0_MAT0 —** Match output 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D9 —** External memory data line 9.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	H10	66	93	[3]	N; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
							-	**R —** Function reserved.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							I	**T0_CAP3 —** Capture input 3 of timer 0.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_18	N12	J10	67	95	[2]	N; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
							-	**R —** Function reserved.
							O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
							O	**T0_MAT3 —** Match output 3 of timer 0.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_D10 —** External memory data line 10.
P1_19	M11	K9	68	96	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I^2S receive master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P2_8	J16	C6	98	140	[2]	N; PU	-	**R —** Function reserved. External boot pin (see Table 5)
							O	**CTOUT_0 —** SCTimer/PWM output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_9	H16	B10	102	144	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. External boot pin (see Table 5).
							O	**CTOUT_3 —** SCTimer/PWM output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	E8	104	146	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCTimer/PWM output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	A9	105	148	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCTimer/PWM output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P3_1	G11	F7	114	163	[2]	N; PU	I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I	**CAN0_RD —** CAN receiver input.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							I/O	**GPIO5[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD15 —** LCD data.
							-	**R —** Function reserved.
P3_2	F11	G6	116	166	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I²S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I²S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	A7	118	169	[4]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I²S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PA_4	G13	-	-	151	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_9 —** SCTimer/PWM output 9. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A23 —** External memory address line 23.
							I/O	**GPIO5[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_0	B15	-	-	164	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_10 —** SCTimer/PWM output 10. Match output 3 of timer 3.
							O	**LCD_VD23 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_1	A14	-	-	175	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULP data line direction.
							O	**LCD_VD22 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[21] —** General purpose digital input/output pin.
							O	**CTOUT_6 —** SCTimer/PWM output 6. Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_2	B12	-	-	177	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							O	**LCD_VD21 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[22] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCTimer/PWM output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
PC_3	F5	-	-	11	[5]	N; PU	I/O	**USB1_ULPI_D5 —** ULPI link bidirectional data line 5.
							-	**R —** Function reserved.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**GPIO6[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**SD_VOLT1 —** SD/MMC bus voltage select output 1.
							AI	**ADC1_0 —** ADC1 and ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_4	F4	-	-	16	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**GPIO6[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							I/O	**SD_DAT0 —** SD/MMC data bus line 0.
PC_5	G4	-	-	20	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							-	**R —** Function reserved.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**GPIO6[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							I/O	**SD_DAT1 —** SD/MMC data bus line 1.
PC_6	H6	-	-	22	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							I/O	**GPIO6[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
Debug pins								
DBGEN	L4	A6	28	41	[2]	I	I	JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways: • Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor. • Tie DBGEN to VDDIO. • Pull DBGEN up to VDDIO with an external pull-up resistor.
TCK/SWDCLK	J5	H2	27	38	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$	M4	B4	29	42	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	C4	30	44	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	H3	31	46	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	G3	26	35	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins								
USB0_DP	F2	E1	18	26	[6]	-	I/O	USB0 bidirectional D+ line. Do not add an external series resistor.
USB0_DM	G2	E2	20	28	[6]	-	I/O	USB0 bidirectional D− line. Do not add an external series resistor.
USB0_VBUS	F1	E3	21	29	[6] [7]	-	I	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 70 kΩ (typical) ± 30 kΩ.
USB0_ID	H2	F1	22	30	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For use with OTG, this pin has an internal pull-up resistor.
USB0_RREF	H1	F3	24	32	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins								
USB1_DP	F12	E9	89	129	[9]	-	I/O	USB1 bidirectional D+ line. Add an external series resistor of 33 Ω +/- 2 %.
USB1_DM	G12	E10	90	130	[9]	-	I/O	USB1 bidirectional D− line. Add an external series resistor of 33 Ω +/- 2 %.
I^2C-bus pins								
I2C0_SCL	L15	D6	92	132	[10]	I; F	I/O	I^2C clock input/output. Open-drain output (for I^2C-bus compliance).
I2C0_SDA	L16	E6	93	133	[10]	I; F	I/O	I^2C data input/output. Open-drain output (for I^2C-bus compliance).
Reset and wake-up pins								
$\overline{\text{RESET}}$	D9	B6	128	185	[11]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up.

Table 4. Boot mode when OTP BOOT_SRC bits are programmed

Boot mode	BOOT_SRC bit 3	BOOT_SRC bit 2	BOOT_SRC bit 1	BOOT_SRC bit 0	Description
USB0	0	1	1	0	Boot from USB0.
USB1	0	1	1	1	Boot from USB1.
SPI (SSP)	1	0	0	0	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	1	0	0	1	Enter ISP mode using USART3 functions on pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USART0	LOW	LOW	LOW	LOW	Enter ISP mode using USART0 pins P2_0 and P2_1.
SPIFI	LOW	LOW	LOW	HIGH	Boot from Quad SPI flash connected to the SPIFI interface on P3_3 to P3_8[1].
EMC 8-bit	LOW	LOW	HIGH	LOW	Boot from external static memory (such as NOR flash) using CS0 and an 8-bit data bus.
EMC 16-bit	LOW	LOW	HIGH	HIGH	Boot from external static memory (such as NOR flash) using CS0 and a 16-bit data bus.
EMC 32-bit	LOW	HIGH	LOW	LOW	Boot from external static memory (such as NOR flash) using CS0 and a 32-bit data bus.
USB0	LOW	HIGH	LOW	HIGH	Boot from USB0
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1].
USART3	HIGH	LOW	LOW	LOW	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

7.18.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.18.2 Digital-to-Analog Converter (DAC)

7.18.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.19 Peripherals in the RTC power domain

7.19.1 RTC

The Real-Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.19.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Alarm interrupt can be generated for a specific date/time.

7.19.2 Event monitor/recorder

The event monitor/recorder allows recording and creating a time stamp of events related to the WAKEUP pins. Sensors report changes to the state of the WAKEUP pins, and the

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See Table 5.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.21 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage			2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	all peripherals disabled					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-	-	0.1	µA
I_{BAT}	battery supply current	Deep power-down mode; RTC running; $V_{DD(REG)(3V3)}$ floating; V_{BAT} = 3.3 V		-	3.0	-	µA
		$V_{DD(REG)(3V3)}$ = V_{BAT} = 3.3 V		-	1.5	-	µA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	< 0.1	-	µA
		power-down mode		-	< 0.1	-	µA
		deep power-down mode		-	< 0.1	-	µA
I_{DDA}	Analog supply current	on pin VDDA; deep sleep mode	[9]	-	0.4	-	µA
		power-down mode	[9]	-	0.4	-	µA
		deep power-down mode	[9]	-	0.007	-	µA
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage		[8]	$0.8 \times (V_{ps} - 0.35)$	-	5.5	V
V_{IL}	LOW-level input voltage		[8]	0	-	$0.3 \times (V_{ps} - 0.1)$	V
V_{hys}	hysteresis voltage		[8]	$0.05 \times (V_{ps} - 0.35)$	-	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.5	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	40	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.4$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			0	-	$0.3 \times V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA		$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−6	-	-	mA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[18]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V. Special conditions for $V_{DD(REG)(3V3)}$ apply when writing to the flash and EEPROM. See Table 16 and Table 15.

[3] Pin VPP should either be not connected (when OTP does not need to be programmed) or tied to pins VDDIO and VDDREG to ensure the same ramp-up time for both supply voltages.

[4] $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V; T_{amb} = 25 °C.

[5] PLL1 disabled; IRC running; CCLK = 12 MHz.

[6] V_{BAT} = 3.6 V.

[7] T_{amb} = -40 °C to +105 °C; $V_{DD(IO)} = V_{DDA}$ = 3.6 V; over entire frequency range CCLK = 12 MHz to 180 MHz; in active mode, sleep mode; deep-sleep mode, power-down mode, and deep power-down mode.

[8] V_{ps} corresponds to the output of the power switch (see Figure 9) which is determined by the greater of V_{BAT} and $V_{DD(Reg)(3V3)}$.

[9] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] To V_{SS}.

[12] The values specified are simulated and absolute values.

[13] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

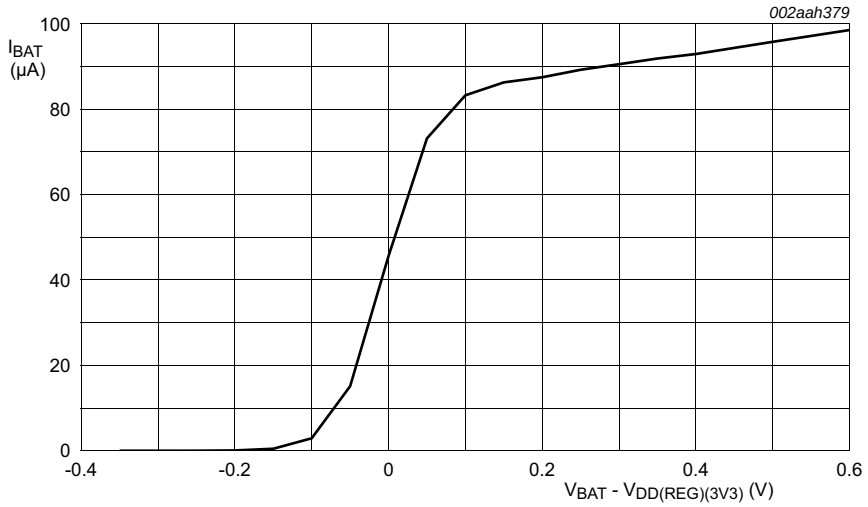
[14] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

[15] The parameter value specified is a simulated value excluding bond capacitance.

[16] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[17] $V_{DD(IO)}$ present.

[18] Includes external resistors of 33 Ω ± 1 % on D+ and D−.



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 2.6 V to 3.6 V; CCLK = 12 MHz.

Remark: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V.

Fig 18. Typical battery supply current in Active mode

10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 12. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
I2C1	CLK_APB3_I2C1	0.01	0.01
I2C0	CLK_APB1_I2C0	< 0.01	0.02
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.07	0.07
ADC1	CLK_APB3_ADC1	0.07	0.07
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.16	0.15
MOTOCON	CLK_APB1_MOTOCON	0.04	0.04
I2S	CLK_APB1_I2S	0.09	0.08
SPIFI	CLK_SPIFI, CLK_M3_SPIFI	1.14	2.29
GPIO	CLK_M3_GPIO	0.72	1.43

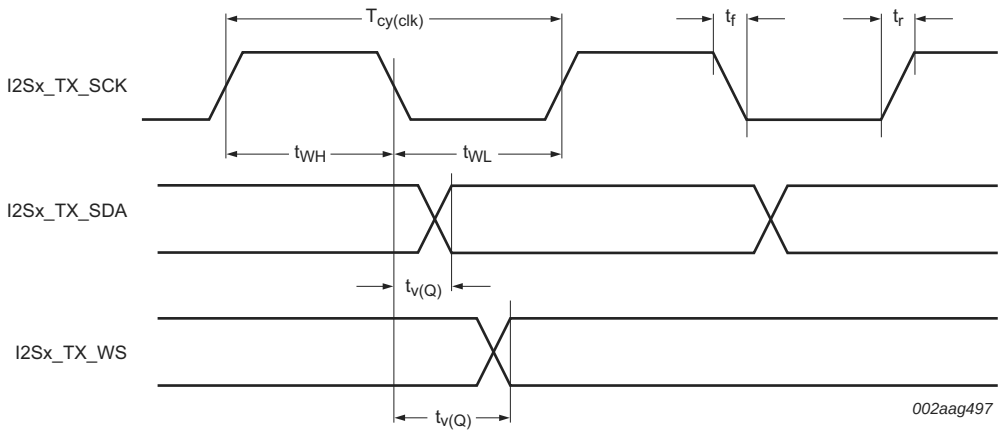


Fig 27. I²S-bus timing (transmit)

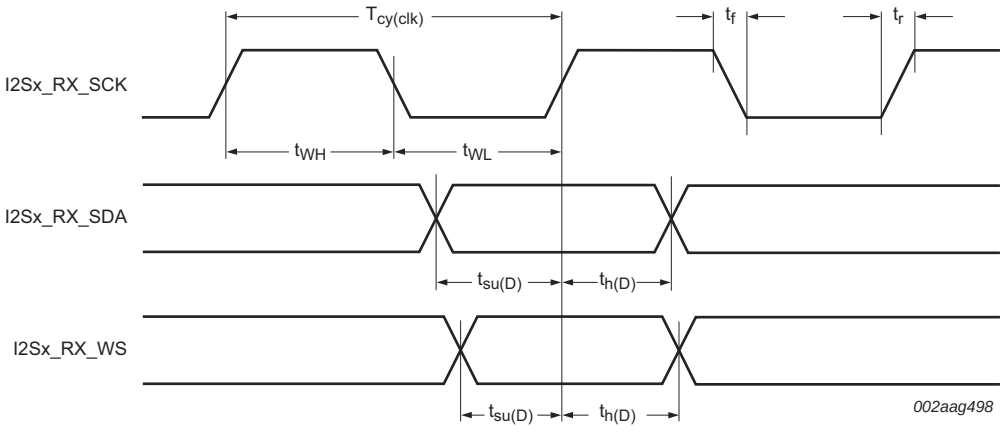


Fig 28. I²S-bus timing (receive)

11.11 USART interface

Table 26. USART dynamic characteristics

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
USART master (in synchronous mode)				
$t_{su(D)}$	data input set-up time	26.6	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	0	10.4	ns
USART slave (in synchronous mode)				
$t_{su(D)}$	data input set-up time	2.4	-	ns
$t_{h(D)}$	data input hold time	0	-	ns
$t_{v(Q)}$	data output valid time	4.3	24.3	ns

11.12 SSP interface

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		12.2	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.6	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.7	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.7	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		microwire frame format		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

11.14 USB interface

Table 31. Dynamic characteristics: USB0 and USB1 pins (full-speed)
C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(IO)}$, unless otherwise specified; 3.0 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 35		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 35		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 35	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 35	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

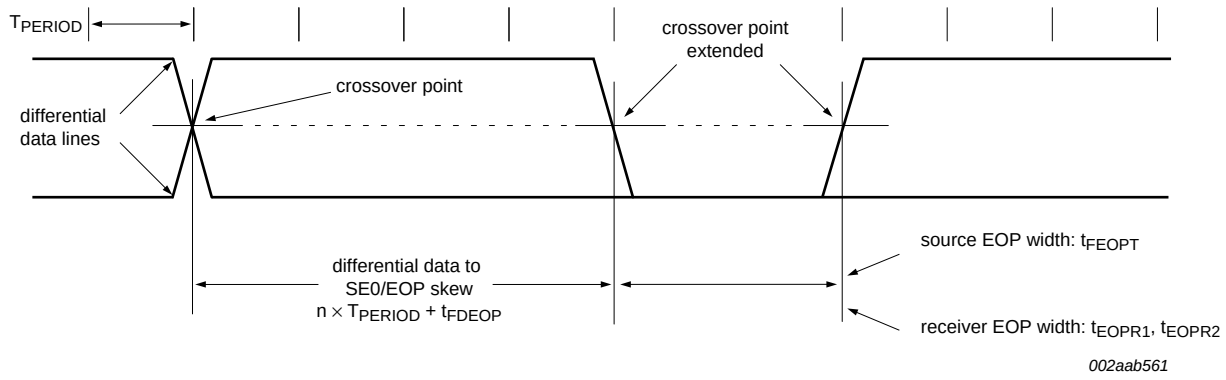


Fig 35. Differential data-to-EOP transition skew and EOP width

Table 40. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 41. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function	LPC18xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4		BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3		BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2		BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1		BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0		BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity		BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

Table 42. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 43. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

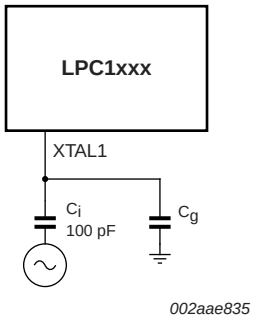


Fig 41. Slave mode operation of the on-chip oscillator

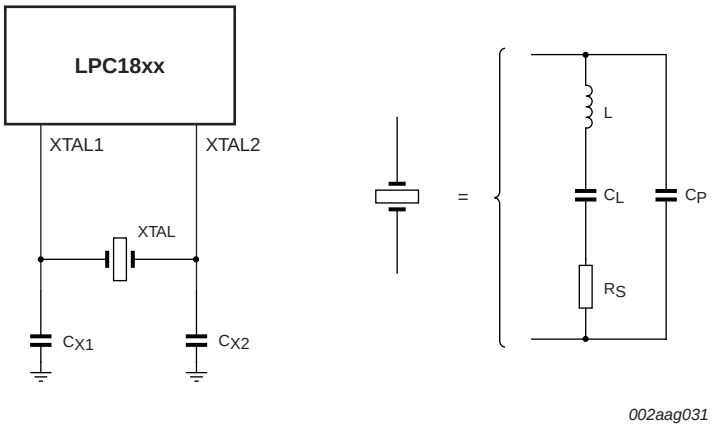


Fig 42. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

18. Revision history

Table 45. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC18S5X_S3Xv.1.2	20160309	Product data sheet	-	LPC18S5X_S3Xv.1.1
Modifications:	• Updated Table 29 “Dynamic characteristics: Dynamic external memory interface”: Read cycle parameters $t_{h(D)}$ min value is 2.2 ns and max value is “-”.			
LPC18S5X_S3Xv.1.1	20151116	Product data sheet	2015110041	LPC18S5X_S3Xv.1.0
Modifications:	• Updated Table 2 “Ordering options”: TFBGA100 package does not support ULPI interface. • Updated USART timing figure. See Figure 29 “USART timing”. • Updated SSP slave and SSP master values in Table 27 “Dynamic characteristics: SSP pins in SPI mode”. Updated footnote 2 to: $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$. – removed $t_{v(Q)}$, data output valid time in SPI mode, minimum value of 3 ´ (1/PCLK) from SSP slave mode. – added units to t_d, delay time, for SSP slave and master mode. • Added GPCLKIN section and table. See Section 11.7 “GPCLKIN” and Table 22 “Dynamic characteristic: GPCLKIN”.			
LPC18S5X_S3Xv.1.0	20150212	Product data sheet	-	-