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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	20
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-TQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq613a-0000

MAXQ613

16-Bit Microcontroller with Infrared Module

ABSOLUTE MAXIMUM RATINGS

Voltage Range on VDD with Respect to GND	-0.3V to +3.6V	44 TQFN (single-layer board)	
Voltage Range on Any Lead with		(derate 27mW/°C above +70°C).....	2162.2mW
Respect to GND Except VDD	-0.3V to (VDD + 0.5V)	44 TQFN (multilayer board)	
Continuous Power Dissipation (TA = +70°C)		(derate 37mW/°C above +70°C).....	2963mW
32 TQFN (single-layer board)		Operating Temperature Range.....	0°C to +70°C
(derate 21.3mW/°C above +70°C).....	1702.1mW	Storage Temperature Range.....	-65°C to +150°C
32 TQFN (multilayer board)		Lead Temperature (excluding dice; soldering, 10s)	+300°C
(derate 34.5mW/°C above +70°C).....	2758.6mW	Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(VDD = VRST to 3.6V, TA = 0°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VDD		VRST		3.6	V
1.8V Internal Regulator	VREG18		1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	VPFW	Monitors VDD (Note 2)	1.75	1.8	1.85	V
Power-Fail Reset Voltage	VRST	Monitors VDD (Note 3)	1.64	1.67	1.70	V
POR Voltage	VPOR	Monitors VDD	1		1.42	V
RAM Data-Retention Voltage	VDRV	(Note 4)	1.0			V
Active Current	IDD_1	Sysclk = 12MHz (Note 5)		3.25	4	mA
Stop-Mode Current	IS1	Power-Fail Off	TA = +25°C	0.2	2.0	µA
			TA = 0°C to +70°C	0.2	8	
	IS2	Power-Fail On	TA = +25°C	22	29.5	
			TA = 0°C to +70°C	27.6	42	
Current Consumption During Power-Fail	IPFR	(Note 6)	$[(3 \times IS2) + ((PCI - 3) \times (IS1 + INANO))]/PCI$			µA
Power Consumption During POR	IPOR	(Note 7)	100			nA
Stop-Mode Resume Time	tON		$375 + (8192 \times t_{HFXIN})$			µs
Power-Fail Monitor Startup Time	tPFM_ON	(Note 4)	150			µs
Power-Fail Warning Detection Time	tPFW	(Note 8)	10			µs
Input Low Voltage for IRTX, IRRX, RESET, and All Port Pins	VIL		VGND	0.3 x VDD		V
Input High Voltage for IRTX, IRRX, RESET, and All Port Pins	VIH		0.7 x VDD		VDD	V

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RECOMMENDED OPERATING CONDITIONS (continued)

(VDD = VRST to 3.6V, TA = 0°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WAKE-UP TIMER						
Wake-Up Timer Interval	tWAKEUP		1/fNANO		65,535/ fNANO	s
FLASH MEMORY						
System Clock During Flash Programming/Erase	fFPSYCLK		6			MHz
Flash Erase Time	tME	Mass erase	20		40	ms
	tERASE	Page erase	20		40	
Flash Programming Time per Word	tPROG	(Note 10)	20		100	μs
Write/Erase Cycles			20,000			Cycles
Data Retention		TA = +25°C	100			Years
IR						
Carrier Frequency	fIR	(Note 4)			fCK/2	Hz

SPI ELECTRICAL CHARACTERISTICS

(VDD = VRST to 3.6V, TA = 0°C to +70°C, unless otherwise noted.) (Note 11)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Master Operating Frequency	1/tMCK				fCK/2	MHz
SPI Slave Operating Frequency	1/tSCK				fCK/4	MHz
SPI I/O Rise/Fall Time	tSPI_RF	CL = 15pF, pullup = 560Ω	8.3		23.6	ns
SCLK Output Pulse-Width High/Low	tMCH, tMCL		tMCK/2 - tSPI_RF			ns
MOSI Output Hold Time After SCLK Sample Edge	tMOH		tMCK/2 - tSPI_RF			ns
MOSI Output Valid to Sample Edge	tMOV		tMCK/2 - tSPI_RF			ns
MISO Input Valid to SCLK Sample Edge Rise/Fall Setup	tMIS		25			ns
MISO Input to SCLK Sample Edge Rise/Fall Hold	tMIH		0			ns
SCLK Inactive to MOSI Inactive	tMLH		tMCK/2 - tSPI_RF			ns
SCLK Input Pulse-Width High/Low	tSCH, tSCL			tSCK/2		ns
$\overline{\text{SSEL}}$ Active to First Shift Edge	tSSE		tSPI_RF			ns
MOSI Input to SCLK Sample Edge Rise/Fall Setup	tSIS		tSPI_RF			ns

16-Bit Microcontroller with Infrared Module**SPI ELECTRICAL CHARACTERISTICS (continued)**(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C, unless otherwise noted.) (Note 11)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MOSI Input from SCLK Sample Edge Transition Hold	t _{SIH}		t _{SPI_RF}			ns
MISO Output Valid After SCLK Shift Edge Transition	t _{SOV}				2t _{SPI_RF}	ns
$\overline{\text{SSEL}}$ Inactive	t _{SSH}		t _{CK} + t _{SPI_RF}			ns
SCLK Inactive to $\overline{\text{SSEL}}$ Rising	t _{SD}		t _{SPI_RF}			ns
MISO Output Disabled After $\overline{\text{SSEL}}$ Edge Rise	t _{SLH}				2t _{CK} + 2t _{SPI_RF}	ns

Note 1: Specifications to 0°C are guaranteed by design and are not production tested. Typical = +25°C, V_{DD} = +3.3V, unless otherwise noted.

Note 2: V_{PFW} can be programmed to the following nominal voltage trip points: 1.8V, 1.9V, 2.55V, and 2.75V ±3%. The values listed in the *Recommended Operating Conditions* table are for the default configuration of 1.8V nominal.

Note 3: The power-fail reset and POR detectors are designed to operate in tandem to ensure that one or both of these signals is active at all times when V_{DD} < V_{RST}, ensuring the device maintains the reset state until minimum operating voltage is achieved.

Note 4: Guaranteed by design and not production tested.

Note 5: Measured on the V_{DD} pin and the device not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current. The device is executing code from flash memory.

Note 6: The power-check interval (PCI) can be set to always on, or to 1024, 2048, or 4096 nanopower ring clock cycles.

Note 7: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

Note 8: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected; refer to the *MAXQ610 User's Guide* for details.

Note 9: The maximum total current, I_{OH}(MAX) and I_{OL}(MAX), for all listed outputs combined should not exceed 32mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

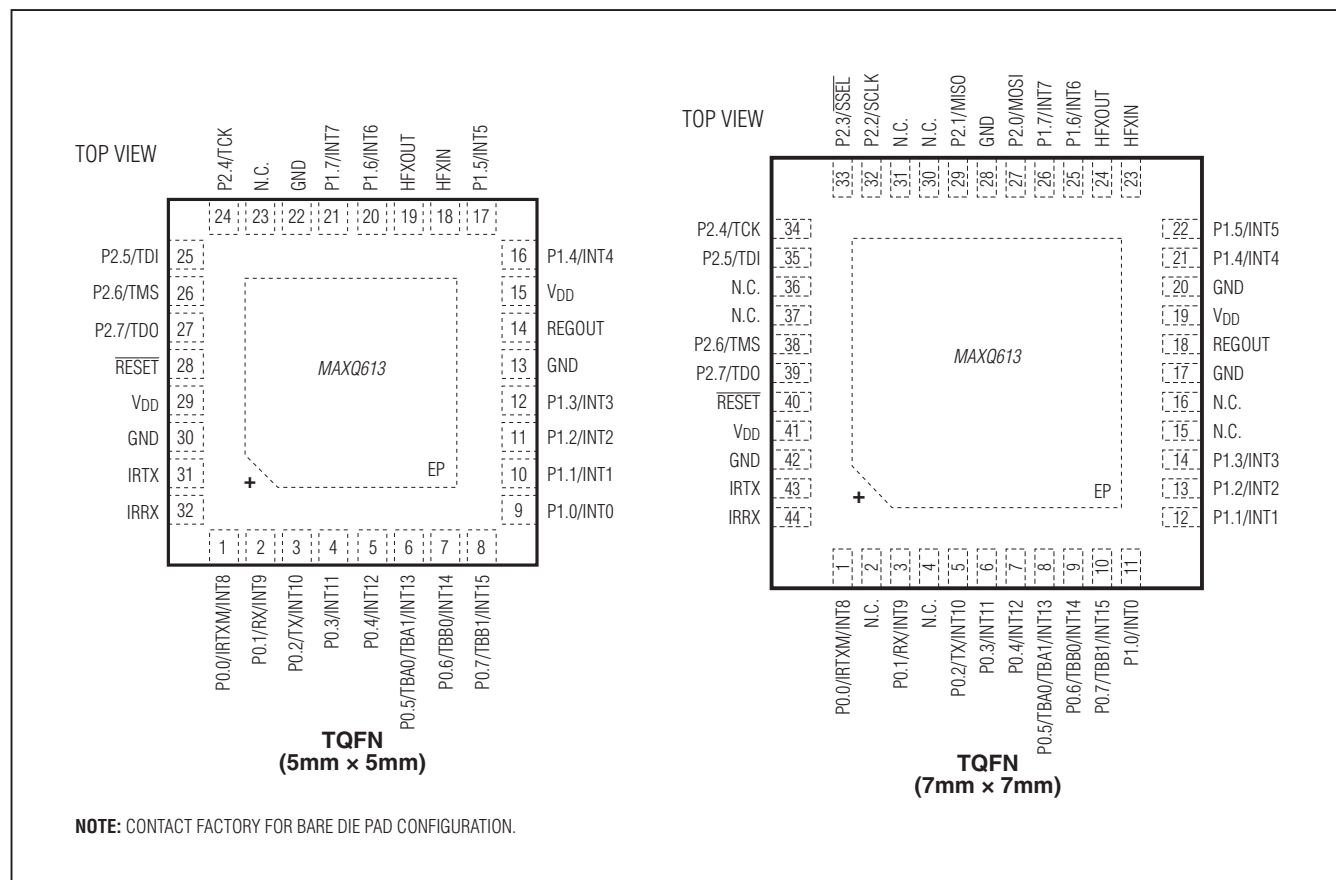
Note 10: Programming time does not include overhead associated with utility ROM interface.

Note 11: AC electrical specifications are guaranteed by design and are not production tested.

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Pin Configurations



Pin Description

PIN			NAME	FUNCTION
BARE DIE	32 TQFN-EP	44 TQFN-EP		
POWER PINS				
15, 36	15, 29	19, 41	VDD	Supply Voltage
13, 16, 25, 37	13, 22, 30	17, 20, 28, 42	GND	Ground. Connect directly to the ground plane.
14	14	18	REGOUT	1.8V Regulator Output. This pin must be connected to ground through a 1.0μF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.

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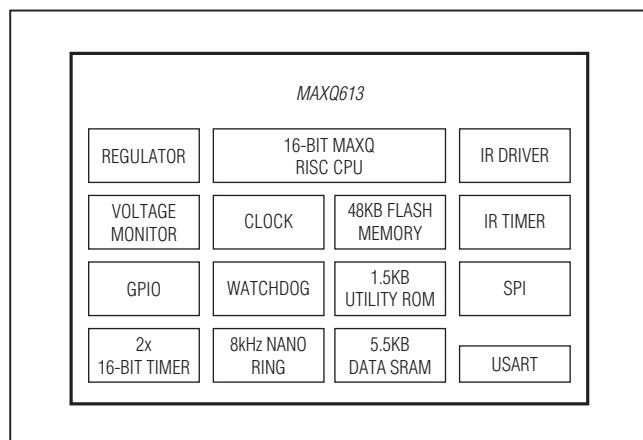
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Pin Description (continued)

PIN			NAME	FUNCTION	
BARE DIE	32 TQFN-EP	44 TQFN-EP			
RESET PIN					
35	28	40	RESET	Digital, Active-Low, Reset Input/Output. The device remains in reset as long as this pin is low and begins executing from the utility ROM at address 8000h when this pin returns to a high state. The pin includes pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin can be left unconnected if there is no need to place the device in a reset state using an external signal. This pin is driven low as an output when an internal reset condition occurs.	
CLOCK PINS					
20	18	23	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT for use as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is unconnected.	
21	19	24	HFXOUT		
IR FUNCTION PINS					
38	31	43	IRTX	IR Transmit Output. IR transmission pin capable of sinking 25mA. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
39	32	44	IRRX	IR Receive Input. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS					
				Port 0 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD0, PO0, and PIO registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All alternate functions must be enabled from software before they can be used.	
				GPIO PORT PIN	
1	1	1	P0.0/IRTXM/INT8	P0.0	IR Modulator Output/INT8
2	2	3	P0.1/RX/INT9	P0.1	USART Receive/INT9
3	3	5	P0.2/TX/INT10	P0.2	USART Transmit/INT10
4	4	6	P0.3/INT11	P0.3	INT11
5	5	7	P0.4/INT12	P0.4	INT12
6	6	8	P0.5/TBA0/TBA1/INT13	P0.5	Type B Timer 0 Pin A or Type B Timer 1 Pin A/INT13

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Block Diagram



Detailed Description

The MAXQ613 provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 48KB of program flash memory; 1.5KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ613 stop-mode current (0.2µA typ) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current IR drive pin capable of sinking up to 25mA current and output pins capable of sinking up to 5mA are ideal for IR applications. It also includes general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the microcontroller's minimum operating voltage.

At the heart of the device is the MAXQ 16-bit, RISC core. Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode

can be invoked from software, resulting in quiescent current consumption of less than 0.2µA (typ) and 2.0µA (max). The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The device is based on Maxim's low-power, 16-bit MAXQ20S family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the device is implemented as a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

16-Bit Microcontroller with Infrared Module**Table 2. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)**

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (μs)
00	Sysclk/2 ¹⁵	2.7ms	42.7
01	Sysclk/2 ¹⁸	21.9ms	42.7
10	Sysclk/2 ²¹	174.7ms	42.7
11	Sysclk/2 ²⁴	1.4s	42.7

different password locks are provided, each of which can be used to protect a different area of memory (system memory, user loader, and user application). Each password lock is controlled by a 16-word area of flash memory; if the password is set to all FFFFh values or all 0000h values, the password is disabled. Otherwise, the password is active and must be matched by the user of the bootloader or debugger before access is granted to the corresponding area of flash program memory. Refer to the *MAXQ610 User's Guide* for more details.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2¹⁵ to 2²⁴ system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 2.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

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IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle

condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR

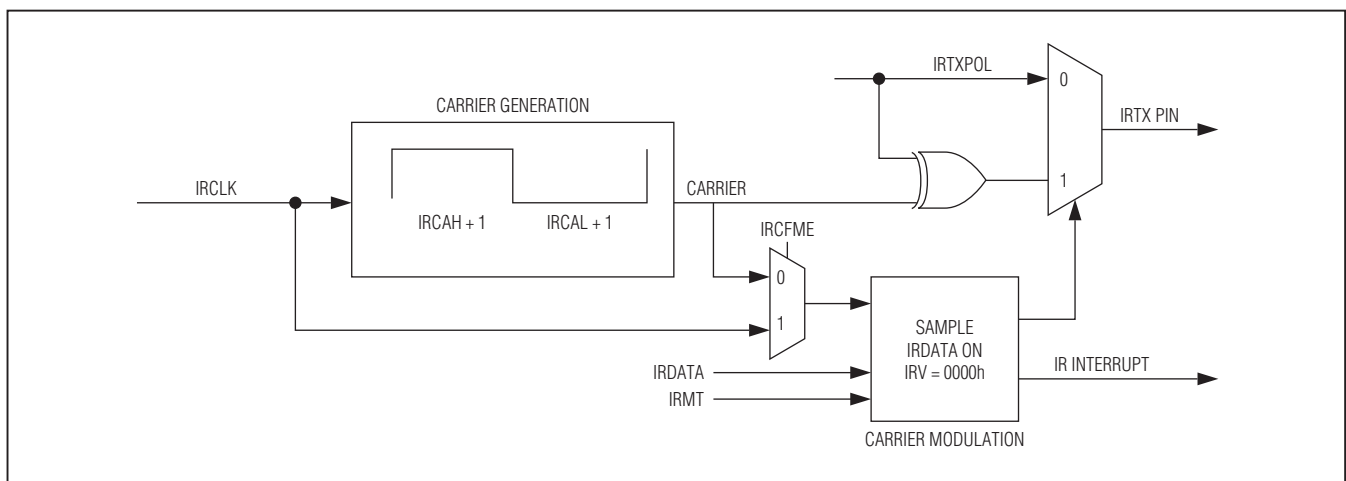


Figure 2. IR Transmit Carrier Generation and Carrier Modulator Control

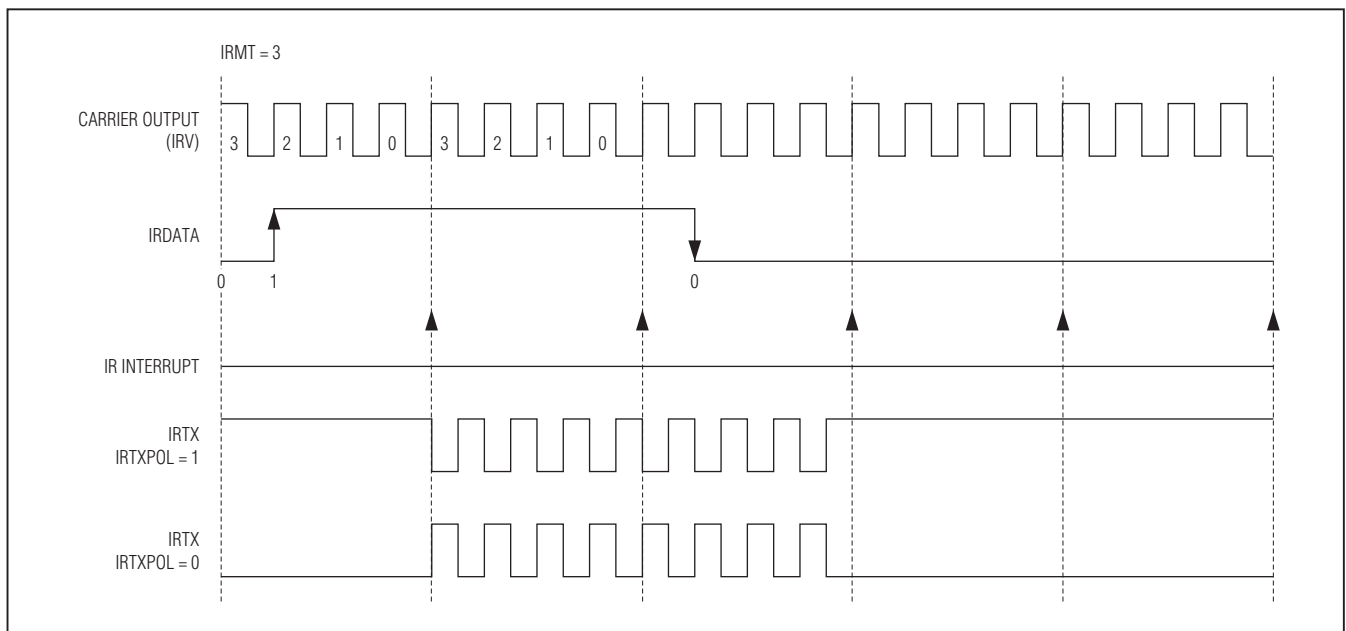


Figure 3. IR Transmission Waveform (IRCFME = 0)

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timer value reloads its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

- 1) Reloads IRV with IRMT.
- 2) Samples IRCA, IRDATA, and IRTXPOL.
- 3) Generates IRTX accordingly.
- 4) Sets IRIF to 1.
- 5) Generates an interrupt to the CPU if enabled (IRIE = 1).

To terminate the current transmission, the user can switch to receive mode (IRMODE = 0) or clear IREN to 0.

Carrier Modulation Time = IRMT + 1 carrier cycles

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. If the IRENV[1:0] bits are configured to 01b or 10b, the modulator/envelope is output to the IRTXM pin. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV down-count interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval down-count boundaries. See Figure 4. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (IRENV[1:0] = 10b) carrier to the IRTX pin.

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function.

The IR module starts operating in the receive mode when IRMODE = 0 and IREN = 1. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) bit can be set to 1 to allow clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV. When IRCFME = 1, the IRCLK clocks the IRV register.

On the next qualified event, the IR module does the following:

- 1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.
- 2) Transfers its current IRV value to the IRMT.
- 3) Resets IRV content to 0000h (if IRXRL = 1).
- 4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt is generated, if

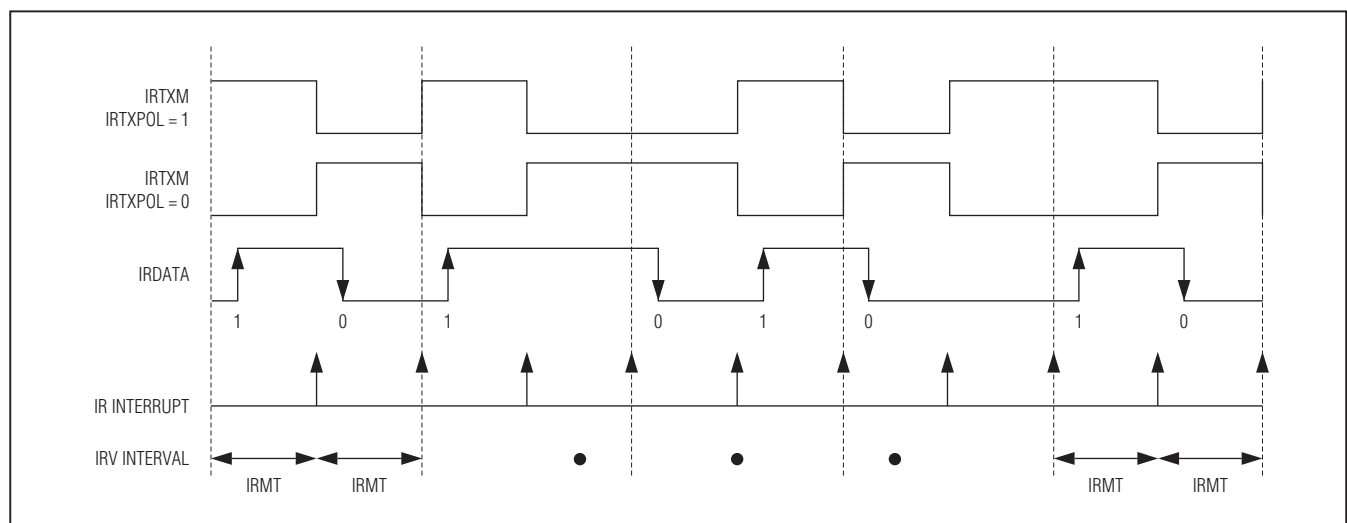


Figure 4. External IRTXM (Modulator) Output

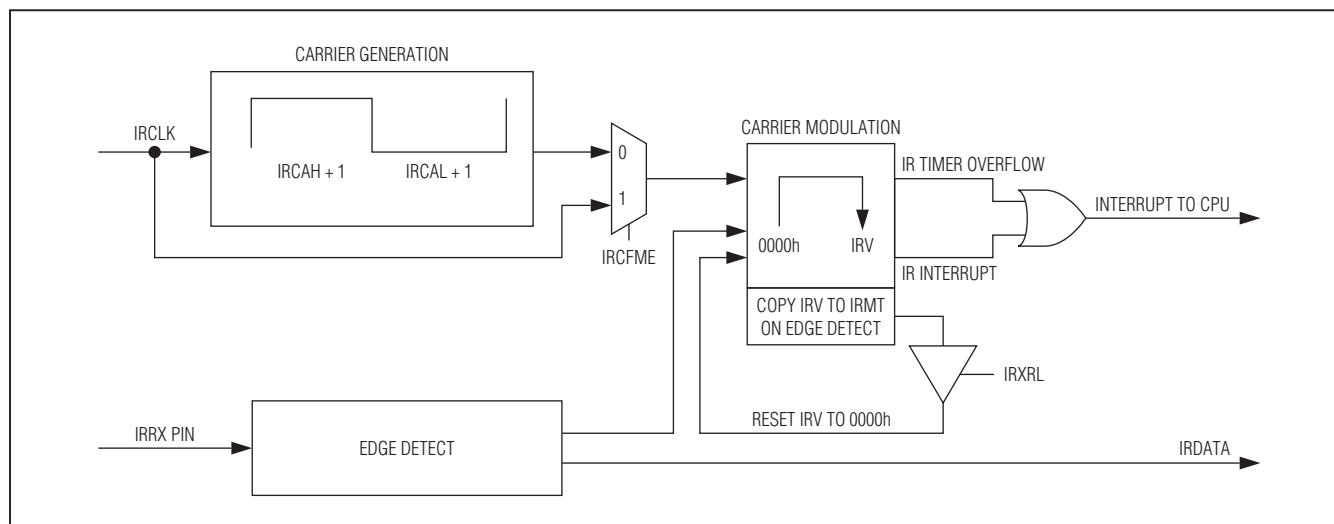


Figure 5. IR Capture

enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode (IRMODE = 1) or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag (normally used to signal a capture when RXBCNT = 0) now becomes set if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. When the RXBCNT bit is changed from 0 to 1, the IRMT register is set to 0001h. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits). Figure 6 and the descriptive sequence embedded

in the figure illustrate the expected usage of the receive burst-count mode.

16-Bit Timers/Counters

The microcontroller provides two timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2^n divider (for $n = 0, 2, 4, 6, 8, 10$)

USART

The device provides a USART peripheral with the following features:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt when transmit or receive data operation completes
- Independent programmable baud-rate generator
- Optional 9th bit parity support
- Start/stop bit support

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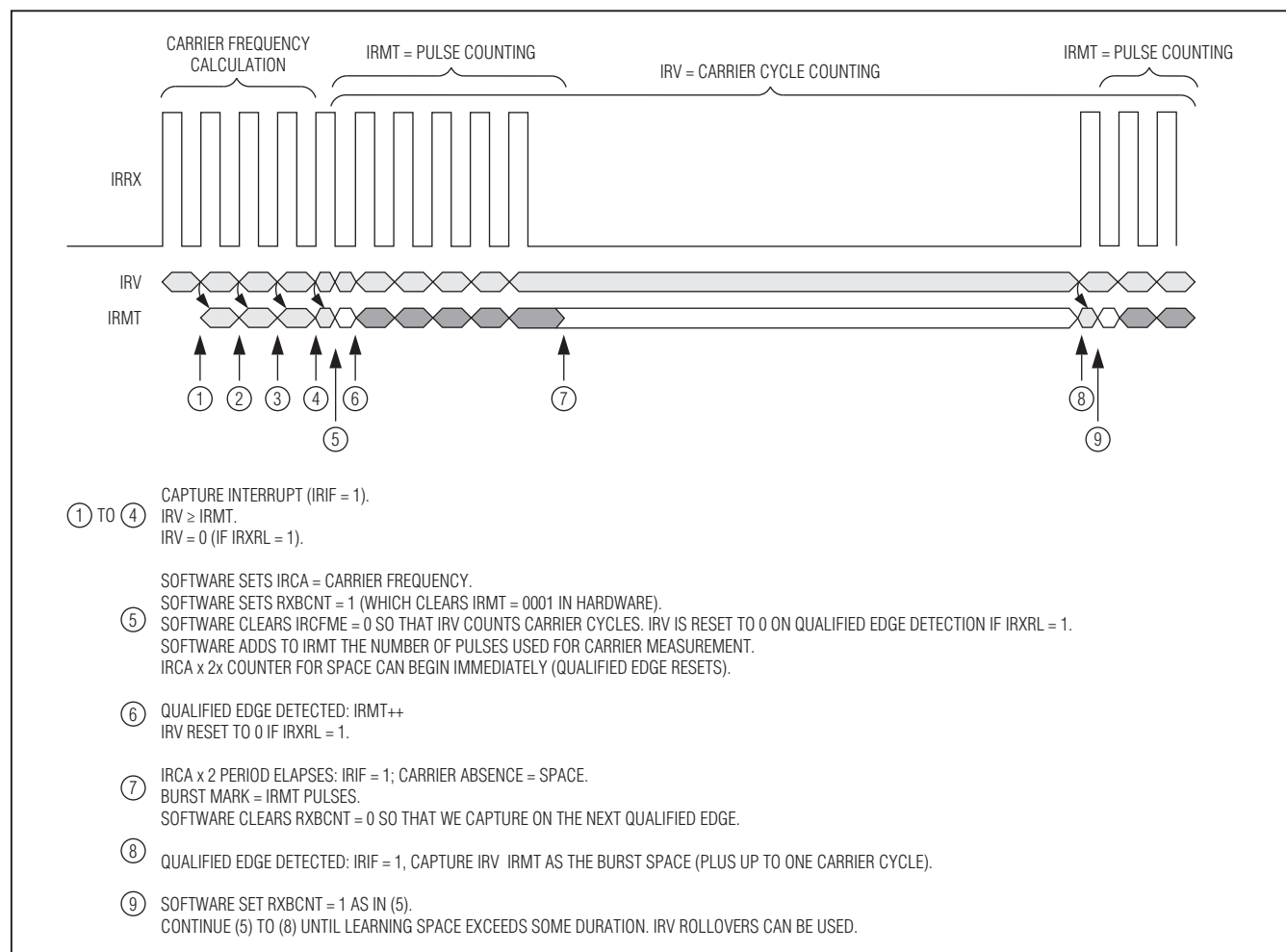


Figure 6. Receive Burst-Count Example

Table 3. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

Serial Peripheral Interface (SPI)

The integrated SPI provides an independent serial communication channel that communicates synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection

is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the device can support up to Sysclk/4 SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of an active \overline{SSEL} state (active low or active high) through the slave active select.

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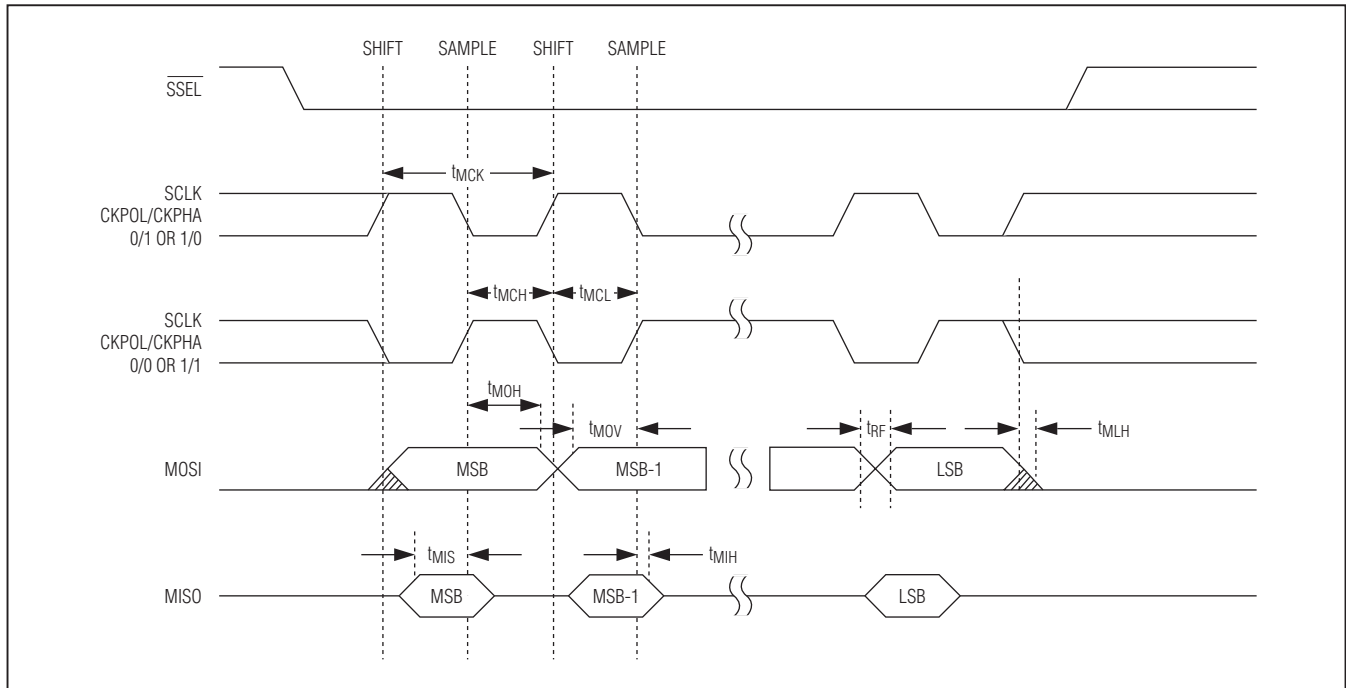


Figure 7. SPI Master Communication Timing

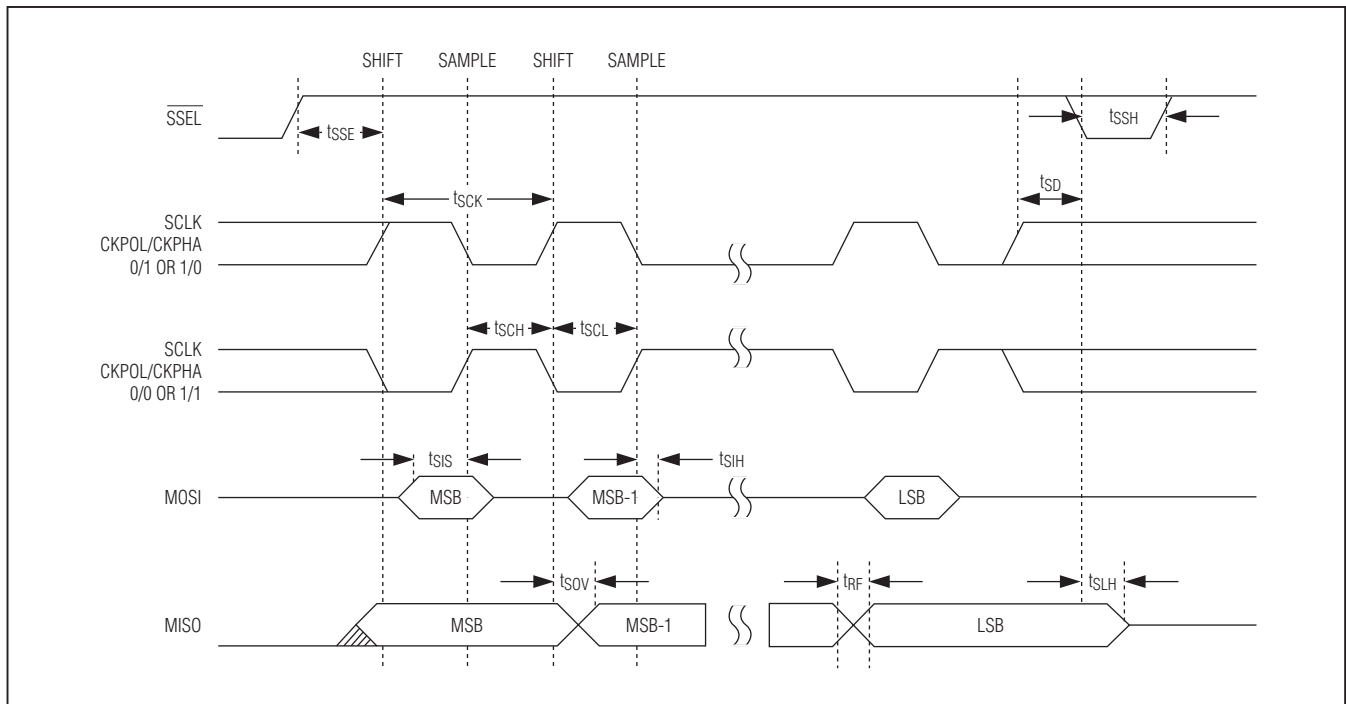


Figure 8. SPI Slave Communication Timing

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General-Purpose I/O

The microcontroller provides port pins for general-purpose I/O that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become high impedance with both weak pullups and input buffers disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the *MAXQ610 User's Guide*.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT, as illustrated in Figure 9.

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors near the oscillator circuitry and connect HFXIN and HFXOUT to ground with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used and should be initially selected based on load capacitance as suggested by the manufacturer.

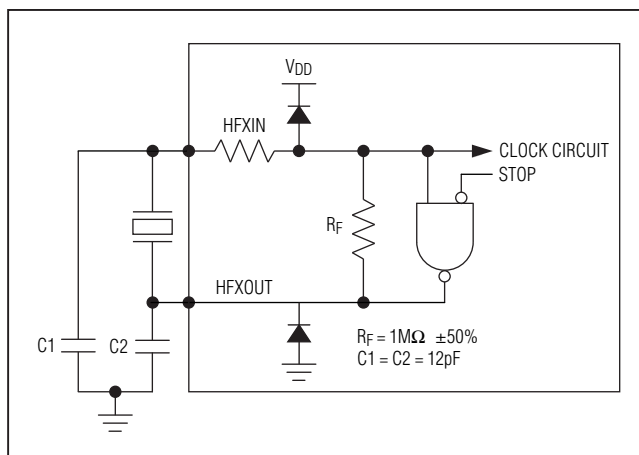


Figure 9. On-Chip Oscillator

ROM Loader

The ROM loader denies access to the system, user loader, or user-application memories unless an area-specific password is provided. The ROM loader is not available in ROM-only versions.

Loading Flash Memory

An internal bootstrap loader allows reloading over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter such as the MAXQJTAG-001, available from Maxim. If in-system programmability is not required, a commercial gang programmer can be used for mass programming. Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to one during reset through the JTAG interface executes the bootstrap-loader mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

In addition, the ROM loader also enforces the memory-protection policies. Passwords that are 16 words are required to access the ROM loader interface.

Loading memory is not possible for ROM-only versions of the device.

In-Application Flash Programming

From user-application code, flash memory can be programmed using the ROM utility functions from either C or assembly language. The function declarations below show examples of some of the ROM utility functions provided for in-application flash memory programming:

```
/* Write one 16-bit word to code address 'dest'.
 * Dest must be aligned to 16 bits.
 * Returns 0 = failure, 1 = OK.
 */
int flash_write (uint16_t dest, uint16_t
data);
```

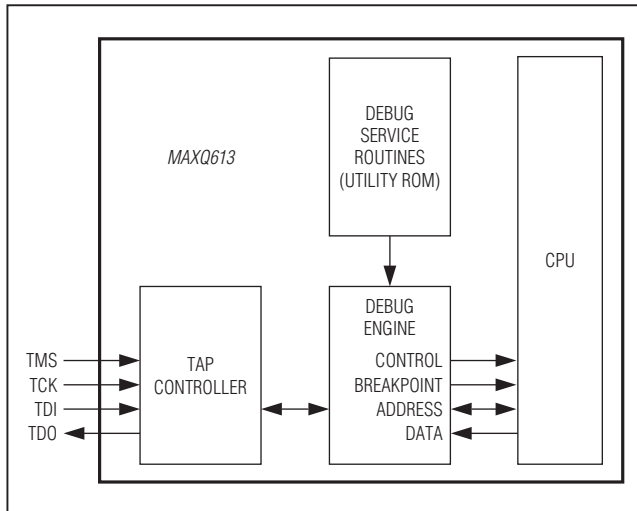
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Figure 10. In-Circuit Debugger

To erase, the following function would be used:

```
/* Erase the given Flash page
 * addr: Flash offset (anywhere within page)
 */
int flash_erasepage(uint16_t addr);
```

The in-application flash memory programming must call ROM utility functions to erase and program any of the flash memory. Memory protection is enforced by the ROM utility functions. In-application is not available in ROM-only versions of the device.

In-Circuit Debug and JTAG Interface

Embedded debug hardware and software are developed and integrated to provide full in-circuit debugging capability in a user-application environment. These hardware and software features include the following:

- Debug engine
- Set of registers providing the ability to set breakpoints on register, code, or data using debug service routines stored in ROM

Collectively, these hardware and software features support two modes of in-circuit debug functionality:

- Background mode:
CPU is executing the normal user program
Allows the host to configure and set up the in-circuit debugger

- Debug mode:

Debugger takes over the control of the CPU

Read/write accesses to internal registers and memory

Single-step of the CPU for trace operation

The interface to the debug engine is the TAP controller. The interface allows for communication with a bus master that can either be automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP that is compatible with the JTAG IEEE Standard 1149. The TAP provides an independent serial channel to communicate synchronously with the host system.

To prevent unauthorized access of the protected memory regions through the JTAG interface, the debug engine prevents modification of the privilege registers and disallows all access to system memory, unless memory protection is disabled. In addition, all services (such as register display or modification) are denied when code is executing inside the system area. The debugger is not available for ROM-only versions of the device.

Operating Modes

The lowest power mode of operation is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, wake-up timer, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the device into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125µs up to approximately 8s.

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $VDD < VRST$ condition does not invoke a reset state.

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Power-Fail Detection

Figures 11, 12, and 13 show the power-fail detection and response during normal and stop-mode operation. If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2¹¹ nanopower ring oscillator clocks (~256ms)
- 2¹² nanopower ring oscillator clocks (~512ms)
- 2¹³ nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two

nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the \overline{RESET} pin being driven low externally or the watchdog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 crystal cycles after the reset source is removed.

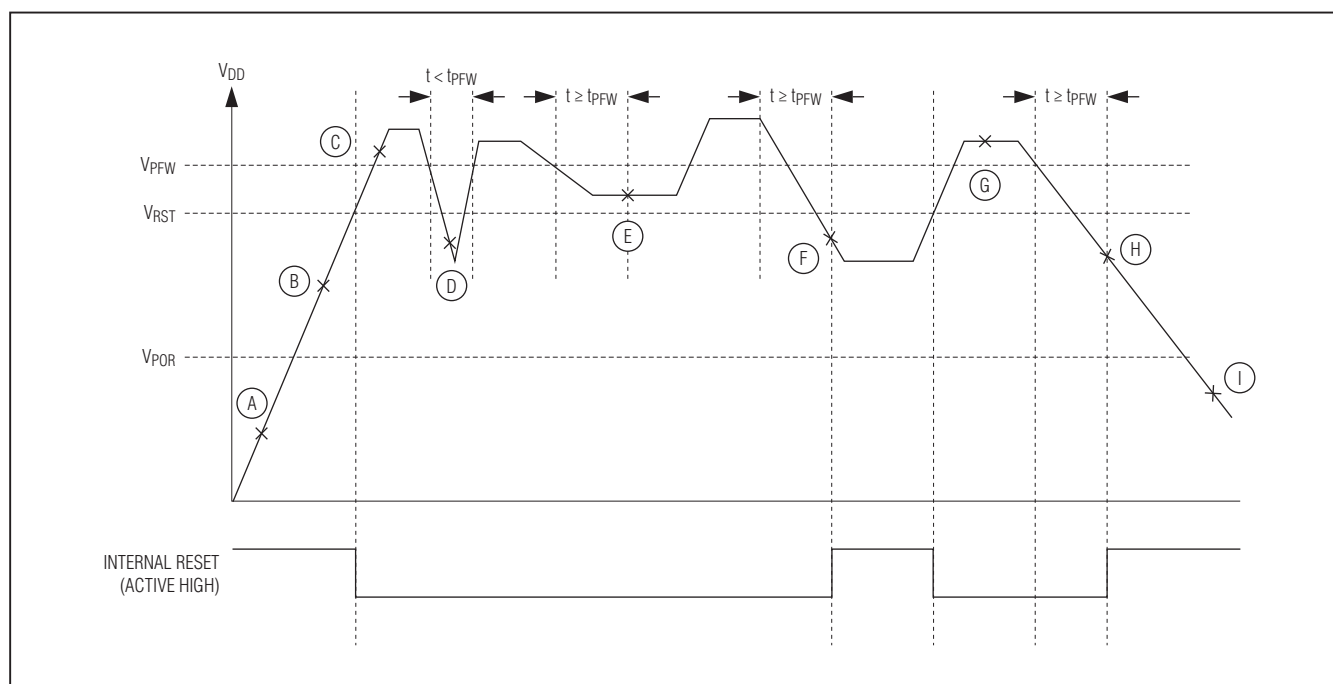


Figure 11. Power-Fail Detection During Normal Operation

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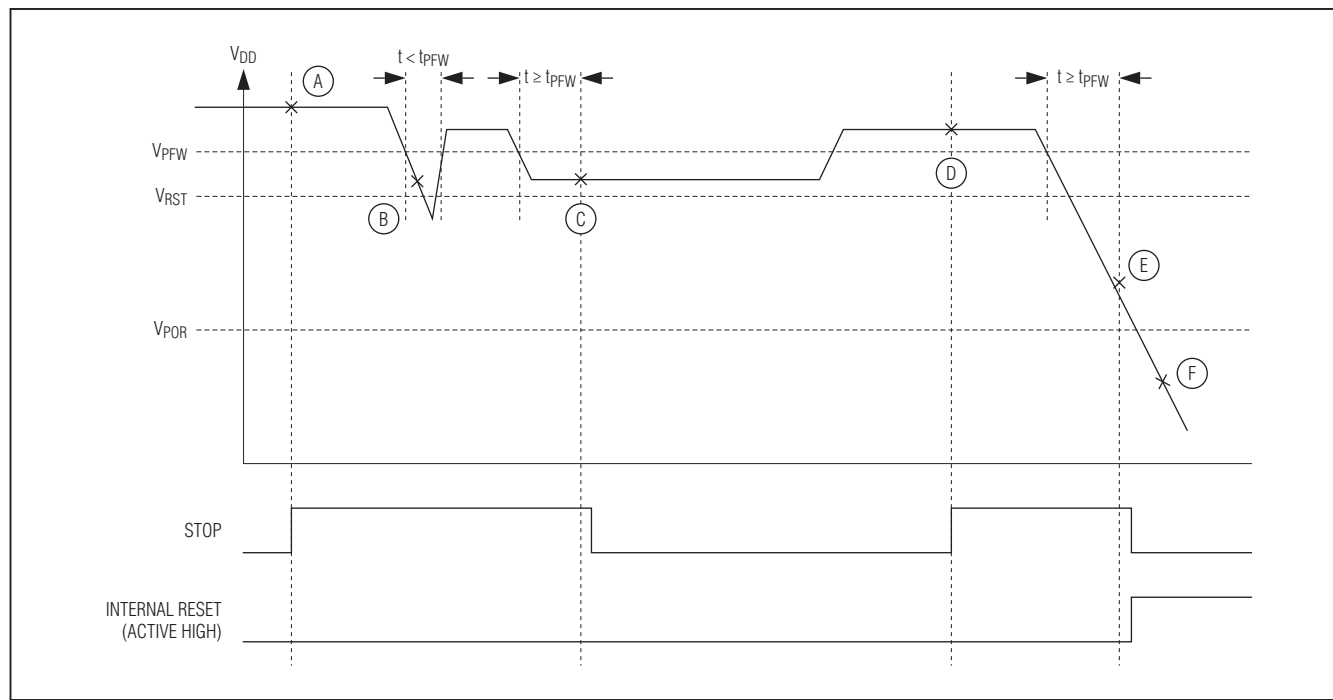


Figure 12. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

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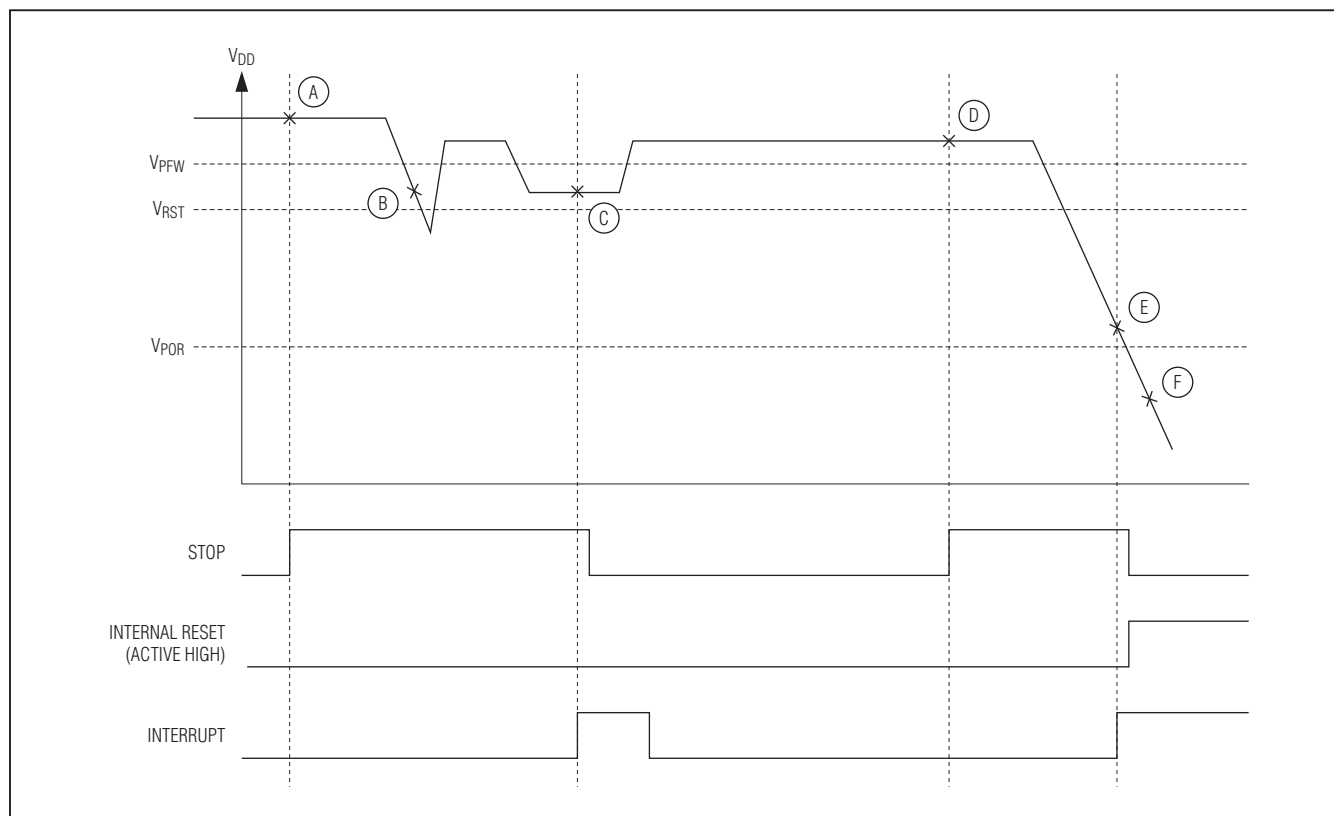


Figure 13. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

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Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, and puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-

purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from www.maximintegrated.com/microcontrollers.

- This MAXQ613 data sheet, which contains electrical/timing specifications, pin descriptions, and package information.
- The MAXQ613 revision-specific errata sheet (www.maximintegrated.com/errata).
- The MAXQ610 User's Guide, which contains detailed information on features and operation, including programming.

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Deviations from the MAXQ610 User's Guide for the MAXQ613

The *MAXQ610 User's Guide* contains all the information that is needed to develop application code for the MAXQ613 microcontroller. However, even though the MAXQ610 and the MAXQ613 are largely code-compatible, there are certain differences between the two devices that must be kept in mind when referring to the *MAXQ610 User's Guide*.

The following registers on the MAXQ610 (which are described in the *MAXQ610 User's Guide*) do not exist on the MAXQ613, and all references to them should be disregarded:

- Port 3 Output Register (PO3)
- Port 3 Direction Register (PD3)
- Port 3 Input Register (PI3)
- Port 4 Output Register (PO4)
- Port 4 Direction Register (PD4)
- Port 4 Input Register (PI4)

Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- Serial-to-JTAG and USB-to-JTAG interface boards for programming and debugging (for microcontrollers with rewritable memory)

A partial list of development tool vendors can be found at www.maximintegrated.com/MAXQ_tools.

For technical support, go to <https://support.maximintegrated.com/micro>.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	21-0140	90-0001
44 TQFN-EP	T4477+2	21-0144	90-0127

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—
1	7/10	Corrected bare die numbers in the <i>Pin Description</i> table for V _{DD} , GND, $\overline{\text{RESET}}$, IRTX, IRRX, P2.5/TDI, P2.6/TMS, and P2.7/TDO	9, 10, 11
2	8/10	Corrected the active mode typ value from 2.0mA to 3.25mA in the <i>Features</i>	1
3	1/11	Removed the LQFP and TQFP packages	1, 4, 8, 9, 10, 27
4	7/12	Removed the ESR reference from the REGOUT description in the <i>Pin Description</i> table; changed the MAXQ core reference to MAXQ20S core in the <i>Microprocessor</i> section; updated the IRDIV bit range from [1:0] to [2:0] in the <i>Carrier Generation Module</i> section	8, 11, 14



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