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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	MAXQ20S
Core Size	16-Bit
Speed	12MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	20
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq613e-0000

MAXQ613

16-Bit Microcontroller with Infrared Module

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on VDD with Respect to GND	-0.3V to +3.6V	44 TQFN (single-layer board)	
Voltage Range on Any Lead with		(derate 27mW/°C above +70°C).....	2162.2mW
Respect to GND Except VDD	-0.3V to (VDD + 0.5V)	44 TQFN (multilayer board)	
Continuous Power Dissipation (TA = +70°C)		(derate 37mW/°C above +70°C).....	2963mW
32 TQFN (single-layer board)		Operating Temperature Range.....	0°C to +70°C
(derate 21.3mW/°C above +70°C).....	1702.1mW	Storage Temperature Range.....	-65°C to +150°C
32 TQFN (multilayer board)		Lead Temperature (excluding dice; soldering, 10s)	+300°C
(derate 34.5mW/°C above +70°C).....	2758.6mW	Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(VDD = VRST to 3.6V, TA = 0°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VDD		VRST		3.6	V
1.8V Internal Regulator	VREG18		1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply	VPFW	Monitors VDD (Note 2)	1.75	1.8	1.85	V
Power-Fail Reset Voltage	VRST	Monitors VDD (Note 3)	1.64	1.67	1.70	V
POR Voltage	VPOR	Monitors VDD	1		1.42	V
RAM Data-Retention Voltage	VDRV	(Note 4)	1.0			V
Active Current	IDD_1	Sysclk = 12MHz (Note 5)		3.25	4	mA
Stop-Mode Current	IS1	Power-Fail Off	TA = +25°C	0.2	2.0	µA
			TA = 0°C to +70°C	0.2	8	
	IS2	Power-Fail On	TA = +25°C	22	29.5	
			TA = 0°C to +70°C	27.6	42	
Current Consumption During Power-Fail	IPFR	(Note 6)	$[(3 \times IS2) + ((PCI - 3) \times (IS1 + INANO))]/PCI$			µA
Power Consumption During POR	IPOR	(Note 7)	100			nA
Stop-Mode Resume Time	tON		$375 + (8192 \times t_{HFXIN})$			µs
Power-Fail Monitor Startup Time	tPFM_ON	(Note 4)	150			µs
Power-Fail Warning Detection Time	tPFW	(Note 8)	10			µs
Input Low Voltage for IRTX, IRRX, RESET, and All Port Pins	VIL		VGND	0.3 x VDD		V
Input High Voltage for IRTX, IRRX, RESET, and All Port Pins	VIH		0.7 x VDD		VDD	V

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RECOMMENDED OPERATING CONDITIONS (continued)

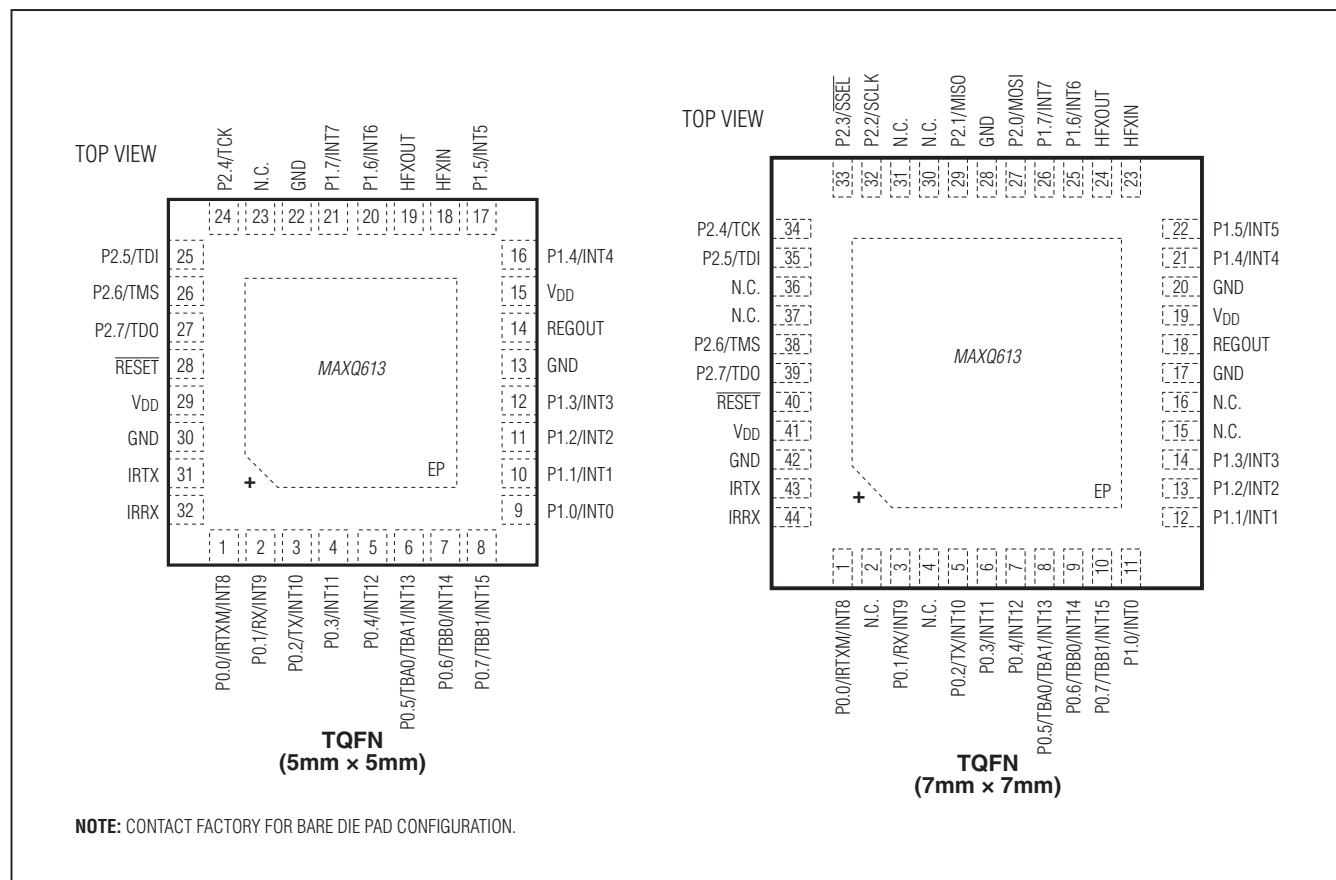
(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Schmitt)	V _{IHYS}	V _{DD} = 3.3V, T _A = +25°C		300		mV
Input Low Voltage for HFXIN	V _{IL_HFXIN}		V _{GND}		0.3 x V _{DD}	V
Input High Voltage for HFXIN	V _{IH_HFXIN}		0.7 x V _{DD}		V _{DD}	V
IRRX Input Filter Pulse-Width Reject	t _{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t _{IRRX_A}		300			ns
Output Low Voltage for IRTX	V _{OL_IRTX}	V _{DD} = 3.6V, I _{OL} = 25mA (Note 3)			1.0	V
		V _{DD} = 2.35V, I _{OL} = 10mA (Note 3)			1.0	
		V _{DD} = 1.85V, I _{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{\text{RESET}}$ and All Port Pins (Note 9)	V _{OL}	V _{DD} = 3.6V, I _{OL} = 11mA (Note 3)		0.4	0.5	V
		V _{DD} = 2.35V, I _{OL} = 8mA (Note 3)		0.4	0.5	
		V _{DD} = 1.85V, I _{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V _{OH}	I _{OH} = -2mA	V _{DD} - 0.5		V _{DD}	V
Input/Output Pin Capacitance for All Port Pins	C _{IO}	(Note 4)			15	pF
Input Leakage Current	I _L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{\text{RESET}}$, IRTX, IRRX, P0, P1, P2	R _{PU}	V _{DD} = 3.0V, V _{OL} = 0.4V (Note 4)	16	28	39	kΩ
		V _{DD} = 2.0V, V _{OL} = 0.4V	17	30	41	
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f _{HFXIN}		1		12	MHz
Crystal/Resonator Period	t _{HFXIN}			1/f _{HFXIN}		ns
Crystal/Resonator Warmup Time	t _{XTAL_RDY}	From initial oscillation		8192 x t _{HFXIN}		ms
Oscillator Feedback Resistor	R _{OSCF}	(Note 4)	0.5	1.0	1.5	MΩ
EXTERNAL CLOCK INPUT						
External Clock Frequency	f _{XCLK}		DC		12	MHz
External Clock Period	t _{XCLK}			1/f _{XCLK}		ns
External Clock Duty Cycle	t _{XCLK_DUTY}	(Note 4)	45		55	%
System Clock Frequency	f _{CK}			f _{HFXIN}		MHz
		HFXOUT = GND		f _{XCLK}		
System Clock Period	t _{CK}			1/f _{CK}		ns
NANOPOWER RING						
Nanopower Ring Frequency	f _{NANO}	T _A = +25°C	3.0	8.0	20.0	kHz
		T _A = +25°C, V _{DD} = POR voltage (Note 4)	1.7	2.4		
Nanopower Ring Duty Cycle	t _{NANO}	(Note 4)	40		60	%
Nanopower Ring Current	I _{NANO}	Typical at V _{DD} = 1.64V, T _A = +25°C (Note 4)		40	400	nA

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Pin Configurations



Pin Description

PIN			NAME	FUNCTION
BARE DIE	32 TQFN-EP	44 TQFN-EP		
POWER PINS				
15, 36	15, 29	19, 41	VDD	Supply Voltage
13, 16, 25, 37	13, 22, 30	17, 20, 28, 42	GND	Ground. Connect directly to the ground plane.
14	14	18	REGOUT	1.8V Regulator Output. This pin must be connected to ground through a 1.0μF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.

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Pin Description (continued)

PIN			NAME	FUNCTION	
BARE DIE	32 TQFN-EP	44 TQFN-EP			
RESET PIN					
35	28	40	RESET	Digital, Active-Low, Reset Input/Output. The device remains in reset as long as this pin is low and begins executing from the utility ROM at address 8000h when this pin returns to a high state. The pin includes pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin can be left unconnected if there is no need to place the device in a reset state using an external signal. This pin is driven low as an output when an internal reset condition occurs.	
CLOCK PINS					
20	18	23	HFXIN	High-Frequency Crystal Input. Connect an external crystal or resonator between HFXIN and HFXOUT for use as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is unconnected.	
21	19	24	HFXOUT		
IR FUNCTION PINS					
38	31	43	IRTX	IR Transmit Output. IR transmission pin capable of sinking 25mA. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
39	32	44	IRRX	IR Receive Input. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.	
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS					
				Port 0 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD0, PO0, and PIO registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All alternate functions must be enabled from software before they can be used.	
				GPIO PORT PIN	
1	1	1	P0.0/IRTXM/INT8	P0.0	IR Modulator Output/INT8
2	2	3	P0.1/RX/INT9	P0.1	USART Receive/INT9
3	3	5	P0.2/TX/INT10	P0.2	USART Transmit/INT10
4	4	6	P0.3/INT11	P0.3	INT11
5	5	7	P0.4/INT12	P0.4	INT12
6	6	8	P0.5/TBA0/TBA1/INT13	P0.5	Type B Timer 0 Pin A or Type B Timer 1 Pin A/INT13

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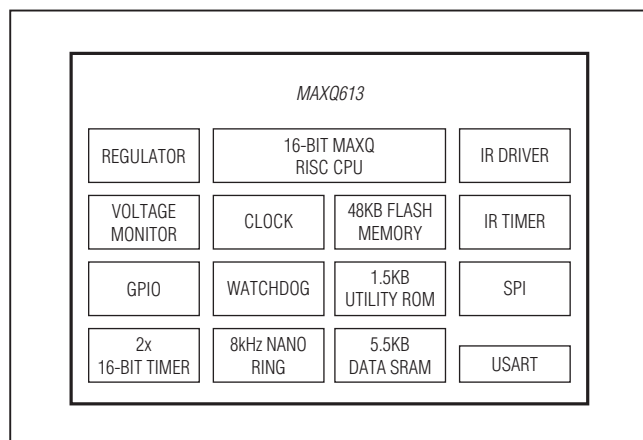
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Pin Description (continued)

PIN			NAME	FUNCTION	
BARE DIE	32 TQFN-EP	44 TQFN-EP			
7	7	9	P0.6/TBB0/ INT14	P0.6	Type B Timer 0 Pin B/INT14
8	8	10	P0.7/TBB1/ INT15	P0.7	Type B Timer 1 Pin B/INT15
			Port 1 General-Purpose, Digital I/O Pins with Interrupt Capability. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD1, PO1, and PI1 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All external interrupts must be enabled from software before they can be used.		
				GPIO PORT PIN	EXTERNAL INTERRUPT
9	9	11	P1.0/INT0	P1.0	INT0
10	10	12	P1.1/INT1	P1.1	INT1
11	11	13	P1.2/INT2	P1.2	INT2
12	12	14	P1.3/INT3	P1.3	INT3
17	16	21	P1.4/INT4	P1.4	INT4
18	17	22	P1.5/INT5	P1.5	INT5
22	20	25	P1.6/INT6	P1.6	INT6
23	21	26	P1.7/INT7	P1.7	INT7
			Port 2 General-Purpose, Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD2, PO2, and PI2 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.		
				GPIO PORT PIN	SPECIAL FUNCTION
24	—	27	P2.0/MOSI	P2.0	SPI: Master Out-Slave In
26	—	29	P2.1/MISO	P2.1	SPI: Master In-Slave Out
28	—	32	P2.2/SCLK	P2.2	SPI: Slave Clock
30	—	33	P2.3/SSSEL	P2.3	SPI: Active-Low Slave Select
31	24	34	P2.4/TCK	P2.4	JTAG: Test Clock
32	25	35	P2.5/TDI	P2.5	JTAG: Test Data In
33	26	38	P2.6/TMS	P2.6	JTAG: Test Mode Select
34	27	39	P2.7/TDO	P2.7	JTAG: Test Data Out
NO CONNECTION PINS					
—	23	2, 4, 15, 16, 30, 31, 36, 37	N.C.	No Connection. Not internally connected.	
—	—	—	EP	Exposed Pad. Connect EP directly to the ground plane.	

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Block Diagram



Detailed Description

The MAXQ613 provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ, 16-bit RISC core; 48KB of program flash memory; 1.5KB data RAM; soft stack; 16 general-purpose registers; and three data pointers. The MAXQ core has the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Lower active-mode current combined with the even lower MAXQ613 stop-mode current (0.2µA typ) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation. A high-current IR drive pin capable of sinking up to 25mA current and output pins capable of sinking up to 5mA are ideal for IR applications. It also includes general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the microcontroller's minimum operating voltage.

At the heart of the device is the MAXQ 16-bit, RISC core. Operating from DC to 12MHz, almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true-code operation. When active device operation is not required, an ultra-low-power stop mode

can be invoked from software, resulting in quiescent current consumption of less than 0.2µA (typ) and 2.0µA (max). The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set, and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The device is based on Maxim's low-power, 16-bit MAXQ20S family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the device is implemented as a pipelined processor with performance approaching 1MIPS per MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that are important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with autoincrement/decrement support.

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Memory

The microcontroller incorporates several memory types:

- 48KB program flash memory
- 1.5KB SRAM data memory
- 5.5KB utility ROM
- Soft stack

Memory Protection

The optional memory-protection feature separates code memory into three areas: system, user loader, and user application. Code in the system area can be kept confidential. Code in the user areas can be prevented from reading and writing system code. The user loader can also be protected from user application code.

Memory protection is implemented using privilege levels for code. Each area has an associated privilege level. RAM/ROM are assigned privilege levels as well. Refer to the *MAXQ610 User's Guide* for a more thorough explanation of the topic. See Table 1.

Stack Memory

The device provides a soft stack that can be used to store program return addresses (for subroutine calls and interrupt handling) and other general-purpose data. This soft stack is located in the 1.5KB SRAM data memory, which means that the SRAM data memory must be shared between the soft stack and general-purpose application data storage. However, the location and size of the soft stack is determined by the user, providing maximum flexibility when allocating resources for a particular application. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store and retrieve values explicitly using the stack by means of the PUSH, POP, and POPJ instructions.

The SP pointer indicates the current top of the stack, which initializes by default to the top of the SRAM data memory. As values are pushed onto the stack, the SP pointer decrements, which means that the stack grows downward towards the bottom (lowest address) of the data memory. Popping values off the stack causes the SP pointer value to increase. Refer to the *MAXQ610 User's Guide* for more details.

Utility ROM

The utility ROM is a 5.5KB block of internal ROM memory located in program space beginning at address 8000h. This ROM includes the following routines:

- In-system programming (bootstrap loader) using JTAG interface
- In-circuit debugging routines using JTAG interface
- Production test routines (internal memory tests, memory loader, etc.), which are used for internal testing only, and are generally of no use to the end-application developer
- User-callable routines for in-application flash programming, buffer copying, and fast table lookup (more information on these routines can be found in the *MAXQ610 User's Guide*)

Following any reset, execution begins in the utility ROM at address 8000h. At this point, unless loader mode or test mode has been invoked (which requires special programming through the JTAG interface), the utility ROM in the device always automatically jumps to location 0000h, which is the beginning of user application code in program flash memory.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. Three

Table 1. Memory Areas and Associated Maximum Privilege Levels

AREA	PAGE ADDRESS	MAXIMUM PRIVILEGE LEVEL
System	0 to ULDR-1	High
User Loader	ULDR to UAPP-1	Medium
User Application	UAPP to top	Low
Utility ROM	N/A	High
Other (RAM)	N/A	Low

16-Bit Microcontroller with Infrared Module**Table 2. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)**

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (μs)
00	Sysclk/2 ¹⁵	2.7ms	42.7
01	Sysclk/2 ¹⁸	21.9ms	42.7
10	Sysclk/2 ²¹	174.7ms	42.7
11	Sysclk/2 ²⁴	1.4s	42.7

different password locks are provided, each of which can be used to protect a different area of memory (system memory, user loader, and user application). Each password lock is controlled by a 16-word area of flash memory; if the password is set to all FFFFh values or all 0000h values, the password is disabled. Otherwise, the password is active and must be matched by the user of the bootloader or debugger before access is granted to the corresponding area of flash program memory. Refer to the *MAXQ610 User's Guide* for more details.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2¹⁵ to 2²⁴ system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 2.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

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Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[2:0]}$
- Carrier Frequency ($f_{CARRIER}$) = $f_{IRCLK}/(IRCAH + IRCAL + 2)$
- Carrier High Time = $IRCAH + 1$
- Carrier Low Time = $IRCAL + 1$
- Carrier Duty Cycle = $(IRCAH + 1)/(IRCAH + IRCAL + 2)$

During transmission, the IRCA register is latched for each IRV down-count interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV down-count interval so that duty-cycle variation and frequency shifting is possible from one interval to the next, which is illustrated in Figure 1.

Figure 2 illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the

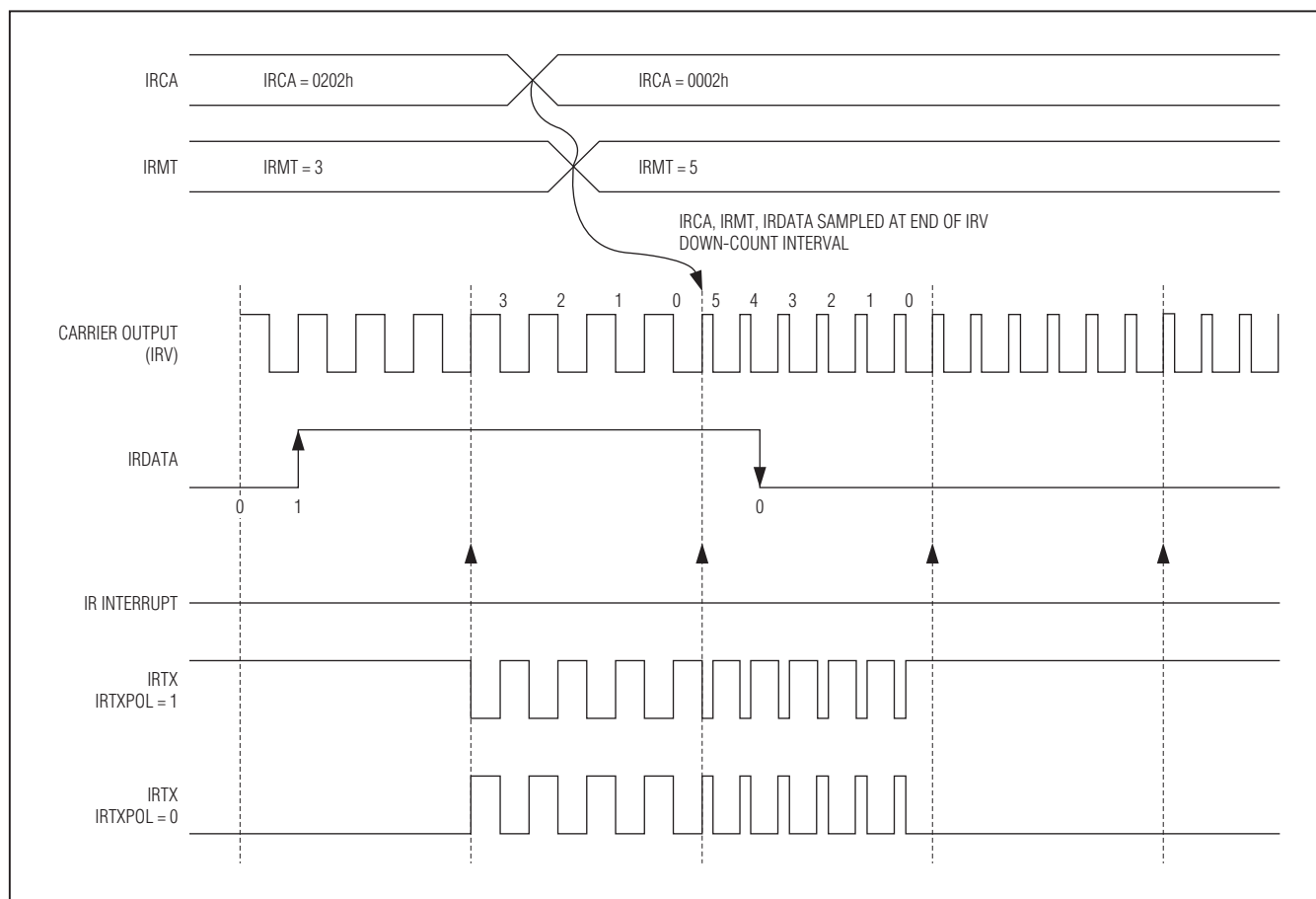


Figure 1. IR Transmit Frequency Shifting Example (IRCFME = 0)

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IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle

condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR

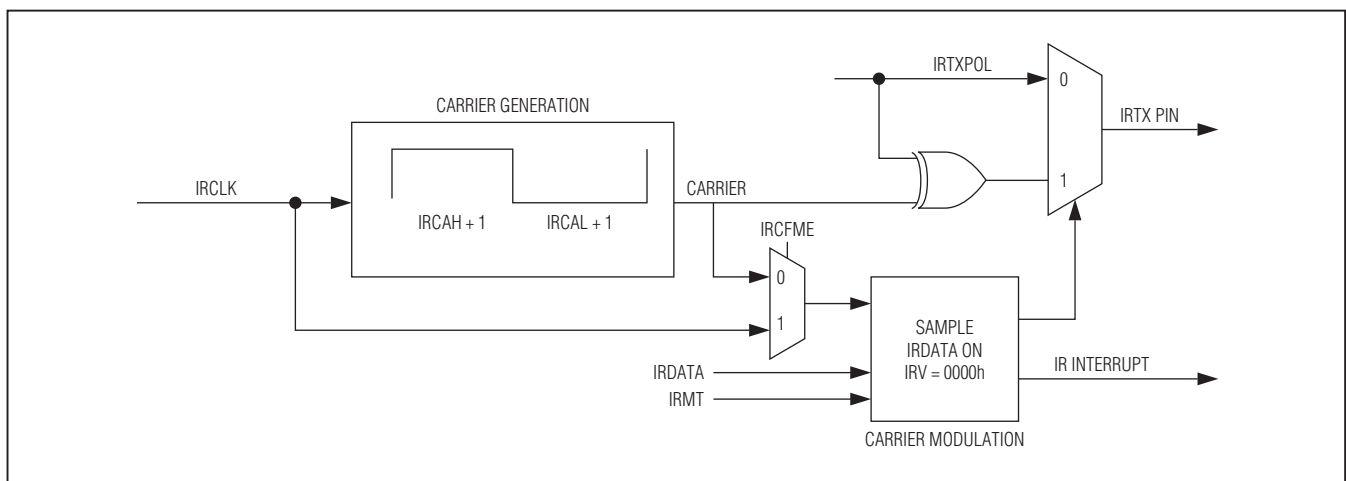


Figure 2. IR Transmit Carrier Generation and Carrier Modulator Control

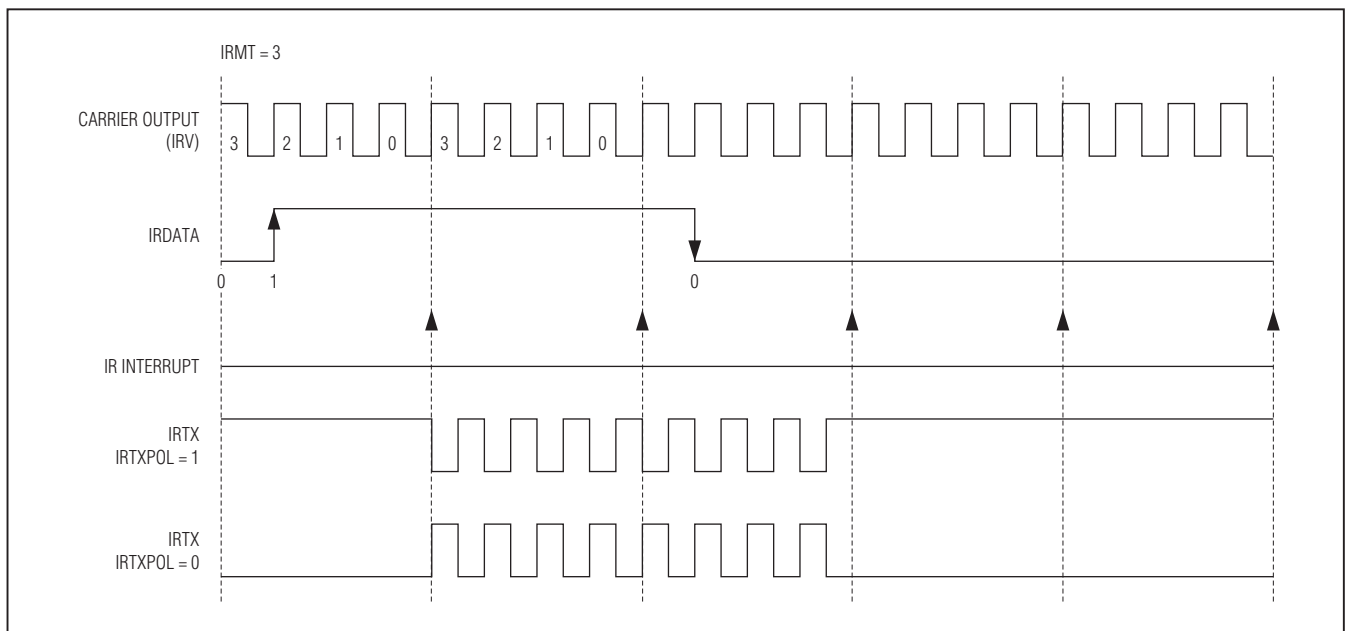


Figure 3. IR Transmission Waveform (IRCFME = 0)

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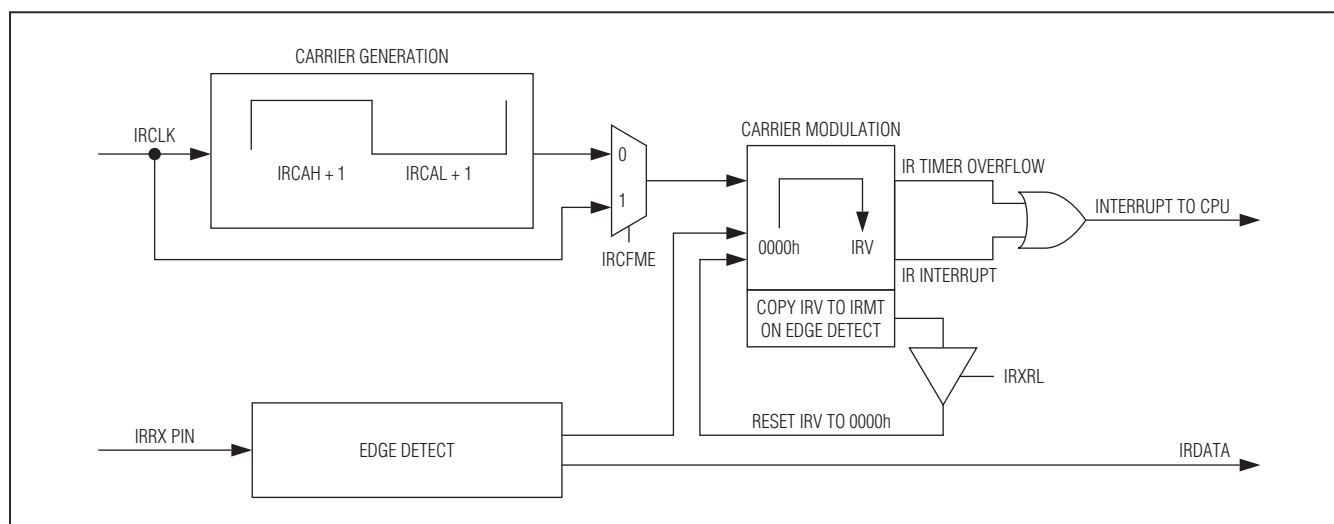


Figure 5. IR Capture

enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode (IRMODE = 1) or clearing IREN = 0.

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register only counts qualified edges. The IRIF interrupt flag (normally used to signal a capture when RXBCNT = 0) now becomes set if two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. When the RXBCNT bit is changed from 0 to 1, the IRMT register is set to 0001h. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit defines whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits). Figure 6 and the descriptive sequence embedded

in the figure illustrate the expected usage of the receive burst-count mode.

16-Bit Timers/Counters

The microcontroller provides two timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2^n divider (for $n = 0, 2, 4, 6, 8, 10$)

USART

The device provides a USART peripheral with the following features:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers
- Programmable interrupt when transmit or receive data operation completes
- Independent programmable baud-rate generator
- Optional 9th bit parity support
- Start/stop bit support

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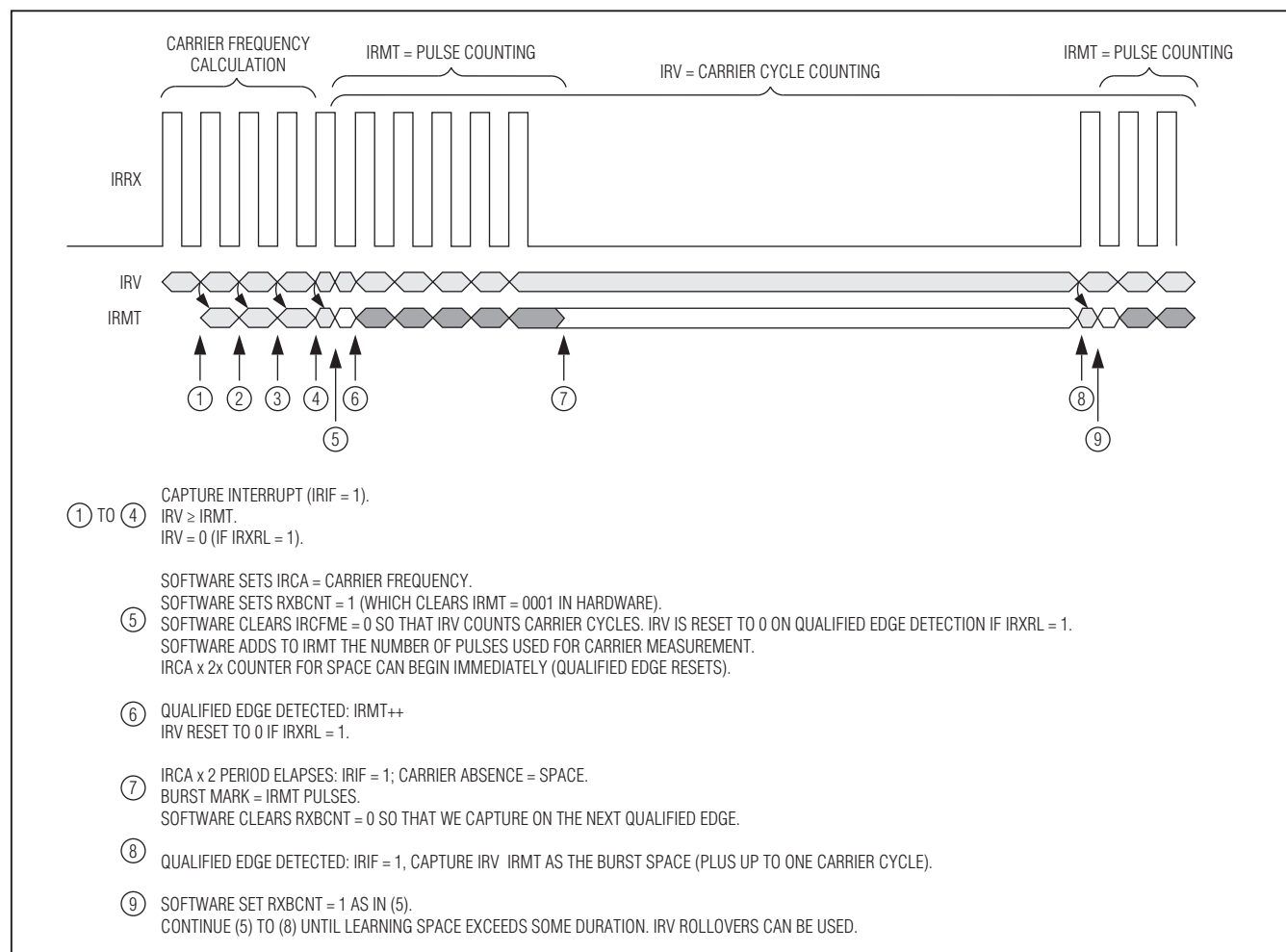


Figure 6. Receive Burst-Count Example

Table 3. USART Mode Details

MODE	TYPE	START BITS	DATA BITS	STOP BITS
Mode 0	Synchronous	N/A	8	N/A
Mode 1	Asynchronous	1	8	1
Mode 2	Asynchronous	1	8 + 1	1
Mode 3	Asynchronous	1	8 + 1	1

Serial Peripheral Interface (SPI)

The integrated SPI provides an independent serial communication channel that communicates synchronously with peripheral devices in a multiple master or multiple slave system. The interface allows access to a 4-wire, full-duplex serial bus, and can be operated in either master mode or slave mode. Collision detection

is provided when two or more masters attempt a data transfer at the same time.

The maximum SPI master transfer rate is Sysclk/2. When operating as an SPI slave, the device can support up to Sysclk/4 SPI transfer rate. Data is transferred as an 8-bit or 16-bit value, MSB first. In addition, the SPI module supports configuration of an active \overline{SSEL} state (active low or active high) through the slave active select.

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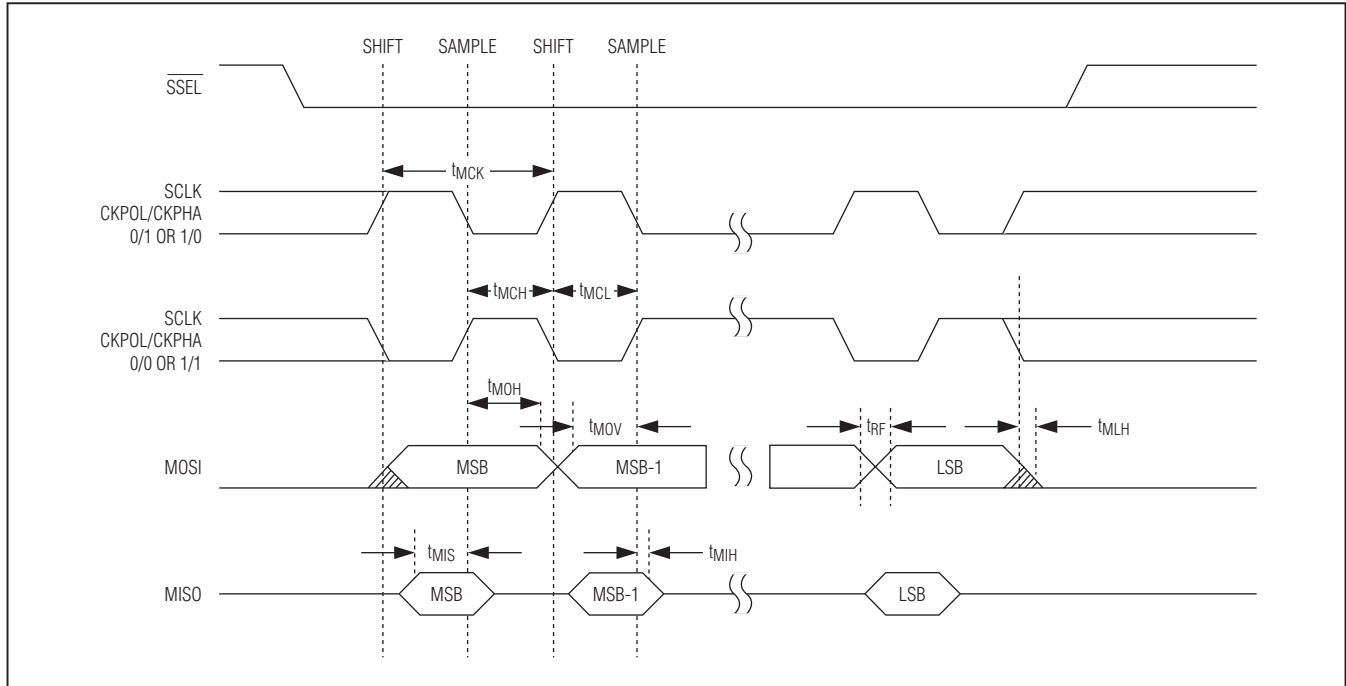


Figure 7. SPI Master Communication Timing

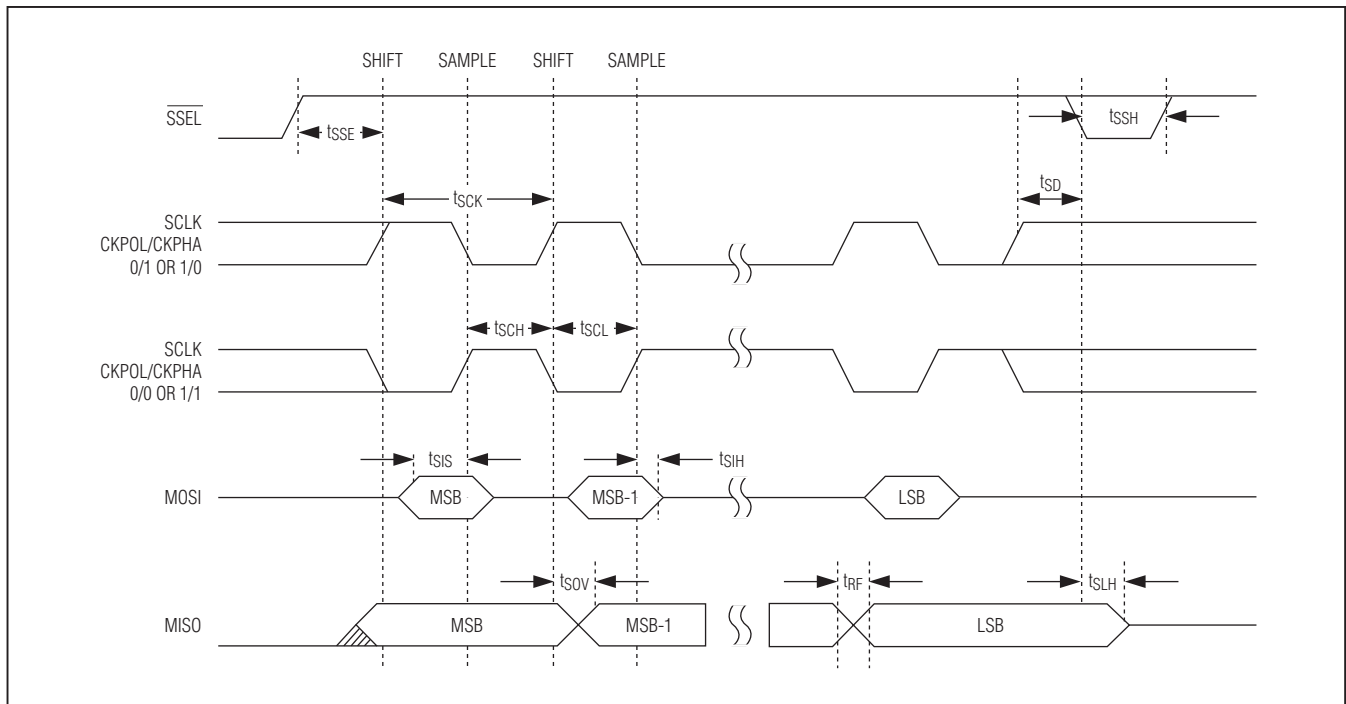


Figure 8. SPI Slave Communication Timing

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Power-Fail Detection

Figures 11, 12, and 13 show the power-fail detection and response during normal and stop-mode operation. If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2¹¹ nanopower ring oscillator clocks (~256ms)
- 2¹² nanopower ring oscillator clocks (~512ms)
- 2¹³ nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two

nanopower ring-oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring-oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the \overline{RESET} pin being driven low externally or the watchdog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 crystal cycles after the reset source is removed.

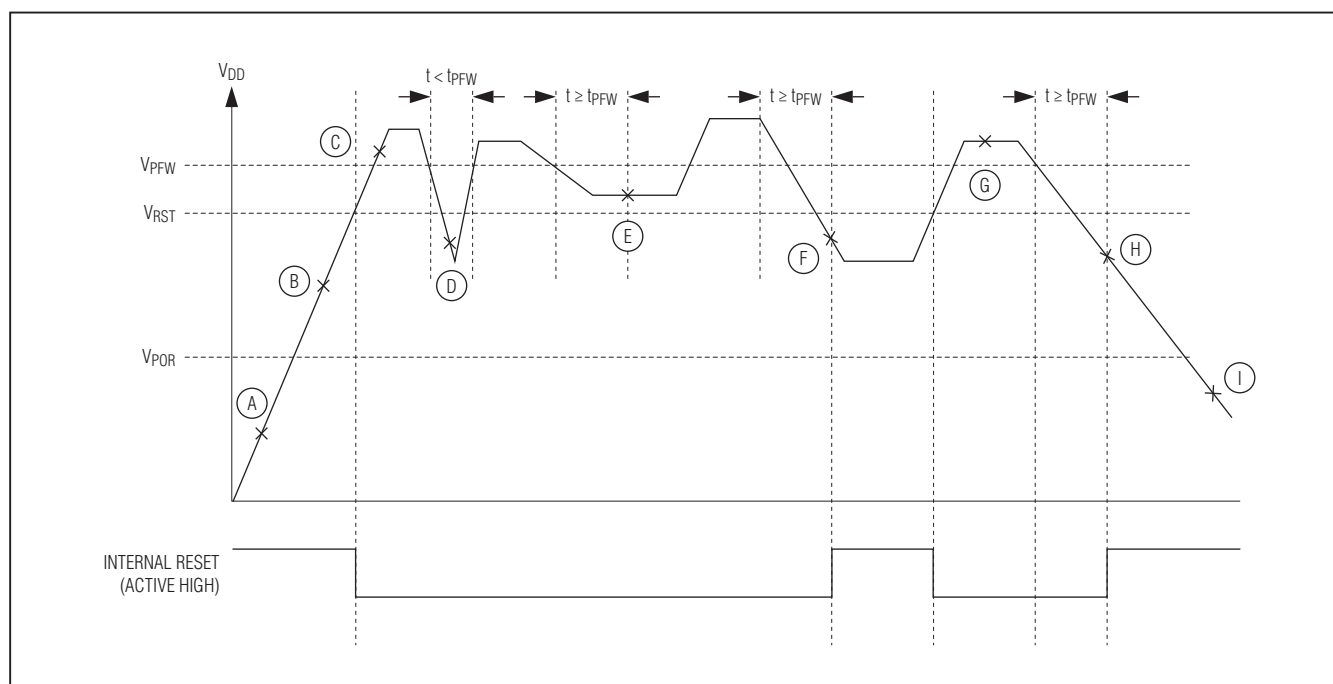


Figure 11. Power-Fail Detection During Normal Operation

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Table 4. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	—	$V_{DD} < V_{POR}$.
B	On	On	On	—	$V_{POR} < V_{DD} < V_{RST}$. Crystal warmup time, t_{XTAL_RDY} . CPU held in reset.
C	On	On	On	—	$V_{DD} > V_{RST}$. CPU normal operation.
D	On	On	On	—	Power drop too short. Power-fail not detected.
E	On	On	On	—	$V_{RST} < V_{DD} < V_{PFW}$. PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW} , at which time a power-fail interrupt is gener- ated (if enabled). CPU continues normal operation.
F	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
G	On	On	On	—	$V_{DD} > V_{RST}$. Crystal warmup time, t_{XTAL_RDY} . CPU resumes normal operation from 8000h.
H	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
I	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

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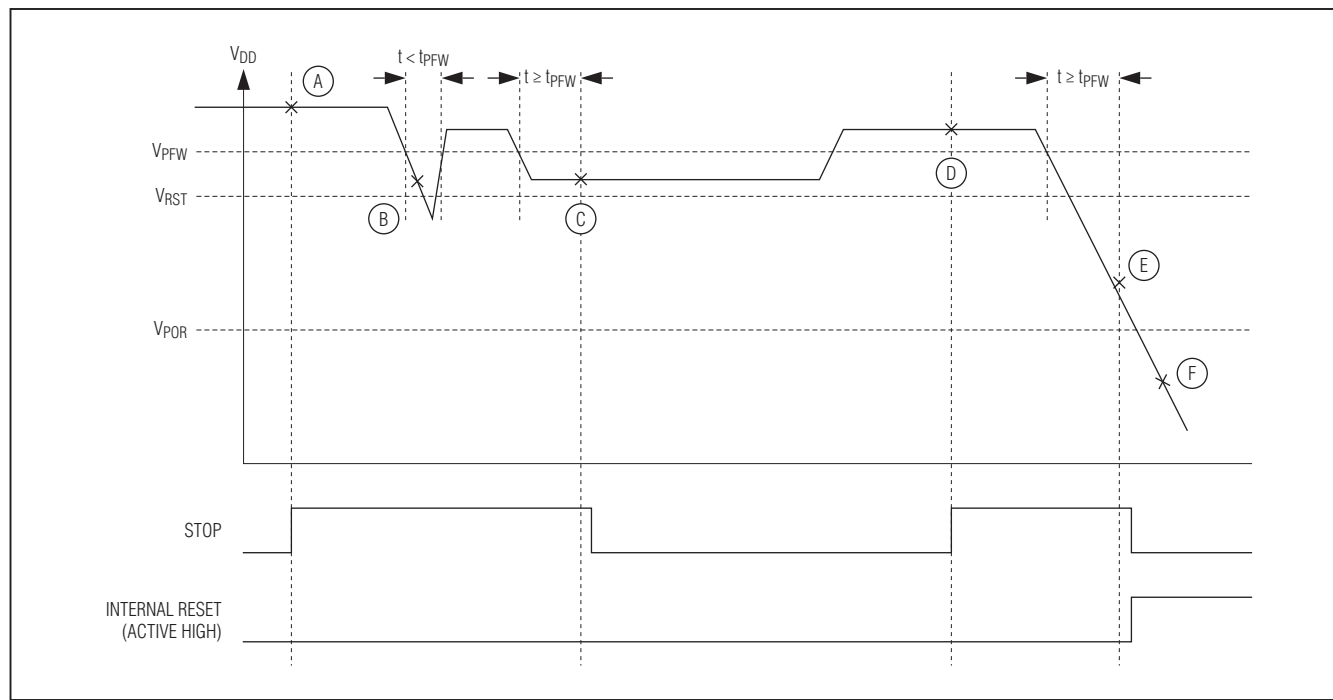


Figure 12. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 5. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY} . Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

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Deviations from the MAXQ610 User's Guide for the MAXQ613

The *MAXQ610 User's Guide* contains all the information that is needed to develop application code for the MAXQ613 microcontroller. However, even though the MAXQ610 and the MAXQ613 are largely code-compatible, there are certain differences between the two devices that must be kept in mind when referring to the *MAXQ610 User's Guide*.

The following registers on the MAXQ610 (which are described in the *MAXQ610 User's Guide*) do not exist on the MAXQ613, and all references to them should be disregarded:

- Port 3 Output Register (PO3)
- Port 3 Direction Register (PD3)
- Port 3 Input Register (PI3)
- Port 4 Output Register (PO4)
- Port 4 Direction Register (PD4)
- Port 4 Input Register (PI4)

Development and Technical Support

Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- In-circuit emulators
- Integrated Development Environments (IDEs)
- Serial-to-JTAG and USB-to-JTAG interface boards for programming and debugging (for microcontrollers with rewritable memory)

A partial list of development tool vendors can be found at www.maximintegrated.com/MAXQ_tools.

For technical support, go to <https://support.maximintegrated.com/micro>.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	21-0140	90-0001
44 TQFN-EP	T4477+2	21-0144	90-0127

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/10	Initial release	—
1	7/10	Corrected bare die numbers in the <i>Pin Description</i> table for V _{DD} , GND, $\overline{\text{RESET}}$, IRTX, IRRX, P2.5/TDI, P2.6/TMS, and P2.7/TDO	9, 10, 11
2	8/10	Corrected the active mode typ value from 2.0mA to 3.25mA in the <i>Features</i>	1
3	1/11	Removed the LQFP and TQFP packages	1, 4, 8, 9, 10, 27
4	7/12	Removed the ESR reference from the REGOUT description in the <i>Pin Description</i> table; changed the MAXQ core reference to MAXQ20S core in the <i>Microprocessor</i> section; updated the IRDIV bit range from [1:0] to [2:0] in the <i>Carrier Generation Module</i> section	8, 11, 14



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