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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	77
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b54l3c6e0y

Table 2. SPC560B54/6x family comparison[1] (continued)

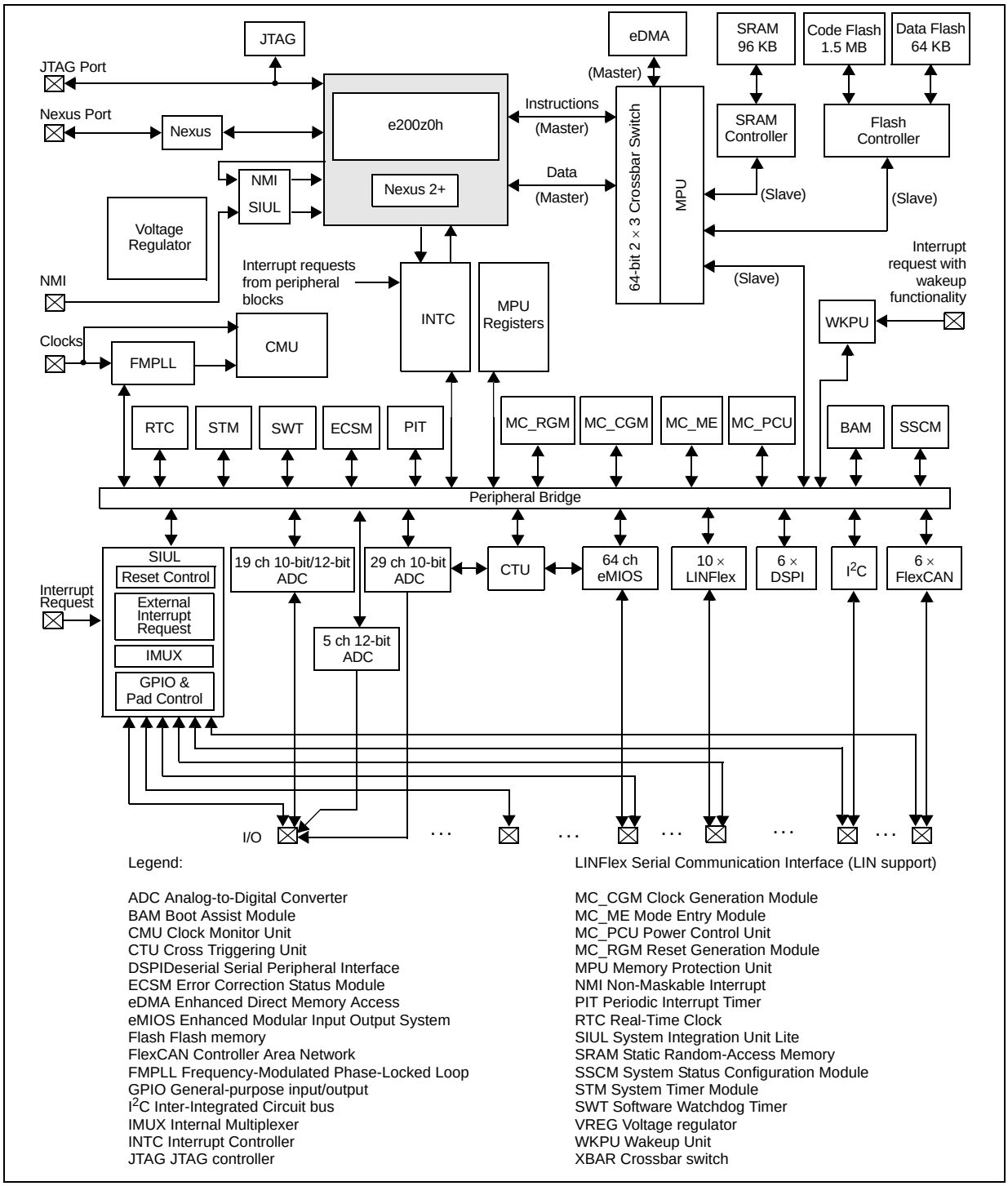
Feature	SPC560B54		SPC560B60			SPC560B64			
OPWM / ICOC[9]	13 ch	33 ch	13 ch	33 ch	33 ch	13 ch	33 ch	33 ch	33 ch
SCI (LINFlex)	4	8	4	8	10	4	8	10	10
SPI (DSPI)	3	5	3	5	6	3	5	6	6
CAN (FlexCAN)	6								
I2C	1								
32 KHz oscillator	Yes								
GPIO[10]	77	121	77	121	149	77	121	149	149
Debug	JTAG								N2+
Package	LQFP 100	LQFP 144	LQFP 100	LQFP 144	LQFP 176	LQFP 100	LQFP 144	LQFP 176	LBGA208[11]

1. Feature set dependent on selected peripheral multiplexing; table shows example.
2. Based on 125 °C ambient operating temperature.
3. Not shared with 12-bit ADC, but possibly shared with other alternate functions.
4. Not shared with 10-bit ADC, but possibly shared with other alternate functions.
5. See the eMIOS section of the chip reference manual for information on the channel configuration and functions.
6. Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
7. Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
8. Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
9. Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.
10. Maximum I/O count based on multiplexing with peripherals.
11. LBGA208 available only as development package for Nexus2+.

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC560B54/6x.

Figure 1. SPC560B54/6x block diagram

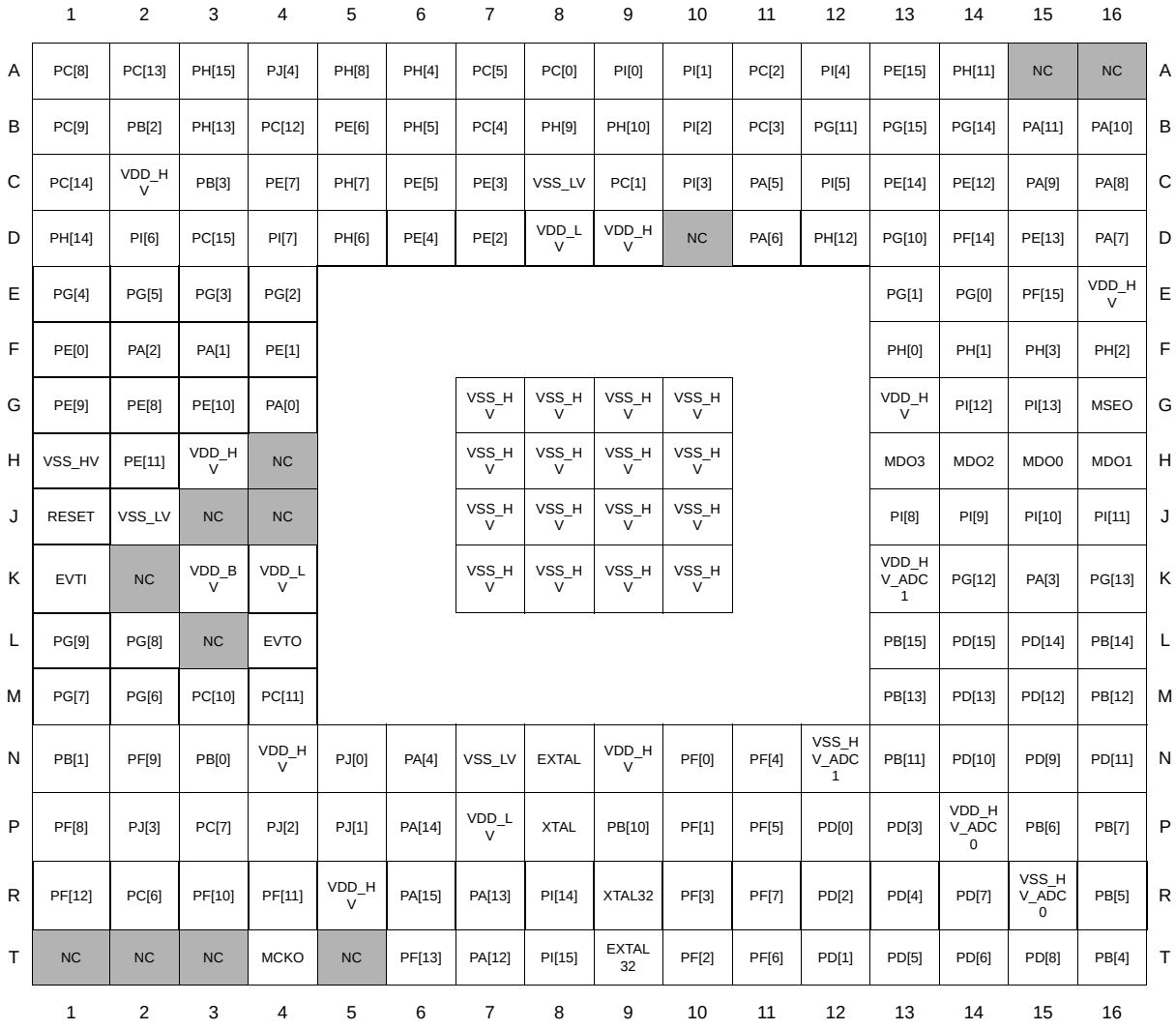


Legend:

ADC Analog-to-Digital Converter
BAM Boot Assist Module
CMU Clock Monitor Unit
CTU Cross Triggering Unit
DSPIDeserial Serial Peripheral Interface
ECSM Error Correction Status Module
eDMA Enhanced Direct Memory Access
eMIOS Enhanced Modular Input Output System
Flash Flash memory
FlexCAN Controller Area Network
FMPLL Frequency-Modulated Phase-Locked Loop
GPIO General-purpose input/output
I^2C Inter-Integrated Circuit bus
IMUX Internal Multiplexer
INTC Interrupt Controller
JTAG JTAG controller
LINFlex Serial Communication Interface (LIN support)
MC_CGM Clock Generation Module
MC_ME Mode Entry Module
MC_PCU Power Control Unit
MC_RGM Reset Generation Module
MPU Memory Protection Unit
NMI Non-Maskable Interrupt
PIT Periodic Interrupt Timer
RTC Real-Time Clock
SIUL System Integration Unit Lite
SRAM Static Random-Access Memory
SSCM System Status Configuration Module
STM System Timer Module
SWT Software Watchdog Timer
VREG Voltage regulator
WKPU Wakeup Unit
XBAR Crossbar switch

Table 3. SPC560B54/6x series block summary (continued)

Block	Function
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	PH[15]	PJ[4]	PH[8]	PH[4]	PC[5]	PC[0]	PI[0]	PI[1]	PC[2]	PI[4]	PE[15]	PH[11]	NC	NC	A
B	PC[9]	PB[2]	PH[13]	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	PI[2]	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	PI[3]	PA[5]	PI[5]	PE[14]	PE[12]	PA[9]	PA[8]	C
D	PH[14]	PI[6]	PC[15]	PI[7]	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	PH[12]	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	PI[12]	PI[13]	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			PI[8]	PI[9]	PI[10]	PI[11]	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_ADC1	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	VDD_HV	PJ[0]	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	VSS_HV_ADC1	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	PJ[3]	PC[7]	PJ[2]	PJ[1]	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC0	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	PI[14]	XTAL32	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC0	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	PI[15]	EXTAL32	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

NOTE: The LBGA208 is available only as development package for Nexus 2+.

NC = Not connected

Figure 5. LBGA208 configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8], PC[0] and PH[9:10] are in input weak pull-up when out of reset.
- RESET pad is driven low by the device till 40 FIRC clock cycles after phase2 completion. Minimum phase3 duration is 40 FIRC cycles.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					LQFP 100	LQFP 144	LQFP 176	LBGA 208(1)
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input weak pull-up after RGM PHASE2 and 40 FIRC cycles	17	21	29	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	50	58	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	Tristate	34	48	56	P8

1. LBGA208 available only as development package for Nexus2+.

3.7 Functional port pins

The functional port pins are listed in *Table 6*.

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — — — —	GPIO[24] — — — OSC32K_XTAL[8] WKPU[25][5] ADC0_S[0] ADC1_S[4]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	39	53	61	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — — — —	GPIO[25] — — — OSC32K_EXTAL[8] WKPU[26][5] ADC0_S[1] ADC1_S[5]	SIUL — — — OSC32K WKPU ADC_0 ADC_1	I — — — — I[9] I I	I	—	38	52	60	T9
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — — — —	GPIO[26] — — — WKPU[8][5] ADC0_S[2] ADC1_S[6]	SIUL — — — WKPU ADC_0 ADC_1	I/O — — — I I I	J	Tristate	40	54	62	P9

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 — —	GPIO[44] E0UC[12] — — EIRQ[19] SIN_2	SIUL eMIOS_0 — — SIUL DSPI_2	I/O I/O — — I I	M	Tristate	97	141	173	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	98	142	174	A2
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	3	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] CS0_2 — EIRQ[20]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	M	Tristate	4	4	4	D3
Port D											

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 — —	GPIO[52] — — — ADC0_P[8] ADC1_P[8]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	45	67	81	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 — —	GPIO[53] — — — ADC0_P[9] ADC1_P[9]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	46	68	82	T13
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 — —	GPIO[54] — — — ADC0_P[10] ADC1_P[10]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	47	69	83	T14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 — —	GPIO[55] — — — ADC0_P[11] ADC1_P[11]	SIUL — — — ADC_0 ADC_1	I — — — I I	I	Tristate	48	70	84	R14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	58	66	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	59	67	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	60	68	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	61	69	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	J	Tristate	—	62	70	R11

3.8 Nexus 2+ pins

In the LBGA208 package, eight additional debug pins are available (see *Table 7*).

Table 7. Nexus 2+ pin descriptions

Port pin	Function	I/O direction	Pad type	Function after reset	Pin number		
					LQFP 100	LQFP 144	LBGA 208(1)
MCKO	Message clock out	O	F	—	—	—	T4
MDO0	Message data out 0	O	M	—	—	—	H15
MDO1	Message data out 1	O	M	—	—	—	H16
MDO2	Message data out 2	O	M	—	—	—	H14
MDO3	Message data out 3	O	M	—	—	—	H13
EVTI	Event in	I	M	Pull-up	—	—	K1
EVTO	Event out	O	M	—	—	—	L4
MSEO	Message start/end out	O	M	—	—	—	G16

1. LBGA208 available only as development package for Nexus2+.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

4.2.1 NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 9* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 9. PAD3V5V field description(1)

Value(2)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. See the device reference manual for more information on the NVUSRO register.
2. Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.2.2 NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. *Table 10* shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 10. OSCILLATOR_MARGIN field description(1)

Value(2)	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1. See the device reference manual for more information on the NVUSRO register.
2. Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

4.2.3 NVUSRO[WATCHDOG_EN] field description

The watchdog enable/disable configuration after reset is dependent on the WATCHDOG_EN bit value. *Table 11* shows how NVUSRO[WATCHDOG_EN] controls the device configuration.

Table 11. WATCHDOG_EN field description

Value(1)	Description
0	Disable after reset
1	Enable after reset

1. Default manufacturing value is '1'. Value can be programmed by customer in Shadow Flash.

Table 14. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	S R	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	S R	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
V_{SS_LV}(3)	S R	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}(4)	S R	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	3.0	V_{DD} + 0.1	
V_{SS_ADC}	S R	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}(5)	S R	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	4.5	5.5	V
			Voltage drop(2)	3.0	5.5	
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	S R	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	S R	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	S R	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	S R	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250×10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.
3. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
4. 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). While the supply voltage ramps up, the slope on V_{DD_BV} should be less than $0.9V_{DD\_HV}$ in order to ensure the device does not enter regulator bypass mode.
5. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
6. Guaranteed by device validation.
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

Note: RAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.5 Thermal characteristics

4.5.1 External ballast resistor recommendations

External ballast resistor on V_{DD_BV} pin helps in reducing the overall power dissipation inside the device. This resistor is required only when maximum power consumption exceeds the limit imposed by package thermal characteristics.

As stated in *Table 15* LQFP thermal characteristics, considering a thermal resistance of LQFP144 as 48.3 °C/W, at ambient temperature T_A = 125 °C, the junction temperature T_j will cross 150 °C if the total power dissipation is greater than (150 – 125)/48.3 = 517 mW. Therefore, the total device current I_{DDMAX} at 125 °C/5.5 V must not exceed 94.1 mA (i.e., PD/VDD). Assuming an average $I_{DD}(V_{DD\_HV})$ of 15–20 mA consumption typically during device RUN mode, the LV domain consumption $I_{DD}(V_{DD\_BV})$ is thus limited to $I_{DDMAX} - I_{DD}(V_{DD\_HV})$, i.e., 80 mA.

Therefore, respecting the maximum power allowed as explained in *Section 4.5.2: Package thermal characteristics*, it is recommended to use this resistor only in the 125 °C/5.5 V operating corner as per the following guidelines:

- If $I_{DD}(V_{DD\_BV}) < 80$ mA, then no resistor is required.
- If 80 mA < $I_{DD}(V_{DD\_BV}) < 90$ mA, then 4 Ω resistor can be used.
- If $I_{DD}(V_{DD\_BV}) > 90$ mA, then 8 Ω resistor can be used.

Using resistance in the range of 4–8 Ω, the gain will be around 10–20% of total consumption on V_{DD_BV}. For example, if 8 Ω resistor is used, then power consumption when $I_{DD}(V_{DD\_BV})$ is 110 mA is equivalent to power consumption when $I_{DD}(V_{DD\_BV})$ is 90 mA (approximately) when resistor not used.

In order to ensure correct power up, the minimum V_{DD_BV} to be guaranteed is 30 ms/V. If the supply ramp is slower than this value, then LVDHV3B monitoring ballast supply V_{DD_BV} pin gets triggered leading to device reset. Until the supply reaches certain threshold, this low voltage detector (LVD) generates destructive reset event in the system. This threshold depends on the maximum $I_{DD}(V_{DD\_BV})$ possible across the external resistor.

4.5.2 Package thermal characteristics

Table 15. LQFP thermal characteristics(1)

Symbol		C	Parameter	Conditions(2)	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection(3)	Single-layer board — 1s	100	—	—	64	°C/W
					144	—	—	64	
					176	—	—	64	
				Four-layer board — 2s2p	100	—	—	49.7	
					144	—	—	48.3	
					176	—	—	47.3	

Table 15. LQFP thermal characteristics[1] (continued)

Symbol		C	Parameter	Conditions[2]	Pin count	Value			Unit
						Min	Typ	Max	
$R_{\theta JB}$	CC		Thermal resistance, junction-to-board[4]	Single-layer board — 1s	100	—	—	36	°C/W
					144	—	—	38	
					176	—	—	38	
				Four-layer board — 2s2p	100	—	—	33.6	
					144	—	—	33.4	
					176	—	—	33.4	
$R_{\theta JC}$	CC		Thermal resistance, junction-to-case[5]	Single-layer board — 1s	100	—	—	23	°C/W
					144	—	—	23	
					176	—	—	23	
				Four-layer board — 2s2p	100	—	—	19.8	
					144	—	—	19.2	
					176	—	—	18.8	

1. Thermal characteristics are targets based on simulation.
2. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C.
3. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA} and R_{thJMA}.
4. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.
5. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.5.3 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using *Equation 1*:

Equation 1 $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A is the ambient temperature in °C.

$R_{\theta JA}$ is the package junction-to-ambient thermal resistance, in °C/W.

P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$).

P_{INT} is the product of I_{DD} and V_{DD}, expressed in watts. This is the chip internal power.

$P_{I/O}$ represents the power dissipation on input and output pins; user determined.

Most of the time for the applications, $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see *Section 4.4: Recommended operating conditions*).

Table 26. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	W
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low-power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

Table 32. Flash power supply DC electrical characteristics

Symbol		Parameter	Conditions(1)		Value			Unit
					Min	Typ	Max	
I_{CFREAD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on read access	Flash module read f_{CPU} = 64 MHz	Code Flash	—	—	33	mA
I_{DFREAD}				Data Flash	—	—	33	
I_{CFMOD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} on matrix modification (program/erase)	Program/Erase on-going while reading Flash registers f_{CPU} = 64 MHz	Code Flash	—	—	52	mA
I_{DFMOD}				Data Flash	—	—	33	
I_{CFLPW}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash low power mode	—	Code Flash	—	—	1.1	mA
I_{DFLPW}				Data Flash	—	—	900	µA
I_{CFPWD}	CC	Sum of the current consumption on V_{DD_HV} and V_{DD_BV} during Flash power down mode	—	Code Flash	—	—	150	µA
I_{DFPWD}				Data Flash	—	—	150	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.10.3 Start-up/Switch-off timings

Table 33. Start-up time/Switch-off time

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
$t_{FLARSTEXIT}$	CC	T	Delay for Flash module to exit reset mode	—	—	—	125	µs
$t_{FLALPEXIT}$	CC	T	Delay for Flash module to exit low-power mode	—	—	—	0.5	
$t_{FLAPDEXIT}$	CC	T	Delay for Flash module to exit power-down mode	—	—	—	30	
$t_{FLALPENTRY}$	CC	T	Delay for Flash module to enter low-power mode	—	—	—	0.5	
$t_{FLAPDENTRY}$	CC	T	Delay for Flash module to enter power-down mode	—	—	—	1.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

4.11 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

4.11.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Equation 14 ADC_1 (12-bit)

$$C_F > 8192 \bullet C_S$$

4.17.3 ADC electrical characteristics

Table 44. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	D	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	70	nA
		D		T_A = 25 °C		—	1	70	
		D		T_A = 85 °C			3	100	
		D		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 45. ADC_0 conversion characteristics (10-bit ADC_0)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC0}	SR	—	Voltage on VSS_HV_ADC0 (ADC_0 reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC0}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC0} – 0.1	—	V_{DD_ADC0} + 0.1	V
$I_{ADC0pwd}$	SR	—	ADC_0 consumption in power down mode	—	—	—	50	µA
$I_{ADC0run}$	SR	—	ADC_0 consumption in running mode	—	—	—	5	mA
f_{ADC0}	SR	—	ADC_0 analog frequency	—	6	—	32 + 4%	MHz
Δ_{ADC0_SYS}	SR	—	ADC_0 digital clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC0_PU}	SR	—	ADC_0 power up delay	—	—	—	1.5	µs
t_{ADC0_S}	CC	T	Sampling time[5]	f_{ADC} = 32 MHz, INPSAMP = 17	0.5	—		µs
				f_{ADC} = 6 MHz, INPSAMP = 255	—	—	42	
t_{ADC0_C}	CC	P	Conversion time[6]	f_{ADC} = 32 MHz, INPCMP = 2	0.625	—	—	µs
C_S	CC	D	ADC_0 input sampling capacitance	—	—	—	3	pF

Table 48. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1/DSPI3/DSPI5			DSPI2/DSPI4			Unit
						Min	Typ	Max	Min	Typ	Max	
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2[6]	—	—	2[6]	—	—	
11	t_{SUO}[7]	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
					Slave mode	—	—	52	—	—	160	
12	t_{HO}[7]	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	8	—	—	13	—	—	

1. Operating conditions: C_L = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns.
2. Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.
3. Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.
4. The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.
5. The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.
6. This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR register.
7. SCK and SOUT are configured as MEDIUM pad.

Table 53. LQFP100 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 56. Revision history (continued)

Date	Revision	Changes
12-Sep- 2011	6	Editorial and formatting changes throughout Replaced instances of “e200z0” with “e200z0h” Device family comparison table: – added 1 MB code flash LQFP100 version – added 1.5 MB code flash LQFP144 version – removed 768 KB code flash LQFP176 version – changed LINFlex count for 144-pin LQFP—was ‘6’; is ‘8’ – changed LINFlex count for 176-pin LQFP—was ‘8’; is ‘10’ – replaced 105 °C with 125 °C in footnote 2 SPC560B54/6x block diagram: added GPIO and VREG to legend SPC560B54/6x series block summary: added acronym “JTAGC”; in WKPU function changed “up to 18 external sources” to “up to 27 external sources” LQFP144 pin configuration: for pins 37–72, restored the pin labels that existed prior to 27 July 2010 LQFP176 pin configuration: corrected name of pin 4: was EPC[15]; is PC[15] Added following sections: – Pad configuration during reset phases – Pad configuration during standby mode exit – Voltage supply pins – Pad types – System pins – Functional port pins – Nexus 2+ pins Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Tables “Absolute maximum ratings” and “Recommended operating conditions (3.3 V)”: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description “Recommended operating conditions (5.0 V)” table: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description; changed 3.6V to 3.0V in footnote 2 Section “External ballast resistor recommendations”: replaced “low voltage monitor” with “low voltage detector (LVD)” “I/O input DC electrical characteristics” table: updated I_{LKG} characteristics “MEDIUM configuration output buffer electrical characteristics” table: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O weight: updated table (includes replacing instances of bit “SRE” with “SRC”) “Reset electrical characteristics” table: updated parameter classification for $\lvert I_{WPU} \rvert$ Updated voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); changed “as well as four low voltage detectors” to “as well as five low voltage detectors”; added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$ Updated section “Power consumption”