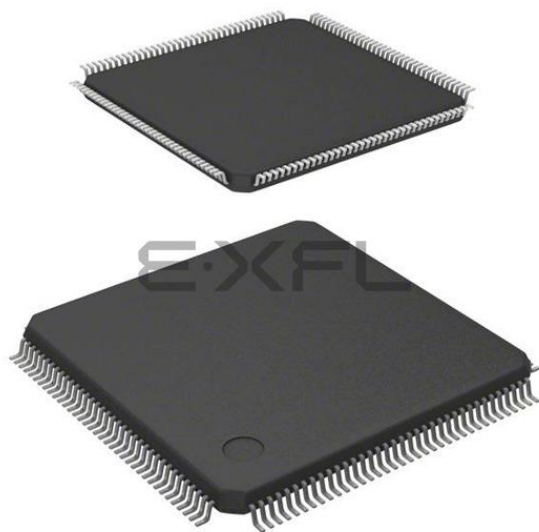




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b54l5b6e0x

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device.

1.2 Description

This family of 32-bit system-on-chip (SoC) microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture technology and only implements the VLE (variable-length encoding) APU (Auxiliary Processor Unit), providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 2. SPC560B54/6x family comparison⁽¹⁾

Feature	SPC560B54		SPC560B60			SPC560B64			
CPU	e200z0h								
Execution speed ⁽²⁾	Up to 64 MHz								
Code flash memory	768 KB		1 MB			1.5 MB			
Data flash memory	64 (4 × 16) KB								
SRAM	64 KB		80 KB			96 KB			
MPU	8-entry								
eDMA	16 ch								
10-bit ADC	Yes								
dedicated ⁽³⁾	7 ch	15 ch	7 ch	15 ch	29 ch	7 ch	15 ch	29 ch	29 ch
shared with 12-bit ADC	19 ch								
12-bit ADC	Yes								
dedicated ⁽⁴⁾	5 ch								
shared with 10-bit ADC	19 ch								
Total timer I/O ⁽⁵⁾ eMIOS	37 ch, 16-bit	64 ch, 16-bit	37 ch, 16-bit	64 ch, 16-bit	64 ch, 16-bit	37 ch, 16-bit	64 ch,1 6-bit	64 ch, 16-bit	64 ch, 16-bit
Counter / OPWM / ICOC ⁽⁶⁾	10 ch								
O(I)PWM / OPWFMB / OPWMCB / ICOC ⁽⁷⁾	7 ch								
O(I)PWM / ICOC ⁽⁸⁾	7 ch	14 ch	7 ch	14 ch	14 ch	7 ch	14 ch	14 ch	14 ch



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A ⁽⁷⁾ —	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS_0 eMIOS_0 — SIUL BAM LINFlex_3	I/O I/O I/O — I I I	S	Input, weak pull-up	72	105	129	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A ⁽⁷⁾	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — O I	S	Pull-down	73	106	130	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] SDA LIN2TX ADC1_S[2]	SIUL eMIOS_0 I ² C_0 LINFlex_2 ADC_1	I/O I/O I/O O I	J	Tristate	74	107	131	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] SCL — EIRQ[16] LIN2RX ADC1_S[3]	SIUL eMIOS_0 I ² C_0 — SIUL LINFlex_2 ADC_1	I/O I/O I/O — I I I	J	Tristate	75	108	132	B15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC0_S[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — I/O I	J	Tristate	—	—	97	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC0_X[0]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	61	83	101	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC0_X[1]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	63	85	103	M13
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC0_X[2]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	65	87	105	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC0_X[3]	SIUL eMIOS_0 — DSPI_0 ADC_0	I/O I/O — O I	J	Tristate	67	89	107	L13



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
Port C											
PC[0] ⁽¹⁰⁾	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	87	126	154	A8
PC[1] ⁽¹⁰⁾	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F ⁽¹¹⁾	Tristate	82	121	149	C9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5]	SIUL DSPI_1 FlexCAN_4 SSCM SIUL	I/O I/O O O I	M	Tristate	78	117	145	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN1RX CAN4RX	SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_1 FlexCAN_4	I/O I/O O O I I I	S	Tristate	77	116	144	B11



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	58	66	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	59	67	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	60	68	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	61	69	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	J	Tristate	—	62	70	R11

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX CS4_0 CAN2TX	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	34	42	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — — —	GPIO[89] E1UC[1] CS5_0 — WKPU[22] ⁽⁵⁾ CAN2RX CAN3RX	SIUL eMIOS_1 DSPI_0 — WKPU FlexCAN_2 FlexCAN_3	I/O I/O O — I I I	S	Tristate	—	33	41	N2
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] CS1_0 LIN4TX E1UC[2]	SIUL DSPI_0 LINFlex_4 eMIOS_1	I/O O O I/O	M	Tristate	—	38	46	R3
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 — —	GPIO[91] CS2_0 E1UC[3] — WKPU[15] ⁽⁵⁾ LIN4RX	SIUL DSPI_0 eMIOS_1 — WKPU LINFlex_4	I/O O I/O — I I	S	Tristate	—	39	47	R4
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] LIN5TX —	SIUL eMIOS_1 LINFlex_5 —	I/O I/O O —	M	Tristate	—	35	43	R1



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PF[13]	PCR[93]	AF0	GPIO[93]	SIUL	I/O	S	Tristate	—	41	49	T6
		AF1	E1UC[26]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	WKPU[16] ⁽⁵⁾	WKPU	I						
		—	LIN5RX	LINFlex_5	I						
PF[14]	PCR[94]	AF0	GPIO[94]	SIUL	I/O	M	Tristate	—	102	126	D14
		AF1	CAN4TX	FlexCAN_4	O						
		AF2	E1UC[27]	eMIOS_1	I/O						
		AF3	CAN1TX	FlexCAN_1	O						
PF[15]	PCR[95]	AF0	GPIO[95]	SIUL	I/O	S	Tristate	—	101	125	E15
		AF1	E1UC[4]	eMIOS_1	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	EIRQ[13]	SIUL	I						
		—	CAN1RX	FlexCAN_1	I						
		—	CAN4RX	FlexCAN_4	I						
Port G											
PG[0]	PCR[96]	AF0	GPIO[96]	SIUL	I/O	M	Tristate	—	98	122	E14
		AF1	CAN5TX	FlexCAN_5	O						
		AF2	E1UC[23]	eMIOS_1	I/O						
		AF3	—	—	—						

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — EIRQ[14] CAN5RX	SIUL — eMIOS_1 — SIUL FlexCAN_5	I/O — I/O — I I	S	Tristate	—	97	121	E13
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] SOUT_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O O —	M	Tristate	—	8	16	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] CS0_3 — WKPU[17] ⁽⁵⁾	SIUL eMIOS_1 DSPI_3 — WKPU	I/O I/O I/O — I	S	Tristate	—	7	15	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] SCK_3 —	SIUL eMIOS_1 DSPI_3 —	I/O I/O I/O —	M	Tristate	—	6	14	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 — —	GPIO[101] E1UC[14] — — WKPU[18] ⁽⁵⁾ SIN_3	SIUL eMIOS_1 — — WKPU DSPI_3	I/O I/O — — I I	S	Tristate	—	5	13	E2

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PG[10]	PCR[106]	AF0 AF1 AF2 AF3 —	GPIO[106] E0UC[24] E1UC[31] — SIN_4	SIUL eMIOS_0 eMIOS_1 — DSPI_4	I/O I/O I/O — I	S	Tristate	—	114	138	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] CS0_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	115	139	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] SOUT_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O O —	M	Tristate	—	92	116	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] SCK_4 —	SIUL eMIOS_0 DSPI_4 —	I/O I/O I/O —	M	Tristate	—	91	115	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] LIN8TX —	SIUL eMIOS_1 LINFlex_8 —	I/O I/O O —	S	Tristate	—	110	134	B14

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	134	162	A6
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	135	163	B6
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC_0	I/O I/O — O	M	Tristate	—	136	164	D5
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	137	165	C5
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC_0	I/O I/O O O	M	Tristate	—	138	166	A5
PH[9] ⁽¹⁰⁾	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	88	127	155	B8

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PI[0]	PCR[128]	AF0 AF1 AF2 AF3	GPIO[128] E0UC[28] LIN8TX —	SIUL eMIOS_0 LINFlex_8 —	I/O I/O O —	S	Tristate	—	—	172	A9
PI[1]	PCR[129]	AF0 AF1 AF2 AF3 — —	GPIO[129] E0UC[29] — — WKPU[24] ⁽⁵⁾ LIN8RX	SIUL eMIOS_0 — — WKPU LINFlex_8	I/O I/O — — I I	S	Tristate	—	—	171	A10
PI[2]	PCR[130]	AF0 AF1 AF2 AF3	GPIO[130] E0UC[30] LIN9TX —	SIUL eMIOS_0 LINFlex_9 —	I/O I/O O —	S	Tristate	—	—	170	B10
PI[3]	PCR[131]	AF0 AF1 AF2 AF3 — —	GPIO[131] E0UC[31] — — WKPU[23] ⁽⁵⁾ LIN9RX	SIUL eMIOS_0 — — WKPU LINFlex_9	I/O I/O — — I I	S	Tristate	—	—	169	C10
PI[4]	PCR[132]	AF0 AF1 AF2 AF3	GPIO[132] E1UC[28] SOUT_4 —	SIUL eMIOS_1 DSPI_4 —	I/O I/O O —	S	Tristate	—	—	143	A12



Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PI[14]	PCR[142]	AF0	GPIO[142]	SIUL	I/O	J	Tristate	—	—	76	R8
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[22]	ADC_0	I						
—	SIN_4	DSPI_4	I								
PI[15]	PCR[143]	AF0	GPIO[143]	SIUL	I/O	J	Tristate	—	—	75	T8
		AF1	CS0_4	DSPI_4	I/O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[23]	ADC_0	I						
Port J											
PJ[0]	PCR[144]	AF0	GPIO[144]	SIUL	I/O	J	Tristate	—	—	74	N5
		AF1	CS1_4	DSPI_4	O						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[24]	ADC_0	I						
PJ[1]	PCR[145]	AF0	GPIO[145]	SIUL	I/O	J	Tristate	—	—	73	P5
		AF1	—	—	—						
		AF2	—	—	—						
		AF3	—	—	—						
		—	ADC0_S[25]	ADC_0	I						
—	SIN_5	DSPI_5	I								

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function ⁽¹⁾	Function	Peripheral	I/O direction ⁽²⁾	Pad type	RESET configuration ⁽³⁾	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208 ⁽⁴⁾
PJ[2]	PCR[146]	AF0 AF1 AF2 AF3 —	GPIO[146] CS0_5 — — ADC0_S[26]	SIUL DSPI_5 — — ADC_0	I/O I/O — — I	J	Tristate	—	—	72	P4
PJ[3]	PCR[147]	AF0 AF1 AF2 AF3 —	GPIO[147] CS1_5 — — ADC0_S[27]	SIUL DSPI_5 — — ADC_0	I/O O — — I	J	Tristate	—	—	71	P2
PJ[4]	PCR[148]	AF0 AF1 AF2 AF3	GPIO[148] SCK_5 E1UC[18] —	SIUL DSPI_5 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	5	A4

1. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
2. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
3. The RESET configuration applies during and after reset.
4. LBGA208 available only as development package for Nexus2+.
5. All WKPU pins also support external interrupt capability. See the WKPU chapter for further details.
6. NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.
7. "Not applicable" because these functions are available only while the device is booting. Refer to the BAM information for details.
8. Value of PCR.IBE bit must be 0.
9. This wakeup input cannot be used to exit STANDBY mode.

- $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified.
- The configuration $PAD3V5 = 1$ when $V_{DD} = 5 \text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 20. FAST configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
V_{OH}	C	Output high level FAST configuration	$I_{OH} = -14 \text{ mA}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ (recommended)	$0.8V_{DD}$	—	—	V
			$I_{OH} = -7 \text{ mA}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 1^{(2)}$	$0.8V_{DD}$	—	—	
			$I_{OH} = -11 \text{ mA}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ (recommended)	$V_{DD} - 0.8$	—	—	
V_{OL}	C	Output low level FAST configuration	$I_{OL} = 14 \text{ mA}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$ (recommended)	—	—	$0.1V_{DD}$	V
			$I_{OL} = 7 \text{ mA}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 1^{(2)}$	—	—	$0.1V_{DD}$	
			$I_{OL} = 11 \text{ mA}$, $V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$ (recommended)	—	—	0.5	

- $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified.
- The configuration $PAD3V5 = 1$ when $V_{DD} = 5 \text{ V}$ is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

4.6.4 Output pin transition times

Table 21. Output pin transition times

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
t_{tr}	CC	Output transition time output pin ⁽²⁾ SLOW configuration	$C_L = 25 \text{ pF}$	—	—	50	ns
			$C_L = 50 \text{ pF}$			100	
			$C_L = 100 \text{ pF}$			125	
			$C_L = 25 \text{ pF}$	—	—	50	
			$C_L = 50 \text{ pF}$			100	
			$C_L = 100 \text{ pF}$			125	

Table 28. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions ⁽¹⁾		Value			Unit
						Min	Typ	Max	
I _{DDMAX} ⁽²⁾	CC	D	RUN mode maximum average current	—		—	115	140 ⁽³⁾	mA
I _{DDRUN} ⁽⁴⁾	CC	T	RUN mode typical average current ⁽⁵⁾	f _{CPU} = 8 MHz		—	12	—	mA
		f _{CPU} = 16 MHz		—	27	—			
		f _{CPU} = 32 MHz		—	43	—			
		f _{CPU} = 48 MHz		—	56	100			
		f _{CPU} = 64 MHz		—	70	125			
I _{DDHALT}	CC	C	HALT mode current ⁽⁶⁾	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	10	18	mA
		P			T _A = 125 °C	—	17	28	
I _{DDSTOP}	CC	P	STOP mode current ⁽⁷⁾	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	350	900 ⁽⁸⁾	μA
		D			T _A = 55 °C	—	750	—	
		D			T _A = 85 °C	—	2	7	mA
		D			T _A = 105 °C	—	4	10	
		P			T _A = 125 °C	—	7	14	
I _{DDSTDBY2}	CC	P	STANDBY2 mode current ⁽⁹⁾	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	30	100	μA
		D			T _A = 55 °C	—	75	—	
		D			T _A = 85 °C	—	180	700	
		D			T _A = 105 °C	—	315	1000	
		P			T _A = 125 °C	—	560	1700	
I _{DDSTDBY1}	CC	T	STANDBY1 mode current ⁽¹⁰⁾	Slow internal RC oscillator (128 kHz) running	T _A = 25 °C	—	20	60	μA
		D			T _A = 55 °C	—	45	—	
		D			T _A = 85 °C	—	100	350	
		D			T _A = 105 °C	—	165	500	
		D			T _A = 125 °C	—	280	900	

- $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to $125 \text{ }^{\circ}\text{C}$, unless otherwise specified.
- I_{DDMAX} is drawn only from the VDD_BV pin. Running consumption does not include I/Os toggling which is highly dependent on the application. The given value is thought to be a worst case value with all peripherals running, and code fetched from code flash while modify operation ongoing on data flash. Notice that this value can be significantly reduced by application: switch off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.
- Higher current may be sunk by device during power-up and standby exit. Please refer to in-rush average current in [Table 26](#).
- I_{DDRUN} is drawn only from the VDD_BV pin. RUN current measured with typical application with accesses on both Flash and RAM.
- Only for the "P" classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPI as Master, PLL as system clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

Figure 11. Crystal oscillator and resonator connection scheme

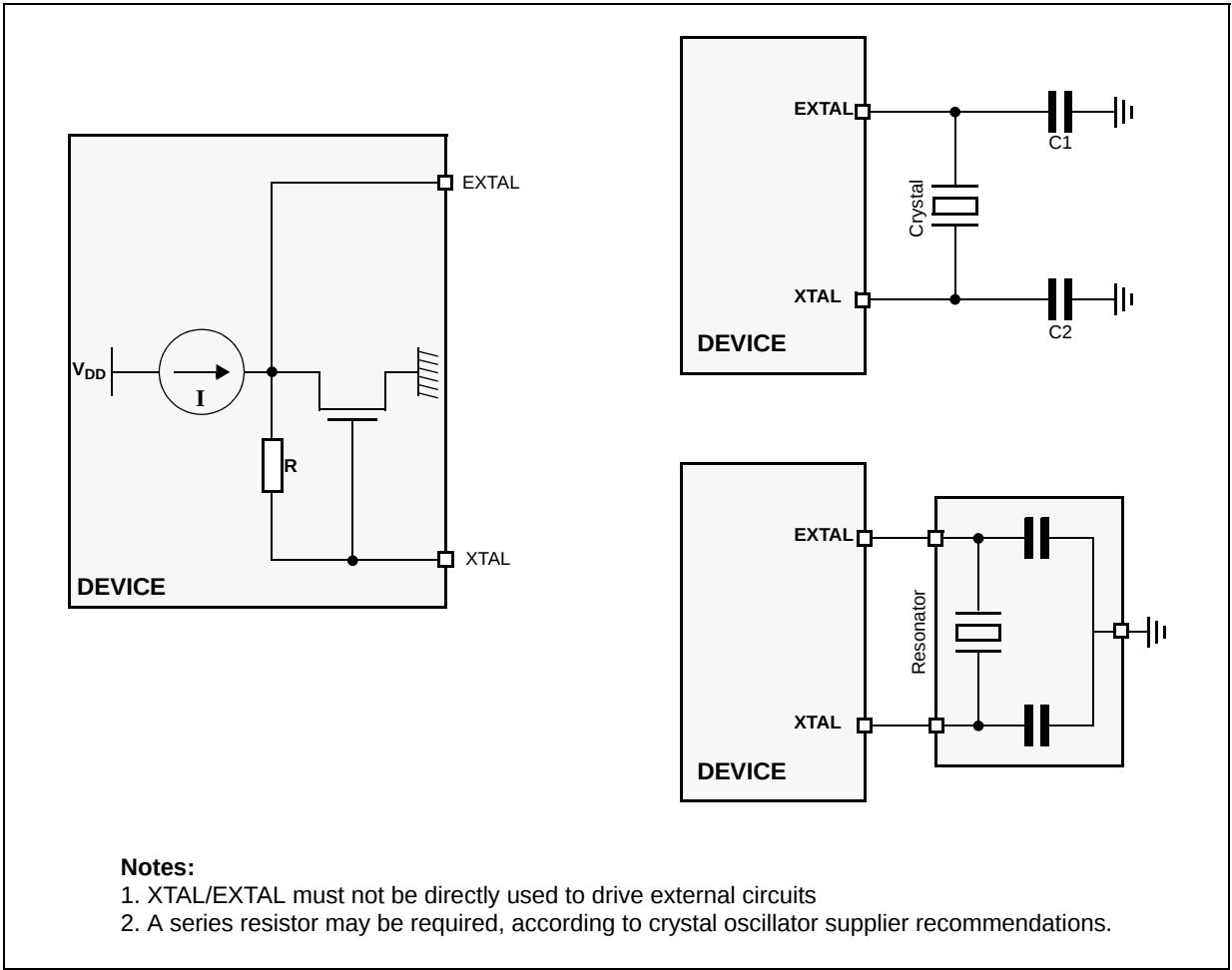


Table 37. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR Ω	Crystal motional capacitance (C_m) fF	Crystal motional inductance (L_m) mH	Load on xtalin/xtalout $C1 = C2$ (pF) ⁽¹⁾	Shunt capacitance between xtalout and xtalin $C0$ ⁽²⁾ (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

1. The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.
2. The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

[Equation 5](#) can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll t_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to [Equation 7](#):

Equation 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_S , a constraints on R_L sizing is obtained:

Equation 9 ADC_0 (10-bit)

$$8.5 \cdot \tau_2 = 8.5 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_S$$

Equation 10 ADC_1 (12-bit)

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < t_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . [Equation 11](#) must be respected (charge balance assuming now C_S already charged at V_{A1}):

Revision history

[Table 56](#) summarizes revisions to this document.

Table 56. Revision history

Date	Revision	Changes
12-Jan-2009	1	Initial release
07-Dec-2009	2	Updated Device Summary-added LBGA208 Part number Updated Features Replaced 27 IRQs in place of 23 ADC features External Ballast resistor support conditions Updated device summary-added 208 BGA details Updated block diagram to include WKUP Updated block diagram to include 5 ch ADC 12 -bit Updated Block summary table Updated LQFP 144, 176 and 100 pinouts. Applied new naming convention for ADC signals as ADCx_P[x] and ADCx_S[x] Section 1, "General description Updated SPC560B54/60/64 device comparison table Updated block diagram-aligned with 512k Updated block summary-aligned with 512k Section 2, "Package pinouts Updated 100,144,176,208 packages according to cut2.0 changes Added Section 3.5.1, "External ballast resistor recommendations Added NVUSRO [WATCHDOG_EN] field description Updated Absolute maximum ratings Updated LQFP thermal characteristics Updated I/O supply segments Updated Voltage regulator capacitance connection Updated Low voltage monitor electrical characteristics Updated Low voltage power domain electrical characteristics Updated DC electrical characteristics Updated Program/Erase specifications Updated Conversion characteristics (10 bit ADC) Updated FMPLL electrical characteristics Updated Fast RC oscillator electrical characteristics-aligned with SPC560B4x/B5x/C4x/C5x Updated On-chip peripherals current consumption Updated ADC characteristics and error definitions diagram Updated ADC conversion characteristics (10 bit and 12 bit) Added ADC characteristics and error definitions diagram for 12 bit ADC