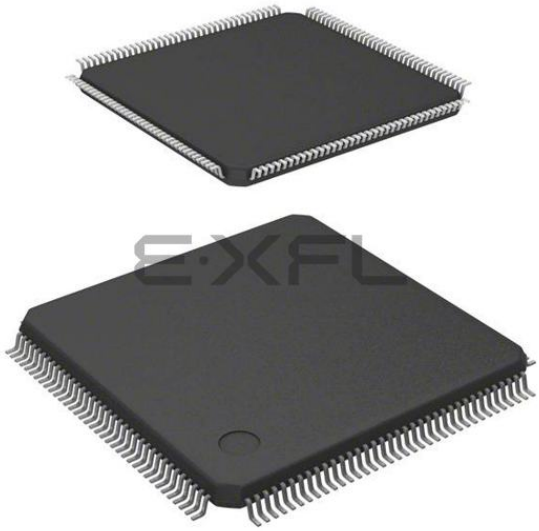

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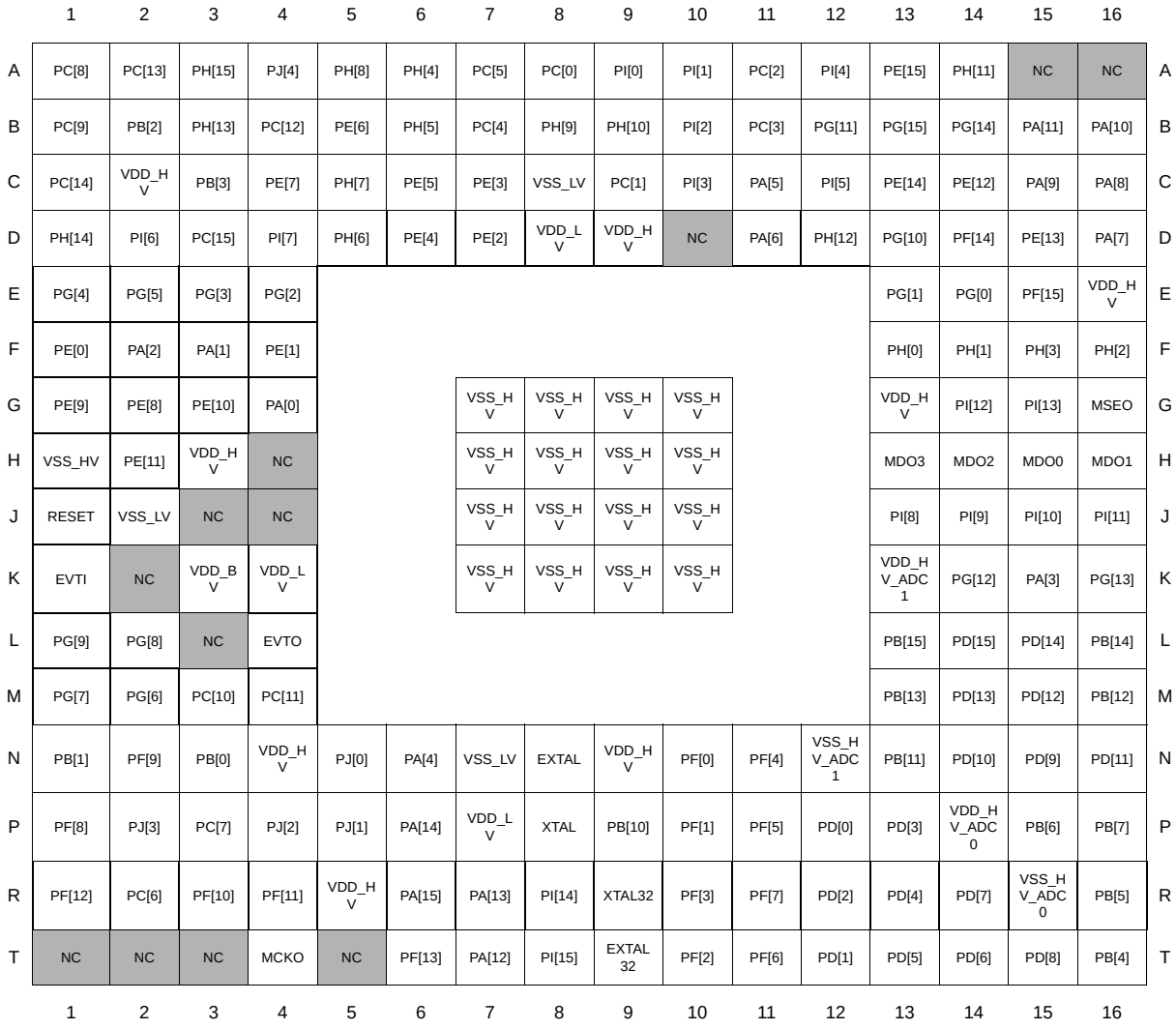
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 53x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560b60l5b6e0x

List of tables

Table 3. SPC560B54/6x series block summary (continued)

Block	Function
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	PH[15]	PJ[4]	PH[8]	PH[4]	PC[5]	PC[0]	PI[0]	PI[1]	PC[2]	PI[4]	PE[15]	PH[11]	NC	NC	A
B	PC[9]	PB[2]	PH[13]	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	PI[2]	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	PI[3]	PA[5]	PI[5]	PE[14]	PE[12]	PA[9]	PA[8]	C
D	PH[14]	PI[6]	PC[15]	PI[7]	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	PH[12]	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV	PI[12]	PI[13]	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC			VSS_HV	VSS_HV	VSS_HV	VSS_HV			PI[8]	PI[9]	PI[10]	PI[11]	J
K	EVTI	NC	VDD_BV	VDD_LV			VSS_HV	VSS_HV	VSS_HV	VSS_HV			VDD_HV_ADC1	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	VDD_HV	PJ[0]	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	VSS_HV_ADC1	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	PJ[3]	PC[7]	PJ[2]	PJ[1]	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC0	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	PI[14]	XTAL32	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC0	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	PI[15]	EXTAL32	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

NOTE: The LBGA208 is available only as development package for Nexus 2+.

NC = Not connected

Figure 5. LBGA208 configuration

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8], PC[0] and PH[9:10] are in input weak pull-up when out of reset.
- RESET pad is driven low by the device till 40 FIRC clock cycles after phase2 completion. Minimum phase3 duration is 40 FIRC cycles.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

Table 5. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number			
					LQFP 100	LQFP 144	LQFP 176	LBGA 208(1)
RESET	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input weak pull-up after RGM PHASE2 and 40 FIRC cycles	17	21	29	J1
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.	I/O	X	Tristate	36	50	58	N8
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator bypass mode is used.	I	X	Tristate	34	48	56	P8

1. LBGA208 available only as development package for Nexus2+.

3.7 Functional port pins

The functional port pins are listed in *Table 6*.

Table 6. Functional port pin descriptions

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
Port A											
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT E0UC[13] WKPU[19][5]	SIUL eMIOS_0 MC_CGM eMIOS_0 WKPU	I/O I/O O I/O I	M	Tristate	12	16	24	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 —	GPIO[1] E0UC[1] NMI[6] — WKPU[2][5]	SIUL eMIOS_0 WKPU — WKPU	I/O I/O I — I	S	Tristate	7	11	19	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — MA[2] WKPU[3][5]	SIUL eMIOS_0 — ADC_0 WKPU	I/O I/O — O I	S	Tristate	5	9	17	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 — —	GPIO[3] E0UC[3] LIN5TX CS4_1 EIRQ[0] ADC1_S[0]	SIUL eMIOS_0 LINFlex_5 DSPI_1 SIUL ADC_1	I/O I/O O O I I	J	Tristate	68	90	114	K15

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
Port C											
PC[0][10]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	87	126	154	A8
PC[1][10]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F[11]	Tristate	82	121	149	C9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX DEBUG[0] EIRQ[5]	SIUL DSPI_1 FlexCAN_4 SSCM SIUL	I/O I/O O O I	M	Tristate	78	117	145	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] DEBUG[1] EIRQ[6] CAN1RX CAN4RX	SIUL DSPI_1 ADC_0 SSCM SIUL FlexCAN_1 FlexCAN_4	I/O I/O O O I I I	S	Tristate	77	116	144	B11

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC0_S[4]	SIUL DSPI_0 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	—	—	100	M15
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC0_S[5]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O I/O I/O — I	J	Tristate	62	84	102	M14
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC0_S[6]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	64	86	104	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC0_S[7]	SIUL DSPI_1 eMIOS_0 — ADC_0	I/O O I/O — I	J	Tristate	66	88	106	L14
Port E											

Table 6. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration[3]	Pin number			
								LQFP 100	LQFP 144	LQFP 176	LBGA 208[4]
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ADC0_S[11]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	58	66	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ADC0_S[12]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	59	67	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ADC0_S[13]	SIUL eMIOS_0 DSPI_2 — ADC_0	I/O I/O O — I	J	Tristate	—	60	68	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] CS1_1 — ADC0_S[14]	SIUL eMIOS_0 DSPI_1 — ADC_0	I/O I/O O — I	J	Tristate	—	61	69	T11
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — CS2_1 — ADC0_S[15]	SIUL — DSPI_1 — ADC_0	I/O — O — I	J	Tristate	—	62	70	R11

4.4 Recommended operating conditions

Table 13. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{SS}	SR	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}(1)	SR	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}(2)	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_BV}(3)	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V_{SS})	—	3.0	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC0, VSS_HV_ADC1 (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}(4)	SR	Voltage on VDD_HV_ADC0, VDD_HV_ADC1 (ADC reference) with respect to ground (V_{SS})	—	3.0(5)	3.6	V
			Relative to V_{DD}	V_{DD} – 0.1	V_{DD} + 0.1	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	—	V
			Relative to V_{DD}	—	V_{DD} + 0.1	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–5	5	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	
TV_{DD}	SR	V_{DD} slope to ensure correct power up(6)	—	3.0(7)	250×10^3 (0.25 [V/µs])	V/s

1. 100 nF capacitance needs to be provided between each V_{DD}/V_{SS} pair.
2. 330 nF capacitance needs to be provided between each V_{DD_LV}/V_{SS_LV} supply pair.
3. 470 nF capacitance needs to be provided between V_{DD_BV} and the nearest V_{SS_LV} (higher value may be needed depending on external regulator characteristics). Supply ramp slope on VDD_BV should always be faster or equal to slope of VDD_HV. Otherwise, device may enter regulator bypass mode if slope on VDD_BV is slower.
4. 100 nF capacitance needs to be provided between V_{DD_ADC}/V_{SS_ADC} pair.
5. Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below V_{LVDHVL}, device is reset.
6. Guaranteed by device validation.
7. Minimum value of TV_{DD} must be guaranteed until V_{DD} reaches 2.6 V (maximum value of V_{PORH}).

Equation 2 $P_D = K / (T_J + 273\ °C)$

Therefore, solving equations <Cross Refs>1 and <Cross Refs>2:

Equation 3 $K = P_D \times (T_A + 273\ °C) + R_{\theta JA} \times P_D^2$

Where:

K is a constant for the particular part, which may be determined from *Equation 3* by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations *Equation 1* and *Equation 2* iteratively for any value of T_A.

4.6 I/O pad electrical characteristics

4.6.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—provide maximum speed. These are used for improved Nexus debugging capability.
- Input only pads—are associated with ADC channels and 32 kHz low power external crystal oscillator providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

4.6.2 I/O input DC characteristics

Table 16 provides input DC electrical characteristics as described in *Figure 6*.

Table 18. SLOW configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 19. MEDIUM configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	C	Output high level MEDIUM configuration	Push Pull	I_{OH} = –3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	V
		P			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	$0.8V_{DD}$	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
		C			I_{OH} = –100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	$0.8V_{DD}$	—	—	
V_{OL}	CC	C	Output low level MEDIUM configuration	Push Pull	I_{OL} = 3.8 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.2V_{DD}$	V
		P			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	
		C			I_{OL} = 100 µA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	$0.1V_{DD}$	

Table 21. Output pin transition times (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin[2] FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.6.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 22*.

Table 23 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 22. I/O supply segments

Package	Supply segment							
	1	2	3	4	5	6	7	8
LBGA208 (1)	Equivalent to LQFP176 segment pad distribution						MCKO	MDOn /MSEO
LQFP176	pin7 – pin27	pin28 – pin57	pin59 – pin85	pin86 – pin123	pin124 – pin150	pin151 – pin6	—	—
LQFP144	pin20 – pin49	pin51 – pin99	pin100 – pin122	pin 123 – pin19	—	—	—	—
LQFP100	pin16 – pin35	pin37 – pin69	pin70 – pin83	pin84 – pin15	—	—	—	—

1. LBGA208 available only as development package for Nexus2+.

6. Data Flash Power Down. Code Flash in Low Power. SIRC 128 kHz and FIRC 16 MHz on. 10 MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clocks gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 to 9 clocks gated. eMIOS: instance: 0 ON (16 channels on PA[0]–PA[11] and PC[12]–PC[15]) with PWM 20 kHz, instance: 1 clock gated. DSPI: instance: 0 (clocked but no communication), instance: 1 to 5 clocks gated. RTC/API ON. PIT ON. STM ON. ADC1 OFF. ADC0 ON but no conversion except two analog watchdogs.
7. Only for the “P” classification: No clock, FIRC 16 MHz off, SIRC 128 kHz on, PLL off, HPVreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.
8. When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.
9. Only for the “P” classification: ULPreg on, HP/LPVreg off, 32 KB RAM on, device configured for minimum consumption, all possible modules switched off.
10. ULPreg on, HP/LPVreg off, 8 KB RAM on, device configured for minimum consumption, all possible modules switched off.

4.10 Flash memory electrical characteristics

4.10.1 Program/erase characteristics

Table 29 shows the program and erase characteristics.

Table 29. Program and erase specifications

Symbol		C	Parameter	Conditions	Value				Unit
					Min	Typ (1)	Initial max (2)	Max (3)	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time(4)	Code Flash	—	18	50	500	µs
				Data Flash		22			
$t_{16Kpperase}$			16 KB block preprogram and erase time	Code Flash	—	200	500	5000	ms
				Data Flash		300			
$t_{32Kpperase}$			32 KB block preprogram and erase time	Code Flash	—	300	600	5000	ms
				Data Flash		400			
$t_{128Kpperase}$			128 KB block preprogram and erase time	Code Flash	—	600	1300	7500	ms
				Data Flash		800			
t_{esus}		D	Erase Suspend Latency	—	—	—	30	30	µs
t_{ESRT}		C	Erase Suspend Request Rate(5)	Code Flash	20	—	—	—	ms
				Data Flash	10	—	—	—	

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Time between erase suspend resume and the next erase suspend request.

Table 43. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\Delta_{SIRCPRE}$	CC	C	Slow internal RC oscillator precision after software trimming of f_{SIRC}	T_A = 25 °C	–2	—	2	%
$\Delta_{SIRCTRIM}$	CC	C	Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

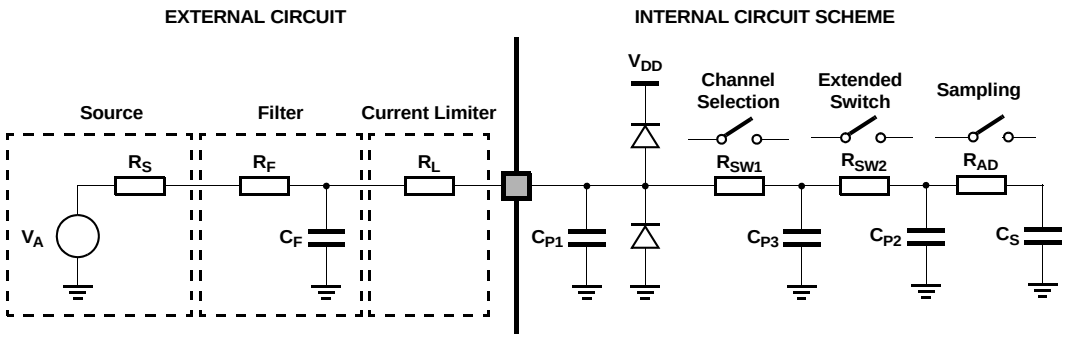
1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.
2. This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides two Successive Approximation Register (SAR) analog-to-digital converters (10-bit and 12-bit).

Figure 18. Input equivalent circuit (extended channels)



R_S Source Impedance

R_F Filter Resistance

C_F Filter Capacitance

R_L Current Limiter Resistance

R_{SW} Channel Selection Switch Impedance (two contributions R_{SW1} and R_{SW2})

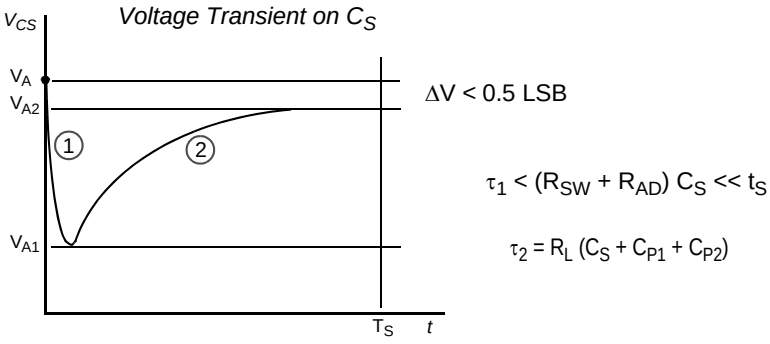
R_{AD}Sampling Switch Impedance

C_P Pin Capacitance (three contributions, C_{P1}, C_{P2} and C_{P3})

C_S Sampling Capacitance

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 17*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 19. Transient behavior during sampling phase



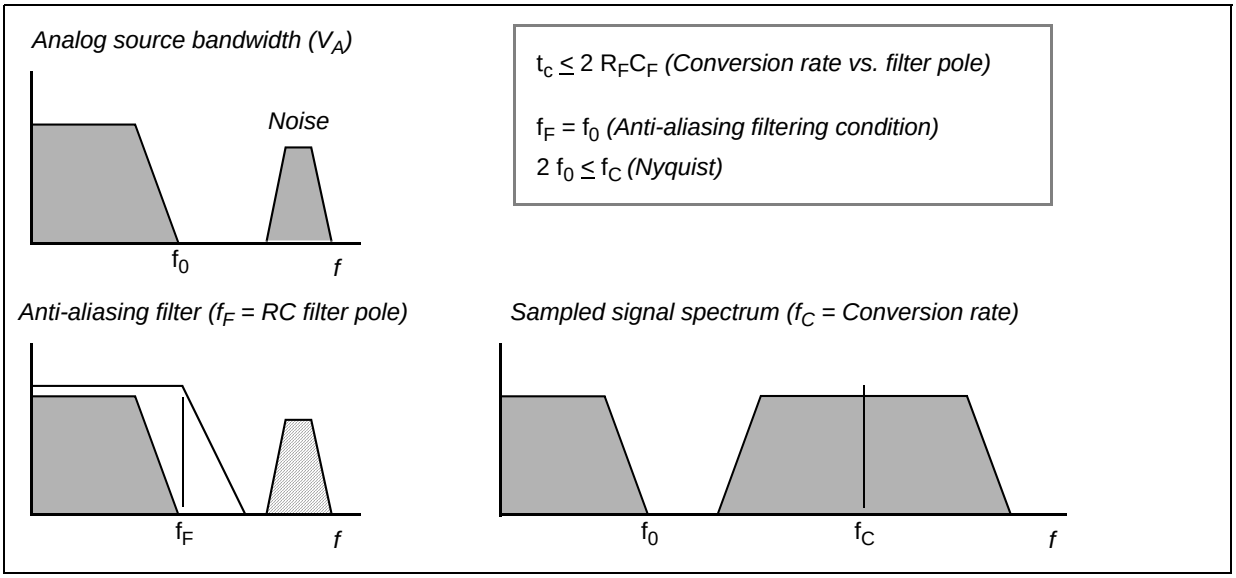
In particular two different transient periods can be distinguished:

Equation 11

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as antialiasing.

Figure 20. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the antialiasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (t_c). Again the conversion period t_c is longer than the sampling time t_s, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time t_s, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 12* between the ideal and real sampled voltage on C_S:

Equation 12

$$\frac{V_{A2}}{V_A} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

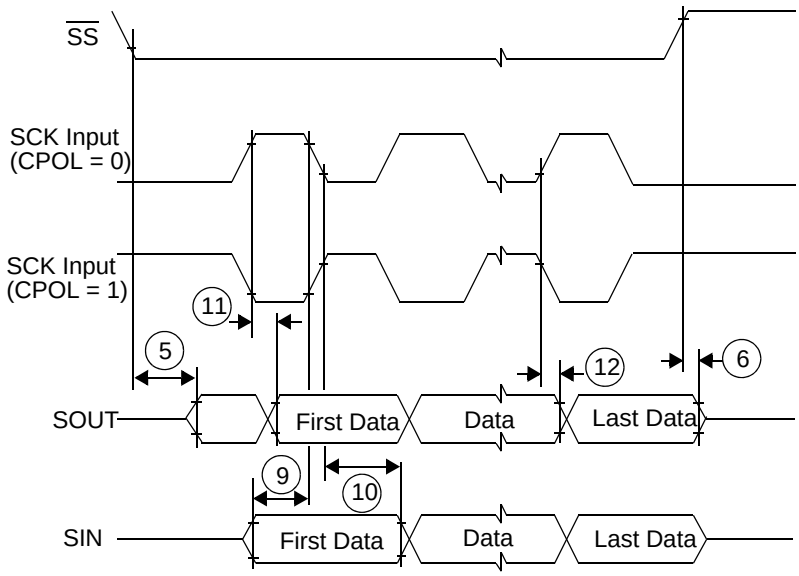
Equation 13 ADC_0 (10-bit)

$$C_F > 2048 \bullet C_S$$

Table 46. ADC_1 conversion characteristics (12-bit ADC_1) (continued)

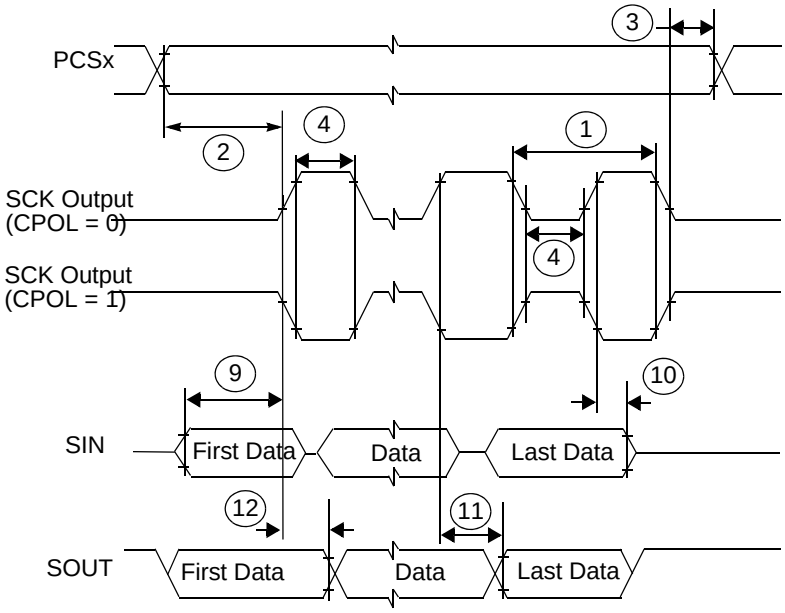
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$I_{ADC1pwd}$	SR	—	ADC_1 consumption in power down mode	—	—	—	50	µA
$I_{ADC1run}$	SR	—	ADC_1 consumption in running mode	—	—	—	6	mA
f_{ADC1}	SR	—	ADC_1 analog frequency	V_{DD} = 3.3 V	3.33	—	20 + 4%	MHz
				V_{DD} = 5 V	3.33	—	32 + 4%	
t_{ADC1_PU}	SR	—	ADC_1 power up delay	—	—	—	1.5	µs
t_{ADC1_S}	CC	T	Sampling time[4] V_{DD} = 3.3 V	f_{ADC1} = 20 MHz, INPSAMP = 12	600	—	—	ns
			Sampling time[4] V_{DD} = 5.0 V	f_{ADC1} = 32 MHz, INPSAMP = 17	500	—	—	
			Sampling time[4] V_{DD} = 3.3 V	f_{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
			Sampling time[4] V_{DD} = 5.0 V	f_{ADC1} = 3.33 MHz, INPSAMP = 255	—	—	76.2	
t_{ADC1_C}	CC	P	Conversion time[5] V_{DD} = 3.3 V	f_{ADC1} = 20 MHz, INPCMP = 0	2.4	—	—	µs
			Conversion time[5] V_{DD} = 5.0 V	$f_{ADC\ 1}$ = 32 MHz, INPCMP = 0	1.5	—	—	µs
			Conversion time[5] V_{DD} = 3.3 V	$f_{ADC\ 1}$ = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
			Conversion time[5] V_{DD} = 5.0 V	f_{ADC1} = 13.33 MHz, INPCMP = 0	—	—	3.6	µs
Δ_{ADC1_SYS}	SR	—	ADC_1 digital clock duty cycle	ADCLKSEL = 1[6]	45	—	55	%
C_S	CC	D	ADC_1 input sampling capacitance	—	—	—	5	pF
C_{P1}	CC	D	ADC_1 input pin capacitance 1	—	—	—	3	pF
C_{P2}	CC	D	ADC_1 input pin capacitance 2	—	—	—	1	pF
C_{P3}	CC	D	ADC_1 input pin capacitance 3	—	—	—	1.5	pF
R_{SW1}	CC	D	Internal resistance of analog source	—	—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—	—	—	0.3	kΩ

Figure 25. DSPI classic SPI timing — slave, CPHA = 1



Note: Numbers shown reference *Table 47*.

Figure 26. DSPI modified transfer format timing — master, CPHA = 0



Note: Numbers shown reference *Table 47*.

5.2.3 LQFP100

Figure 35. LQFP100 package mechanical drawing

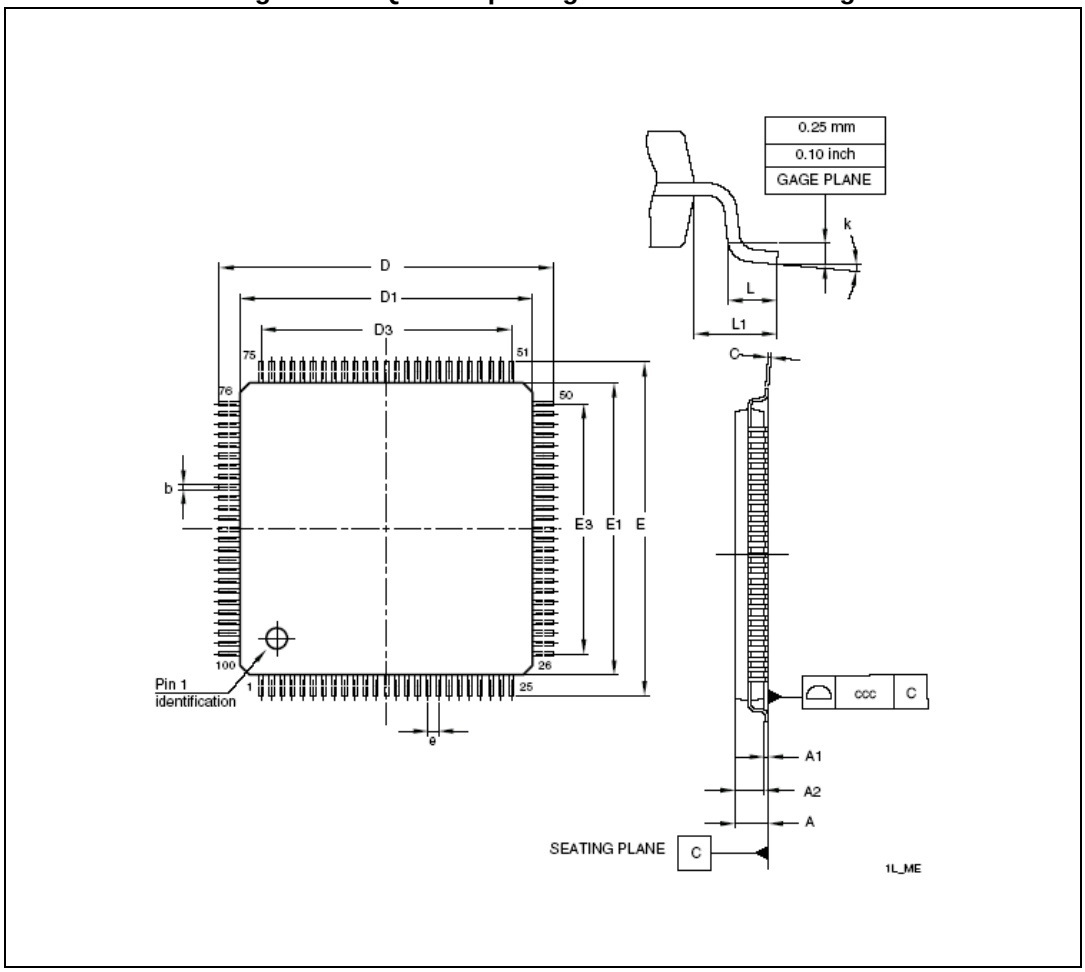


Table 53. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 56. Revision history (continued)

Date	Revision	Changes
12-Sep- 2011	6	Editorial and formatting changes throughout Replaced instances of “e200z0” with “e200z0h” Device family comparison table: – added 1 MB code flash LQFP100 version – added 1.5 MB code flash LQFP144 version – removed 768 KB code flash LQFP176 version – changed LINFlex count for 144-pin LQFP—was ‘6’; is ‘8’ – changed LINFlex count for 176-pin LQFP—was ‘8’; is ‘10’ – replaced 105 °C with 125 °C in footnote 2 SPC560B54/6x block diagram: added GPIO and VREG to legend SPC560B54/6x series block summary: added acronym “JTAGC”; in WKPU function changed “up to 18 external sources” to “up to 27 external sources” LQFP144 pin configuration: for pins 37–72, restored the pin labels that existed prior to 27 July 2010 LQFP176 pin configuration: corrected name of pin 4: was EPC[15]; is PC[15] Added following sections: – Pad configuration during reset phases – Pad configuration during standby mode exit – Voltage supply pins – Pad types – System pins – Functional port pins – Nexus 2+ pins Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality; updated footnote describing default value of ‘1’ in field descriptions NVUSRO[PAD3V5V] and NVUSRO[OSCILLATOR_MARGIN] Added section “NVUSRO[WATCHDOG_EN] field description” Tables “Absolute maximum ratings” and “Recommended operating conditions (3.3 V)”: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description “Recommended operating conditions (5.0 V)” table: replaced “VSS_HV_ADC0, VSS_HV_ADC1” with “VDD_HV_ADC0, VDD_HV_ADC1” in V_{DD_ADC} parameter description; changed 3.6V to 3.0V in footnote 2 Section “External ballast resistor recommendations”: replaced “low voltage monitor” with “low voltage detector (LVD)” “I/O input DC electrical characteristics” table: updated I_{LKG} characteristics “MEDIUM configuration output buffer electrical characteristics” table: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O weight: updated table (includes replacing instances of bit “SRE” with “SRC”) “Reset electrical characteristics” table: updated parameter classification for $\lvert I_{WPU} \rvert$ Updated voltage regulator electrical characteristics Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); changed “as well as four low voltage detectors” to “as well as five low voltage detectors”; added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; updated values for $V_{LVDLVBKPL}$ and $V_{LVDLVCORL}$ Updated section “Power consumption”